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Design and Analysis of CMOS Cells using Adiabatic Logic

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ABSTRACT

This paper deals with two types of inverter structure design using CMOS and adiabatic technique. Power consumption is the important and basic parameters of any kind of digital integrated circuit (IC). There is always a tradeoff between power and performance to meet the systems requirement. System cost is directly affected by power. Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and which recycle the energy from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. All simulation result and analysis are perform on 180nm TSMC technology using tanner tool.

Keywords: Low Power, VLSI, Dynamic Power Dissipation, Static Power Dissipation, Adiabatic logic, Capacitor.

1. INTRODUCTION

New generations of processing technology are being developing while present generation of devices are at very safe distance from fundamental physical limits. Need for low power VLSI chips arise from such evolution forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors that dissipated about 1 watt of power and at 1 MHz frequency. After that Pentium comes in 2001, which has 42 million transistors, dissipating 65 watts of power at a frequency of 2.4 GHz. If power density rises in this exponential way increase continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electro migration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance. Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field.

Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power. A study by American Council for an Energy-Efficient Economy estimated that office equipment account for 5% for the total US commercial energy usage in 1997 and could rise to 10% by the year 2004 if no actions are taken to prevent the trend [7].

Power consumption is one of the basic parameters of any kind of integrated circuit (IC). Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost.

2. POWER AND ENERGY DEFINITION

The total power consumed by a device is, the energy consumed per unit time. In other words, we can say that energy (E) required for a given operation is the integral of the power (P) consumed over the operation time (T) hence,

$$E = \int_0^T P(t)dt \qquad (1)$$

Here, the power of digital CMOS circuit is given by

$$P = C V_{DD}^2 f \qquad (2)$$

Where, C is the capacitance being recharged during a transition period. VDD is the supply voltage, Vs is the voltage swing of the signal, and f is the clock frequency. Let assumed that an operation requires n clock cycles, then T can be expressed as n / f. Hence, Equation (1) can be rewritten as

$$E = n C_{VDD} VS \qquad (3)$$

It is important to note that the energy required per operation is independent of the clock frequency. Then it is more convenient to talk about power consumption of digital circuits at this point. Although power depends greatly on the circuit design style, it can be divided, into static and dynamic power. In all of the logic families except for the push-pull types such as CMOS, the static power tends to dominate. Due to this reason CMOS is the most suitable circuit style for very large scale integration (VLSI). The power consumed by the CMOS circuit can be divided into two basic classes static and dynamic.

2.1 Static Power

The static or steady state power dissipation of a circuit depends upon logical state of circuit rather than switching activities and is expressed as

$$P_{static} = I_{static} V_{DD} \qquad (4)$$

where, I_{static} is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static (DC) power as in steady state there is no direct path from V_{DD} to ground because PMOS and NMOS transistors are never becomes on simultaneously. Therefore static power dissipation is due to leakage currents and substrate injection currents. Another form of static power dissipation that occurs is called Ratioed logic. Pseudo-NMOS is an example of a Ratioed CMOS logic. In this, the PMOS pull-up transistor is always in on condition and acts as a load device for the NMOS pull-down network. Therefore, when the gate output is in low-state, there is a direct path from V_{DD} to ground and the static currents flow. In this state, the exact value of the output voltage depends on the ratio of PMOS and NMOS network hence the name. The static power consumed by these logic families can be considerable shown in Figure 1.

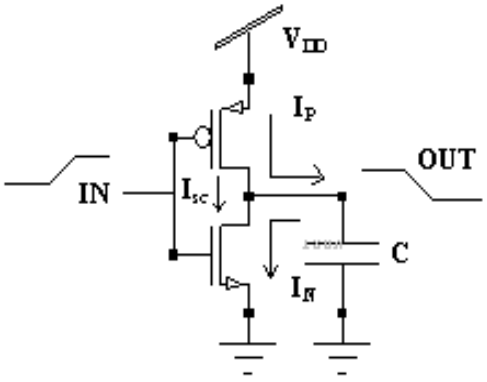

Figure 1: CMOS Inverter for power analysis

2.2 Dynamic Power

Dynamic power dissipation is related to switching activities of device. At some point during the switching transient time, both the NMOS and PMOS devices become turned on. This condition occurs for gate voltages between Vtn and V_{DD} - Vtp. During this time, a short circuit path exists between V_{DD} and ground that allowed the currents to flow. Although short circuit power dissipation cannot be always completely ignored, it is certainly not the dominant component of power dissipation in CMOS circuits. Instead, dynamic power dissipation due to capacitance charging and discharging consumes most of the power. This component of dynamic power dissipation is the result of charging and discharging of the parasitic capacitances in the circuit.

The situation is modeled in Figure 1, where the parasitic capacitances are lumped at the output of the inverter. Consider the behavior of the circuit over one full cycle of operation with the input voltage going from V_{DD} to ground and back to V_{DD} again. As the input switches from high state to low state, the NMOS pull-down network is in cut-off region and PMOS pull-up network is in linear region charging the load capacitance C up to V_{DD}. This charging process draws energy equal to CV_{DD}^2 from the power supply. Half of this is energy is dissipated immediately in the PMOS transistors, while the other half part is stored on the load capacitance. After that when the input returns to V_{DD}, the process is reversed and the capacitance is discharged, its energy is being dissipated in the NMOS network. In other way , every time a capacitive node switches from ground to V_{DD} (and back to ground), energy of CV_{DD}^2 is consumed. This leads to the conclusion that CMOS power consumption depends on the switching activity of the signals involved. Now we can define activity, α as the expected number of zero to one transition per data cycle. If this is coupled with the average data rate, f is the clock frequency in a synchronous system, then the effective frequency of nodal charging is given by the product of the activity and the data rate: αf. Therefore average CMOS power consumption is

$$P_{dyn} = CV_{DD}^2 f \qquad (5)$$

3. ADIABATIC LOGIC CIRCUITS

Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and also which recycles the energy from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. As such every time a charge-

discharge cycle occurs, an amount of energy equal to CV_{dd}^2 is dissipated. Unlike the conventional CMOS circuits, in adiabatic circuits energy is recycled.

3.1 Principle of Adiabatic Switching

Adiabatic switching is used to minimize energy losses during the charging/discharging cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time varying voltage source instead of a fixed voltage supply. Here, the load capacitance (CL) is charged by using a constant current source (I) while in conventional CMOS logic we use constant voltage source to charge the load capacitance. Here R is the on-resistance of PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume the capacitor voltage zero initially shown in Figure 2.

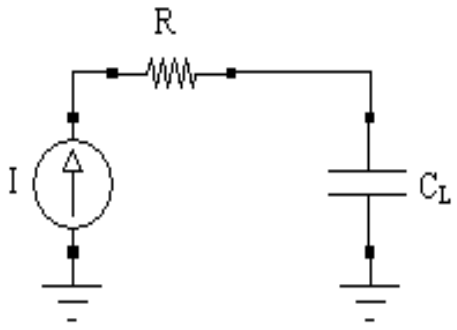

Figure 2: Adiabatic logic circuit

Theoretically, when driving voltage (Va) switching time (T) from 0 V to Vdd is long, the energy dissipation is nearly zero. When Va changes from high state to low state in pull- down network, discharging path via the NMOS transistor is created. From this, it is observed that energy dissipation is minimized by decreasing the rate of switching transition, and the system draws some of the energy that is stored in the load capacitor during the current subsequent computational steps. A system based on this above-mentioned technique is not necessarily reversible for charge recovery.

3.2 A Simple Adiabatic Logic Gate

In this we will examine simple circuit configurations which can be used for adiabatic switching. A general circuit topology for the conventional CMOS gates and adiabatic counterparts is shown in Figure 3. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up transistor and the pull-down transistor networks must be replaced with complementary transmission-gate (T-gate). The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pull-down function drives the complementary output node. Note that all the inputs should also be available in complementary form.

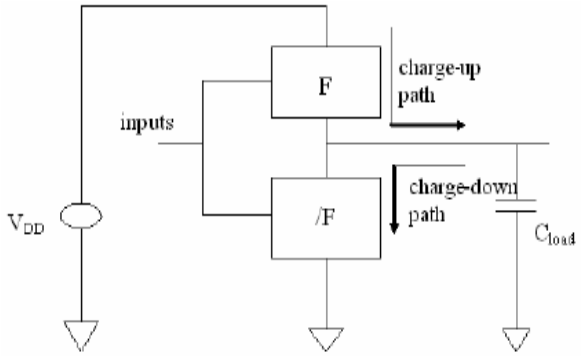

Figure 3: The general circuit topology of a conventional CMOS logic gate

Both the pull-up and pull-down networks in the adiabatic logic circuit are used for charging as well as discharging the output node capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle shown in Figure 4. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a varying power supply with the ramped voltage output.

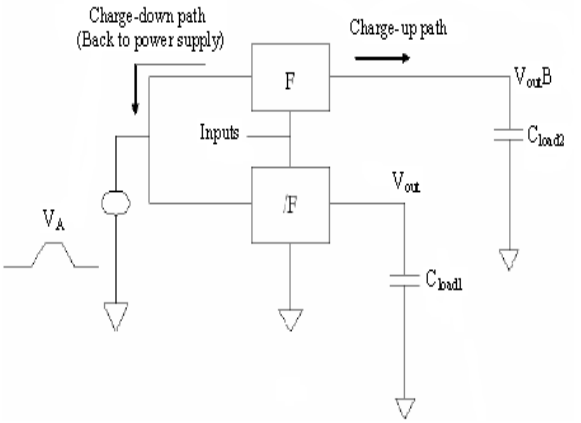

Figure 4: The topology of an adiabatic logic gate Implementing the same function

The necessary circuit modifications which are used to convert a conventional CMOS logic circuit into an

adiabatic logic circuit increase the device count by a factor of two or even more.

4. IMPLEMENTATION AND RESULT

Dissipation of power in conventional CMOS circuits primarily occurs during the device switching time. When the logic level in the system is "1," there is a sudden flow of current through R. Q = C_LVdd is the charge supplied by the positive power supply rail for charging CL to the level of Vdd. Hence, the energy drawn from the power supply is Q·Vdd = $C_L Vdd^2$ which shown in Figure.5.

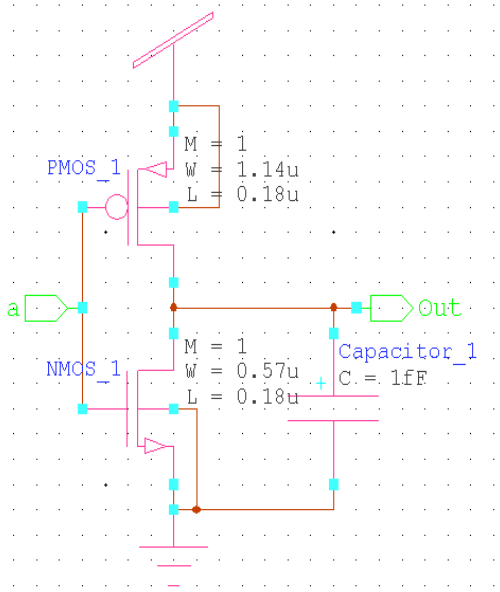

Figure 5: CMOS inverter circuit

By assuming that the energy drawn from the power supply is equal to that supplied to CL, the energy stored in CL is said to be one-half the supplied energy, i.e., Estored = (1/2)CLVdd2.The output waveform of conventional CMOS shown in Figure 6.

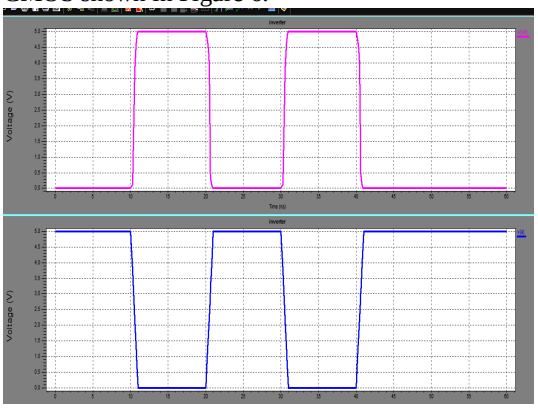

Figure 6: Waveforms of input and output voltage

4.1 Proposed adiabatic logic inverter

Adiabatic switching is commonly used to minimize energy loss during the charge/discharge cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time varying voltage source instead of a fixed voltage supply. This is accomplished by using AC power supplies to charge the circuit during the specific adiabatic phases and subsequently discharge the circuit to recover the supplied charge. The peak current in adiabatic circuits can be significantly reduced by ensuring uniform charge transfer over the entire time available. Hence, if I is considered as the average of the current flowing to CL, the overall energy dissipated during the transition phase can be reduced in proportion to

$$I2RTp = (C_L Vdd/ Tp)^2 RTp$$
$$= (RCL/Tp)\, C_L Vdd^2 \quad \ldots. (10)$$

Theoretically, during adiabatic charging, when Tp, the time for the driving voltage Va to change from 0 V to Vdd is long, energy dissipation is nearly zero. When VaB changes from HIGH to LOW in the pull-down network, discharging via the NMOS transistor occurs. From Eq. (10), it is apparent that when energy dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the capacitors during a given computation step and uses it during subsequent computations. Systems based on the above-mentioned theory of charge recovery are not necessarily reversible. The basic inverter circuit is shown in Figure7. In this circuit is an adiabatic amplifier, a latch made by the two PMOS M1 and M2 and two NMOS M5 and M6, that avoids the logic level degradation at Out and Outb, the logic circuit M3 and M4 are in parallel with M1 and M2 and forms transmission gate . This circuit uses two-phase split level sinusoidal power supplies which are denoted as Va and VaB, where Va & VaB can vary from 1.3 to 1.6V & 0.3 to 0V respectively. The circuit operates in two phases, evaluation and hold, in evaluation phase, Va swings up and VaB swings down, and in hold phase, VaB swings up and Va swings down.

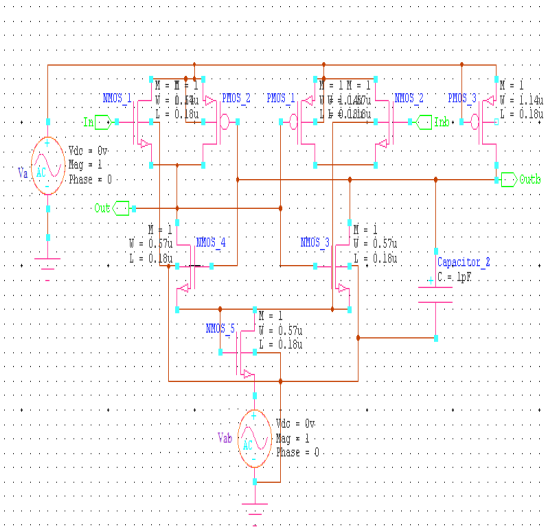

Figure 7: Proposed adiabatic logic inverter circuit

Let us assume, during evaluation phase the input (In) is high and input (InB) goes low accordingly, consequently M3 is conducting and output (OutB) follows the power supply Va, and at the same time M1 gets turned ON by output (Out) and thus reduces the charging resistance. Being in parallel with M3 and during hold phase, charge stored on the load capacitance CL flows back to power supply through M1. So that power dissipation is reduced. The proposed circuit uses two MOS diodes, one is connected to Out and Va and other diode is connected between

Table 1: Power Consumption comparison of proposed inverter vs CMOS

V_{DD} (Volts)	Power Consumption (Watts)	
	CMOS	Proposed
1.2	5.054443E-008	2.450000E-013
1.4	6.595536E-008	2.780000E-012
1.6	8.316927E-008	3.480000E-010
1.8	9.878095E-008	4.980000E-010

Common source of M5-M6 and other power supply VaB, Both the MOS diodes are used to increase the discharging rate of internal nodes. The power analysis of conventional CMOS and proposed inverter is given in Table 1.

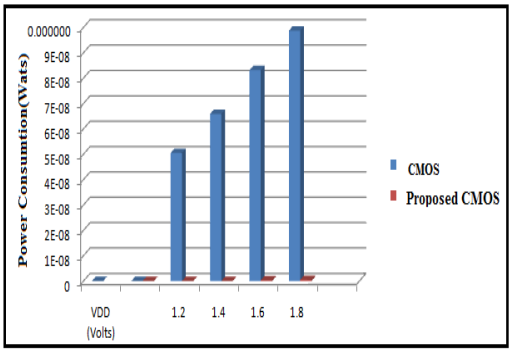

Figure 8: Power Consumption comparison of proposed inverter vs CMOS at power supply

5. CONCLUSION

Simulation results obtained from the proposed inverter and CMOS gate has wide acceptance in low power VLSI regime at low frequency. The comparison of the proposed circuit with other traditional methodologies has proved that power consumption with the proposed logic is far less as compared to CMOS based technique. The simulation result shows that power consumption of proposed adiabatic CMOS inverter is less compare to CMOS inverter. All simulation result and analysis are performing using 180nm TSMC technology using tanner tool.

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