ISSN
Volume 1, No.1, September - October 2012
International Journal of Information Systems and Computer Sciences
Available Online at http://warse.org/pdfs/ijiscs04112012.pdf

Design of multi-precision reconfigurable Wallace Tree Multiplier for high performance applications

Monika Vaishnav
M.Tech (Scholar), Mewar Universiy, Chittorgarh, Rajasthan (India)
Vaishnav.monika2@gmail.com

ABSTRACT

We designed reconfigurable 8x8 multiplier architecture in 180nm with 1.8 power supply based on Wallace Tree, efficient in power and regularity without increase in delay and area. The idea is the generation of partial products in parallel using AND gates. The addition of partial products is reducing using Wallace Tree which is hierarchically divided into levels. Therefore there will be a significant reduction in the power consumption, since power is provided only to the level that is involved in computation and the remaining two levels switched off. To improve the speed of addition at the final level of computation, a carry look-ahead adder (CLA) is used which is better in terms of area/speed.

Keywords: 180 nm technology, Low power, High Performance, VLSI, Carry Look-ahead Adder

1. INTRODUCTION

Multiplication is the basic arithmetic operations. In DSP (digital signal processing) a lot of arithmetic operations require the use of multiplications. The performance of three dimensional computer graphics mostly depends on the performance of multiplications. Therefore, there has been much work on advanced multiplication algorithms and design also. Critical factors in the design of multipliers are chip area and speed of multiplication. There is highly demand of high-speed multiplications and require less hardware. The performance of multiplier is affected by the multiplication strategy and type of the multiplier used.[1]

There are steps in multiplication. In first step, the partial products are generated. In second step, the partial products are reducing to one row of sum and one row of carries. In third step, the sum and carries are added to generate the final result. In some multiplier used in first steps Modified Booth Encoding to cut the number of partial product rows in half. Then apply some scheme, such as Wallace trees or compressor trees, in the second step to reduce the number of partial product rows to the final sums and carries. In third step, some adder used such as carry-look ahead or carry-select adder, to add the final two rows. [2]

For fast three dimensional computer graphics, high-speed floating point processing, the multiplier units are incorporated in DSP. For high speed, the Wallace tree multiplier architecture used. Sometimes it used with Booth recoding techniques for high speed. Because it's non regularities, the layout of Wallace tree multipliers take a lot of wasted area. The enhanced speed leads to increased power consumption. Thus, power saving architecture need for the future. Hence for high performance reducing the power dissipation of multipliers without compromising the speed and performance. Portion multipliers are employed for high speed and performance. In portions multipliers, the entire multiplication operation is decomposed into 4x4 or 8x8 multiplication module. The sub product bits are obtained in parallel from the 4x4 or 8x8 multiplication module. The efficiency of the NxN multiplication is dependent on the performance of the smaller multipliers [2]. The 8x8 reconfigurable Wallace Tree Multipliers are designed since Wallace tree are efficient in terms of power without increase in delay and area. The performance of Wallace tree improves at the operand with higher than 4. The multiplier computation is hierarchically divided into levels, saving a huge amount of power. The 8x8 Wallace tree architecture through hierarchical computation implement which is more efficient than conventional Wallace logic.

2. ARCHITECTURE

Algorithm presented for fast multiplication in two's complement representation. Indeed, the approach focuses on reducing the number of partial product rows .Having less number of partial product rows; the reduction tree can be smaller and faster in speed. This influences the speed of the multiplication, before applying partial products reduction techniques. Fewer partial products rows are produced, hence decreasing the overall operation time. The results

are a true diamond-shape for the partial product tree which is more efficient in terms of implementation which is shown in Figure 1. To achieve fast multiplication two's complement representation algorithm is used. The aim of this algorithm is reducing the number of partial product row. This directly influences the speed of the multiplication. Fewer partial products rows are produced, thereby lowering the overall operation time.

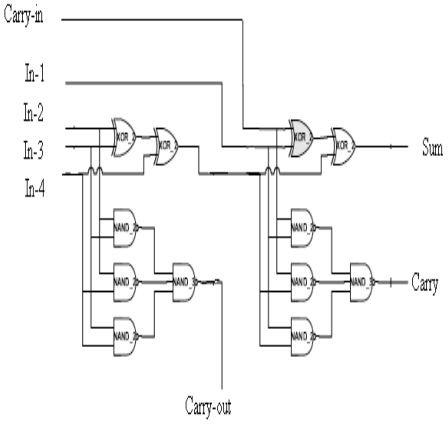

Figure 1: compressor schematic diagrams

The Modified Booth Encoding (MBE) is used for the first step because it cut the number of partial products rows in half. This prevent the extra partial product row, and this save the time of one additional carry save adding stage and the hardware required for the additional carry save adding.

2.1. Low Power Hierarchal Multiplier

8x8 bit multiplier architecture based on Wallace Tree, which is efficient in terms of power and regularity without increase in delay and area. The idea involves the generation of partial products in parallel using AND gates .The addition of partial products is done using Wallace tree, which is hierarchal, divided into levels [1]. There will be a reduction in the power consumption, since power is provided only to the level that is involved in computation. To improve the speed of addition at the third level of computation, a novel carry look-ahead adder (CLA) is proposed. The 8x8 bit size is chosen since Wallace Tree gets its performance improvement at the operand width higher than four do.

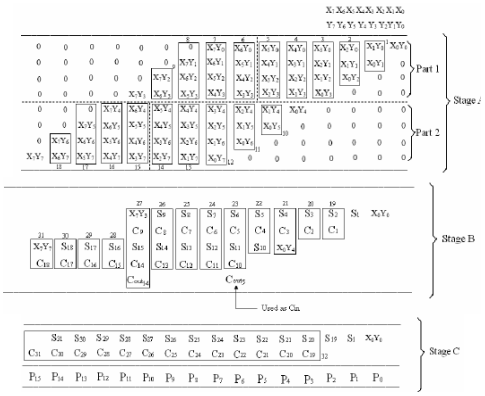

Figure 2: Modified Tree Logic Having Hierarchical Decomposition

2.2 Multi-Precision Booth Multipliers

The 8x8 bit Booth multiplier unit is cascaded together to form a 16x16 bit Booth multiplier shown in Figure 3. Following the same approach an 8nx8n Booth multiplier can be built. The Booth multiplier operates on two's complement signed numbers. A sign extension circuit is required to manipulate the most significant bits of each row.

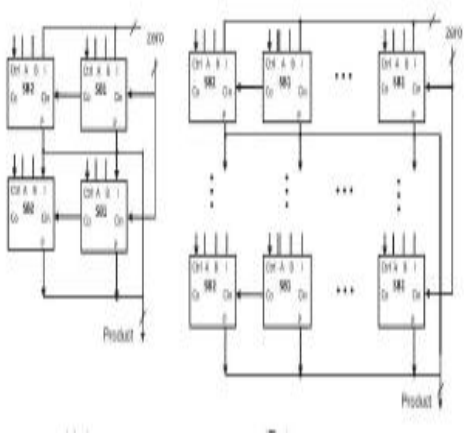

Figure 3: Multi-precision Booth Multiplier

The concept of the reconfigurable multiplier relies heavily on the reconfigurability of the partial product addition (CPA). The Booth algorithm reduces the partial products from 8 rows of 8-bit to 4 rows of 9-bit.

3. IMPLEMENTATION AND RESULT3.1.

3.1 4-2 Compressor: Schematic of 4:2 compressors

The conventional 4-2 compressor structure actually compresses five partial product bits into three. The architecture can be implemented with two stages of full adder (FA) connected in series shown Figure 4.

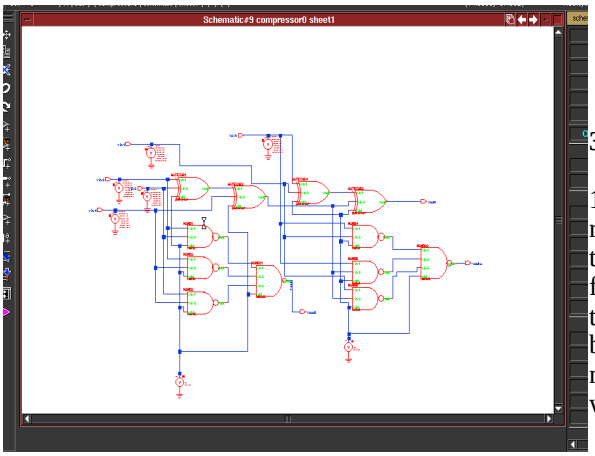

Figure 4: Schematic of 4:2 compressors

Input output waveform of conventional 4-2 compressor is shown in Figure 5 and 6 respectively.

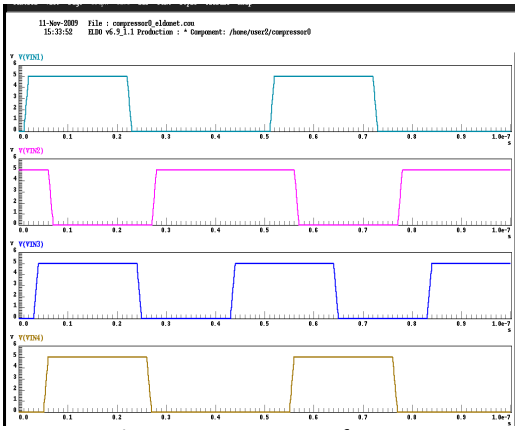

Figure 5: Input wave form

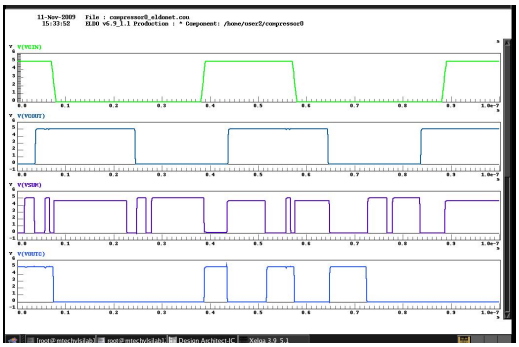

Figure 6: Output wave form

3.2. 16-Bit CLA :

16-Bit CLA shown in Figure 7. Which is required for multiplier module and then generate the symbol .After that we designed half adder, full adder, 4:2 compressor, 5:2 compressors and then we used modified full adder for making 4-bit carry look-ahead adder. Then Used 4-bit CLA make 8-bit CLA and then design 16-bit CLA which is used in final addition in multiplier.

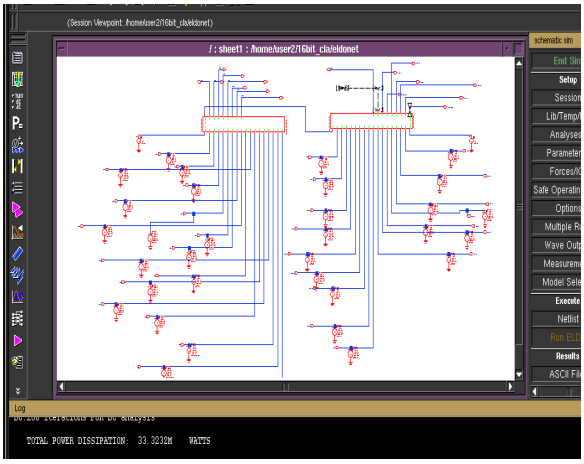

Figure 7: Schematic of 16-Bit CLA

3.3. 8x8Wallace Tree Multiplier structure

8x8Wallace Tree Multiplier structure shown in Figure 8.

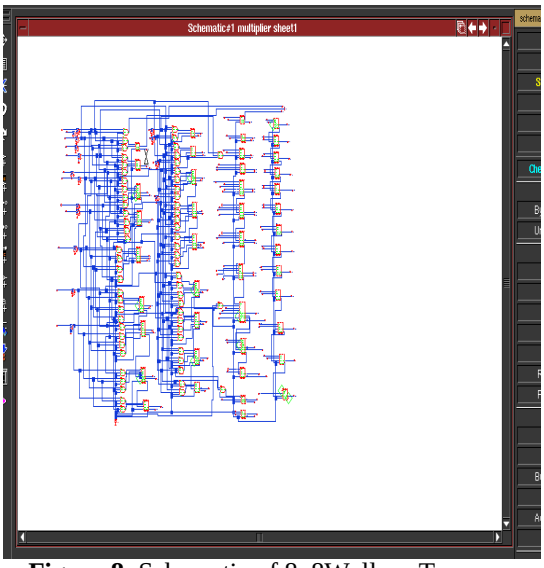

Figure 8: Schematic of 8x8Wallace Tree Multiplier

4. CONCLUSION

The reconfigurable Wallace tree is designed for improving the speed and regularity of the conventional Wallace tree multiplier. The Wallace tree multiplier has a number of advantages compared to the conventional Wallace tree multiplier. A carry look-ahead adder is used which has very less area. This reconfigurable Wallace tree multiplier is hierarchically divided into blocks; the blocks can be appropriately manually placed during routing. For this reason it leads to significant saving of the dead area in the chip. The regularity in configurable Wallace architecture will significantly help in reduction of interconnection capacitance problem found in higher width multiplier implemented with conventional Wallace tree logic. This multiplier can be multiply 4-bit and 8-bit.

REFERENCES

1. Himanshu Thapliyal, Neela Gopi, K. K Pavan Kumar and M. B Srinivas, **Low Power Hierarchical Multiplier and Carry Look-Ahead Architecture**, in proceedings International Conference on Signal Processing, ICSP 2004, Turkey, Dec 2004.

2. Jung-Yup Kang and Jean-Luc Gaudiot, **A Fast and Well-Structured Multiplier**, Proceedings of the EUROMICRO Systems on Digital System Design (DSD'04)

3. Oliver A. Pfänder, Reinhard Nopper, Hans-Jörg Pfleiderer, Shun Zhou and Amine Bermak. **Configurable Blocks for Multi-Precision Multiplication**, 4th IEEE International Symposium on Electronic Design, Test & Applications.

4. Jan. M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic. **Digital Integrated Circuits A Design Perspective**, Prentice-Hall of India Pvt Ltd, New Delhi, 2004.

5. A. Dandapat, S. Ghosal, P. Sarkar and D. Mukhopadhyay. **A 1.2-ns16×16-Bit Binary Multiplier Using High Speed Compressors**, International Journal of Electrical, Computer, and Systems Engineering DOI 10.1109/DELTA.2008, pp.109.

6. Siraram Vangal et.al. **A 5GHz Floating Point Multiply-Accumulator in 90nm Dual Vt CMOS**,,ISSCC 2003.

7. Robert Montoye et.al. **A Double Precision Floating Point Multiply**, ISSCC 2003.

8. Niichi Itoh, Yuka Naemura, Hiroshi Makino and Yasunobu Nakase. **A Compact 54x54 Multiplier with Improved Wallace-Tree Structure**, 1999 Symposium on VLSI Circuits Digest of Technical Papers.

9. Pascal C.H. Meier, Rob A. Rutenbar, L and Richard Carley. **Exploring Multiplier Architecture and Layout for Low Power**, IEEE 1996 Custom Integrated Circuits Conference.

10. S. Shah, A.J. Al-Khalili and D. Al-Khalili. **Comparison of 32-bit Multipliers for Various Performance Measures**, The 12th International Conference on Microelectronics, Tehran.