ISSN 2347 - 3983
Volume 8. No. 9, September 2020
International Journal of Emerging Trends in Engineering Research
Available Online at http://www.warse.org/IJETER/static/pdf/file/ijeter97892020.pdf
https://doi.org/10.30534/ijeter/2020/97892020

Features of the Formation of Impurity-Defective Centers in Silicon Doped with Chromium

Sharifa Bekmuradovna Utamuradova[1], Shakhrukh Khojakbarovich Daliev[2], Yuldoshali Ruzimuradovich Ravshanov[3], Kakhramon Makhmudjanovich Fayzullaev[4]

[1]Institute of Semiconductor Physics and Microelectronics at the National University of Uzbekistan, 100057, Tashkent, Uzbekistan. E-mail: sh-utamuradova@yandex.ru.

[2]Institute of Semiconductor Physics and Microelectronics at the National University of Uzbekistan, 100057, Tashkent, Uzbekistan. E-mail: shakhrukhd@mail.ru.

[3]Institute of Semiconductor Physics and Microelectronics at the National University of Uzbekistan, 100057, Tashkent, Uzbekistan.

[4]Institute of Semiconductor Physics and Microelectronics at the National University of Uzbekistan, 100057, Tashkent, Uzbekistan. E-mail: qahramon_fayz@mail.ru

ABSTRACT

In this work, the processes of the formation of impurity-defect centers in silicon doped with chromium are investigated. It was found that the diffusion introduction of Cr impurity into n-Si leads to the formation of three deep levels with fixed ionization energies: E_C–0.21 eV, E_C-0.41 eV, and E_C-0.51 eV, and in p-Si - two levels E_V+0.20 eV, E_V+0.41 eV. It is shown that only the levels E_C-0.41 eV and E_C-0.51 eV, E_V+0.20 eV are associated with chromium atoms in silicon. It was found that the Cr atoms introduced into Si during its growth are electrically neutral. It is shown that high-temperature treatment (HTT) in the range 1000÷1200°C of n-Si<Cr> samples leads to activation of Cr atoms.

Key words : Alloying, chromium, deep level, formation efficiency, impurity, impurity-defect center, silicon.

1. INTRODUCTION

It is known that the technological route of manufacturing practically any semiconductor device is accompanied by various cycles of low and high temperature treatments, which inevitably leads to the formation of various kinds of defects. Such treatments have a significant effect on the development of the defect structure of silicon and the formation of impurity-defect centers formed by impurities introduced in order to modify the properties of semiconductor materials (increase photosensitivity, strain sensitivity, change in resistivity, etc.) [1]-[6].

In addition, the presence of technological impurities plays an important role in the development of the defect structure of Si. Uncontrolled impurity atoms (iron, copper, etc.) that enter the bulk of silicon during the growth process and during technological treatments create electrically active and inactive defect states in the lattice. Technological impurities in Si always interact with dopant impurity atoms. Therefore, a change in the state of these impurities in the crystal lattice during heat treatment leads to the development of a defect structure of silicon, and also determines the efficiency of the formation of various defects [7]-[9].

Among the impurities of transition elements in silicon, chromium is the least studied impurity and there is no unambiguous opinion about the deep centers created by Cr in Si and about the behavior of its atoms in the silicon lattice. Thus, according to the data of the authors of [10], deep levels (DL) of E_V+0.21 eV, E_V+0.33 eV are associated with Cr atoms in Si, the authors of [11], [12] give a different DL spectrum for Cr: E_C-0.41 eV and E_V+0.21 eV. It should be noted that the capture cross sections for these DL differ from different authors by more than two orders of magnitude.

2. MATERIALS AND METHODS

In order to study the features of the formation of impurity-defect centers created by Cr atoms in silicon, we studied the properties of silicon doped both by diffusion and in the process of growing crystals from a melt using non-stationary capacitive deep-level spectroscopy (DLTS) and photocapacity (PC). Additional experiments were conducted using neutron activation analysis (NAA).

Monocrystalline silicon of n- and p-type conductivity with a specific resistance ρ_{out}=0.3÷40 Ohm·cm was used as the initial samples. Diffusion of Cr atoms in both n-Si and p-Si was carried out from the deposited layer of metallic impurity in the temperature range 1000÷1200 °C for 0.5÷2 hours,

followed by cooling at different rates.

For the experiments, we also used samples of silicon doped with chromium in the process of growing crystals from the melt, with a resistivity ρ=10÷100 Ohm·cm.

For capacitive measurements, Schottky barriers were created by depositing gold on n-Si and antimony on p-Si in a vacuum. Nickel was chemically deposited as an ohmic contact, and sometimes antimony or aluminum was deposited. The DLTS spectra were measured in the modes of constant capacitance [13] and constant voltage [14], and measurements of the PC spectra were carried out according to the usual methods described in [15].

3.EXPERIMENTAL RESULTS

Measurements of DLTS spectra showed that after diffusion introduction of Cr in n-Si <Cr> samples (Fig. 1) deep levels are formed with fixed ionization energies and charge carrier capture cross sections: E_C–0.21 eV, $\sigma_n=2\cdot10^{-15}$cm^2 (peak A), E_C–0.41 eV, $\sigma_n=6\cdot10^{-16}$ cm^2 (peak B) and E_C–0.51 eV, $\sigma_n=1\cdot10^{-16}$ cm^2 (peak C), and in p-Si<Cr > DL are observed E_V+0.20 eV, $\sigma_P=7\cdot10^{-15}$ cm^2 (peak L) and E_V+0.41 eV, $\sigma_P=3\cdot10^{-15}$ cm^2 (peak M). In the control heat-treated samples (without Cr), deep levels E_C–0.21 eV (peak A') and E_V+0.41 eV (peak M') are also observed, and their concentration in Si <Cr>$_{diff.}$ much lower. These results allow us to conclude that only the efficiency of formation of levels E_C–0.41 eV, E_C–0.51 eV, and E_V+0.20 eV depends on technological modes (diffusion temperature T_{diff} and cooling rate υ_{cool}) their concentrations increase with increasing T_{diff} and υ_{cool}.

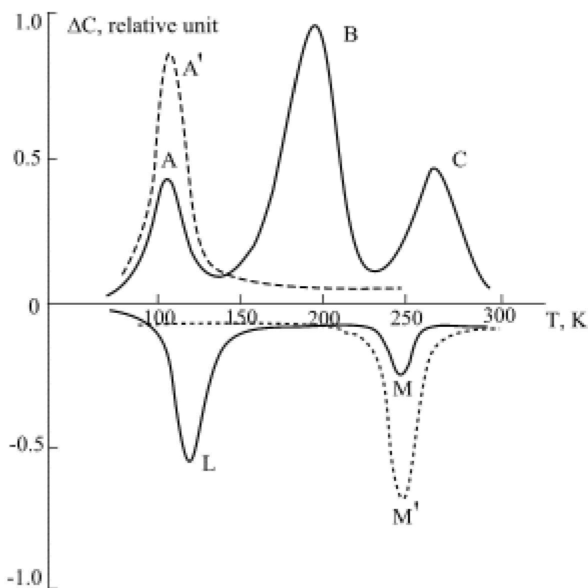

Figure 1: DLTS spectra of Si <Cr> samples

In the samples of n-Si diffusion doped with chromium, the photocapacity spectra were also measured, in which the relaxation of the capacitance is observed near hν~0.21 eV, hν~0.41 eV, and hν~0.51 eV (Fig. 2, curve 1). An analysis of these spectra shows that the observed relaxations are due to the charge exchange of three deep centers: E_C–0.21 eV, E_C–0.41 eV and E_C–0.51 eV. In the spectra of the induced PC of these samples, two steps are observed near hν~0.20 eV and hν~0.41 eV (Fig. 2, curve 2), caused by level exchange in the lower half of the band gap: E_V+0.20 eV and E_V+0.41 eV. Analysis of the DLTS and PC spectra shows that the thermal and optical activation energies of the detected levels in the n-Si<Cr> samples coincide within the measurement error.

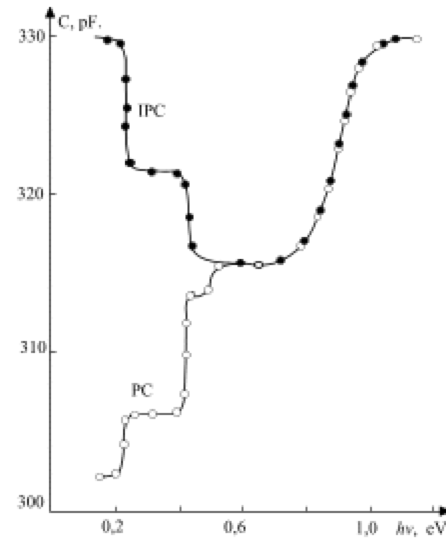

Figure 2: Spectra of PC (1) and IPC (2) of Si <Cr> samples

Measurements of the DLTS spectra of chromium-doped silicon samples during the growth of silicon from the melt showed that no deep levels are observed in significant concentrations, although according to the NAA data the total concentration of Cr atoms in the bulk of silicon was about $4\cdot10^{15}$ cm^{-3}. Hence, it can be concluded that chromium atoms introduced into silicon during the growth process do not exhibit electrical activity.

In order to test the possibility of activating chromium atoms in such samples, experiments were carried out with high-temperature treatment of n-Si<Cr> samples grown in the temperature range T = 900-1200 °C followed by rapid cooling. The n-Si<Cr> plates were thoroughly washed with acid-peroxide prior to heat treatment. Annealing was carried out in quartz boats in a tube in air.

Figure 3 shows the DLTS spectrum of a silicon sample doped with chromium during growth and subjected to high-temperature treatment at 1100^{0}C (curve 1) and 1200^{0}C (curve 2) for 1 hour, followed by cutting quenching.

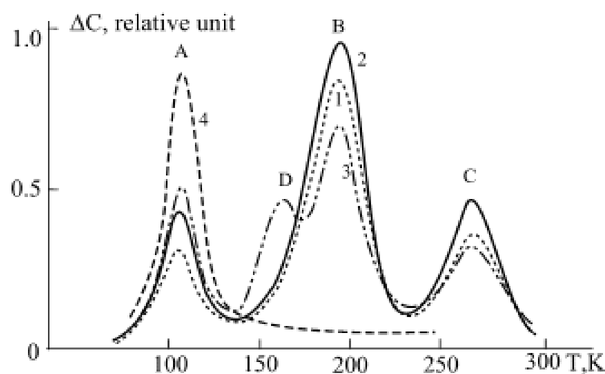

Figure 3: Typical DLTS spectra of n-Si<Cr> samples grown after heat treatment at 1100⁰C (1), 1200⁰C (2), 1200⁰C with insufficient purification (3) and control n-Si (4)

The spectra were measured in the constant voltage mode by a single scan [13]-[15]. Analysis of the measured DLTS spectra shows that high-temperature treatment of n-Si<Cr> samples leads to the formation of three levels with ionization energies E_C–0.21 eV, E_C-0.41 eV, and E_C-0.51 eV. The E_C–0.21 eV level is also observed in the control heat-treated samples (without Cr impurity); its parameters coincide with the parameters of known heat-treatment defects with the E_C–0.21 eV level (peak A) [16].

The deep levels E_C-0.41 eV and E_C-0.51 eV are probably due to the activation of Cr atoms; we observed similar levels above during diffusion doping of silicon with a chromium impurity. Note that the concentrations of the observed DLs increase with an increase in the heat treatment temperature.

An analysis of the measured DLTS spectra shows that in some samples, insufficient cleaning of the surface of n-Si<Cr> samples before high-temperature treatment leads to the appearance of a new deep center with a level of E_C-0.30 eV (peak D) in a noticeable concentration. Comparison of the DLTS spectra of such samples heat-treated in the range 900 ÷ 1200⁰C (Fig. 1, curve 3, peaks D and B) showed that the efficiency of formation of the E_C-0.30 eV level depends on the processing temperature and the degree of surface cleaning before high-temperature treatment. It was found that the appearance of this level occurs synchronously with the annealing of the E_C-0.41 eV level (Fig. 1, curves 2 and 3, peak B).

4. DISCUSSION

Measurements of DLTS spectra have shown that additional low-temperature treatment at T = 100-400⁰C of n-Si<Cr> samples that have undergone preliminary HTT at 1200⁰C leads to transformation of the energy spectrum of deep levels. As can be seen from Fig. 4 (curve 3, peak B), the concentration of the E_C-0.30 eV level, stimulated by high-temperature treatment, as a result of low-temperature treatment at 250⁰C for 1 hour, noticeably decreases and with a further increase in the duration of treatment, it is completely annealed.

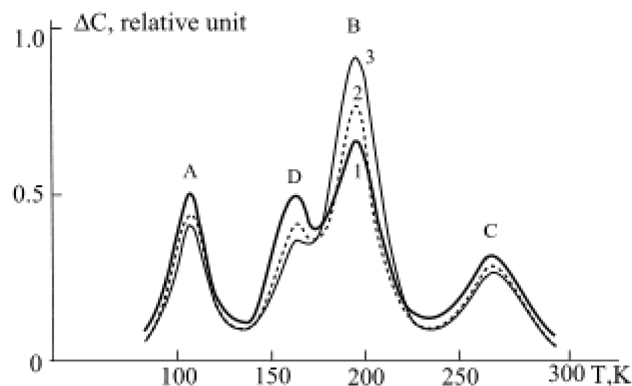

Figure 4: Typical DLTS spectra of n-Si samples doped with chromium during growth after heat treatment at 1200⁰C (1), after additional heat treatment at 250⁰C, 1 h. (2) and 250⁰C, 2 h. (3)

Analysis of the DLTS spectra showed that annealing of the E_C-0.30 eV level is accompanied by an increase in the concentration of E_C-0.41 eV levels ($\Delta N_{Ec\text{-}0.30} \approx \Delta N_{Ec\text{-}0.41}$).

The parameters of the E_C-0.30 eV level and the change in its concentration during heat treatment are similar to the behavior of the Fe-Au complex, which was reported in [17]. An additional argument in favor of identifying a center with a level of E_C-0.30 eV as a Fe-Cr complex may also be the fact that the efficiency of its formation depends on the temperature and degree of purification of the samples before high-temperature treatment. It is very likely that the source of Fe is an insufficiently cleaned surface of n-Si<Cr> samples before heat treatment. It is also possible that Fe atoms got into silicon during the growth process and, upon subsequent slow cooling, passed into an inactive state, and high-temperature treatment at 1200 °C activated these atoms, which may be responsible for the formation of DL E_C-0.30 eV. The assumption about the connection of this DL with the Fe-Cr impurity pair is also supported by synchronous changes in the concentration of levels Ec-0.41 eV: these changes are almost equal and opposite to the changes in the concentration of DL E_C-0.30 eV.

5. CONCLUSION

Thus, when studying the processes of the formation of impurity-defect centers in silicon doped with chromium, it was found that the diffusion introduction of a chromium impurity into n-Si leads to the formation of three deep levels with fixed ionization energies: E_C–0.21 eV, E_C-0.41 eV, and E_C-0.51 eV, and in p-Si - two levels E_V+0.20 eV E_V+0.41 eV. It was found that only the levels E_C-0.41 eV and E_C-0.51 eV, E_V+0.20 eV are associated with chromium atoms in silicon.

It was found that chromium atoms introduced into silicon during its growth are electrically neutral. Analysis of the results obtained shows that high-temperature treatment in the range 900–1200 °C with subsequent quenching of silicon samples doped with chromium during growth leads to the

activation of chromium atoms with the formation of deep levels E_C-0.41 eV and E_C-0.51 eV. In the n-Si <Cr> samples, a new level E_C-0.30 eV is also observed, which is characterized by thermal instability and its formation or annealing is accompanied by synchronous changes in the concentration of the chromium level.

REFERENCES

1. N.N.Gerasimenko. ***Silicon - material of nanoelectronics,*** Moscow, Technosphere, 2007, p.351.
2. Y. Rodionov. ***Technological processes in micro- and nanoelectronics,*** Moscow, 2019, p.352.
3. V.A. Gurtov. ***Solid state electronics,*** Moscow, Technosphere, 2005, p..406.
4. Sh. B. Utamuradova, Kh. S. Daliev, Sh. Kh. Daliev, and K. M. Fayzullaev, **The influence of chromium and iron atoms on the processes of defect formation in silicon,** *Applied Physics*, Vo. 6, 90 (2019).
5. Sh. Utamuradova, S. Nasriddinov, Sh. Ismoilov. **Electrophysical Properties of Silicon doped by Nickel impurity using Diffusion method.** *International Journal of Emerging Trends in Engineering Research (IJETER),* 2020, Vol 8, No 7, pp 3513- 3518.
6. Ragavi. R, Papanasam Esakki. **Profound Understanding of Various Annealing Scheme Effects on the Electrical Characteristics of Silicon Carbide based Devices.** *Intermational Journal of Emerging Trends in Engineering Research (IJETER),* 2020, Vol 8, No 7, pp 3513- 3518.
7. K. Ravey. ***Defects and impurities in semiconductor silicon***, M., Mir, 1984, p. 471.
8. V.I.Fistul. ***Physics and Materials Science of Semiconductors with Deep Levels,*** Moscow., 1987, p. 232.
9. V.V. Emtsev, T.V. Mashovets. ***Impurities and point defects in semiconductors.*** M., Radio and communication, 1981, p. 248.
10. L. Milnes. ***Impurities with deep levels in semiconductors.*** - M., Mir, 1977, p.547.
11. E.M. Omelyanovskiy. ***Transition metal impurities in semiconductors.*** Moscow, 1983, p.192.
12. Rohatgi A., Davis I. R., Hopkins R. H. and Mullin P.G.Mc. Sol.St. El. 1983, V. 26, P. 1039-1048.
13. D.V. Lang. **Deep level transient spectroscopy A new method to characterize traps in semiconductors.** *Journal of Applied Physics.* 1974. Vol. 45. No. 7, p. 3023-3032.
14. G.L.Miller, D.V. Lang, L.C. Kimerling. **Capacitance transient spectroscopy,** *Ann. Rev. Mater. Sci.* 1977, v. 7, p. 377-448.
15. L.S. Berman, A.A. Lebedev. ***Capacitive spectroscopy of deep centers in semiconductors.*** L., Nauka, 1981, p.170.
16. Kh. S. Daliev. **Spectroscopy of Defects in Semiconductors Doped Nickel.** *Journal of Scientific and Engineering Research*, 2017, 4 (5), p. 211-215.
17. S.D. Brotherton, P. Bradley, E.R. Weber. **Electrical observation of the Au-Fe complex in silicon,** - *Journal of Applied Physics.*, 1984, v. 55, no. 4, p. 952-956.