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Simulation Study of Memristor-Based Digital Logic Circuit using Stateful Logic

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ABSTRACT

Computer technology consists of three basic block of logic gate, which is NOT, AND, and OR gate. When apply memristor into logic gate, a new logic operation needs to be introduced, called material implication, IMPLY. This study is an attempt to investigate performance of memristor using LT SPICE model with Boilek and Prodromakis window function. We incorporate the SPICE model of memristor to simulate the IMPLY stateful logic circuit. As a result, Biolek memristor switching performance is 35ms faster than Prodromakis memristor at 1.2V while both recorded highest percentage of correct output at 4Hz with similar time taken of 1s. As a conclusion, both Biolek and Pedromakis windows function simulation and transient analysis showed the characteristics of the memristor, but the current step size remained a constraint for further performance review.

Key words : memristor, non-linear drift, stateful logic, Biolek, Pedromakis

1. INTRODUCTION

Memristor is only an idea proposed by Leon Chua on 1971 which stated that there is fourth passive circuit element that yet fabricated called memristor which stand for memory and resistor provides a relation between charge, q and flux, Φ [1]. Basically, the component is described as two-terminal in which function of flux between two terminals is a sum of electric charge that has passed through the device [2]. It also known to be flux-controlled when the interaction between flux and charge is expressed as function of the flux linkage. This property is quite similar to fundamental circuit element resistor but memristor is described as variable resistor which is depend on duration, magnitude and direction when voltage is applied across its terminal. Memristor behavior also present in the battery, however battery is an active element which memristor is otherwise.

Fundamentally, memristor property is called memristance, when charge is flow through it in a direction, the device resistance decreases, when charge flow in reverse direction, resistance increases in the circuit. If the source is turn off, memristor remember it last resistance state it had [3]. This basic resistance effect for the memristor is describe in Figure 1.

Figure 1: Memristive device symbol.

As depicted in Figure 1, the resistance of the device decreases when current enter left side of the device, and resistance device increases when current flows out of the device. The thick black line represents the polarity of the device.

In 2008, Leon Chua's idea has been realized by one of the teams from the HP lab. They have fabricated the memristor model by using a thin film of Titanium Dioxide (TiO2) and connect two Platinum (Pt) contact at both ends [2]-[10].

Numerous of research has been conducted from the date until today which covered various spectrum of research including simulation, fabrication, and material. Although significant development of the technology growth, the simulation of the memristor using stateful logic is still new. Therefore, in this study, we are using Nonlinear ion Drift memristor model provided by [4], [5], [11] with p =10 and the simulation was conducted using LTSPICE software to determine performance including the limit of model in executing and simulating IMPLY logic circuit.

In this paper, the overview and technology gap are highlighted in the introduction part. As to provide a clear flow of study, recent memristor technology included in section II. Section III addressed the complete methodology used in this performance evaluation via simulation study. The result obtained is highlighted in specific section IV. The finding is summarized in the last section of this article.

2. RECENT MEMRISTOR TECHNOLOGY

This thin film of Titanium Dioxide (TiO2) consist of 2 different layers; one layer has oxygen vacancy denoted as (TiO2-x), and the other layer doped with oxygen dioxide (TiO2). Where x is representing the number of oxygen vacancies and cannot be equalled to 2 and 0. The idea is to make the TiO2-x region has a positive ion in the device; to obtain memristive behavior. The Titanium with oxygen vacancies are positively charged ion; behave conductively while other layer is the resistance component when the memristor is off. In this layer, Titanium is doped with oxygen which is pure Titanium Dioxide (TiO2) to act as resistance or insulating properties to the memristor; and to reduce Titanium behavior as a conductor [5]. The memristor model and simplified diagram is shown Figure 2(a) and Figure 2(b).

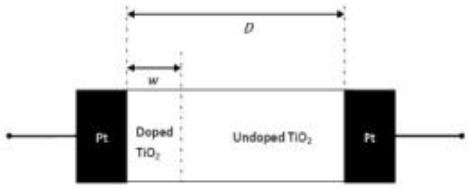


Figure 2(a): Memristor model developed at HP lab

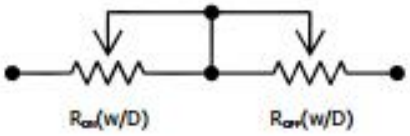


Figure 2(b): Simplified diagram of linear ion drift memristor [5]

As depicted in Figure 2(a) and Figure 2(b), the working principles of a memristor depend on the length of time voltage supplied, the magnitude of the supplied voltage, and the polarity of the supplied voltage. Basically, the conductivity of the whole device increases when the positive voltage applied. Specifically, the positively charged ion Titanium which has oxygen vacancies in the TiO2-x layer moving the boundary towards the pure TiO2 layer and increasing its area while decreasing pure TiO2 layer area. As a result, the conductivity of the TiO2-x layer increase when the negative voltage is applied.

Moreover, the TiO2-x positively charged oxygen vacancies will contract, move in direction of doped TiO2-x layer. This result in increasing the amount of insulating TiO2. When supply voltage is turned off, the oxygen vacancies do not move and boundary between two titanium dioxide layers is preserved. This is how memristor traces the voltage last applied [5].

There are several memristor model have been discovered in the [12], [13], [14] and [15]. In this paper, we will highlight four of the models which associated and related to this study.

2.1 Linear Ion Drift Model

Linear Ion Drift Model is the simplest representation of memristor which model after Titanium Oxide (TiO2) created by HP Lab as reported in [1] and [5]. The model consists of doped region of TiO2-x and undoped region consist of TiO2. Switching mechanism for this model is current. Moreover, this model has accuracy issue related to the boundary of the device and behave slightly distinct to physical device.

2.2 Simmons Tunnel Barrier Model

Simmon Tunnel Barrier Model [13] depicted as different physical memristor model to Nonlinear ion Drift. Moreover, this model consists of a resistor and an electron tunnel barrier in series and contradict with the Nonlinear ion Drift model which consist of 2 resistors in series [16], [17]. In consideration of nonlinear of memristor behavior, the parameters in this model forces upper and lower boundary of state variable x which x represent Simmon tunnel barrier width. Thus, window function for this model is not compulsory and the switching mechanism for this model is current.

2.3 Threshold adaptive Memristor (TEAM) Model

TEAM [12] model switching mechanism is based on current. For this model, the status variable is not change for current below a certain threshold value. Moreover, this model able to assimilate to the Simmon Tunnel Barrier model for purpose of analysis, simplification and efficiency in computation.

2.4 Nonlinear ion Drift Model

Recent study in [4] and [13] stated that behavior of Linear ion Drift model never reach both end of memristor for doped and undoped region boundary, and the drift of oxygen vacancies shows nonlinear behavior near both boundaries. To provide nonlinearity for boundary issue, window function is introduced. Window function, f(x) is a state variable. This function is to restrict and add nonlinear behavior close to the bound.

There are two famous window function: Biolek and Prodromakis which will be used in this study. In this project we implement Biolek and Prodromakis window function in the LT SPICE model to see the differences and only consider these two types of window function. Biolek proposed window function as,

$$f(x) = 1 - (x - stp(-i))^{2p} \quad (1)$$

This function allows reverse bias to move back the state

variable after its reach either boundary [4]. stp(i) is a current dependent step function that behaves differently depend on voltage direction. p is control parameter, which is a positive integer, this control parameter give linearity to the model as p value increases.

$$stp(i) = \begin{cases} 1 & pro \quad i \geq 0 \\ 0 & pro \quad i < 0 \end{cases} \tag{2}$$

On the other hand, window function proposed by Prodromakis is,

$$f(x) = 1 - [(x - 0.5)^2 + 0.75]^p \tag{3}$$

which in the Prodromakis window function, p value offers more flexibility and take any positive integer [11]. This window function also overcome terminal state problem where fmax (x) can take any value within 0 to 1, 0<fmax(x) <1. Contradict with the previous model, the switching mechanism for Nonlinear ion Drift Model is voltage.

3. METHODOLOGY

In this study, SPICE model was adapted from [5], and the adjustment was made to run and operate for Biolek and Prodromakis window function as shown in Figure 3.

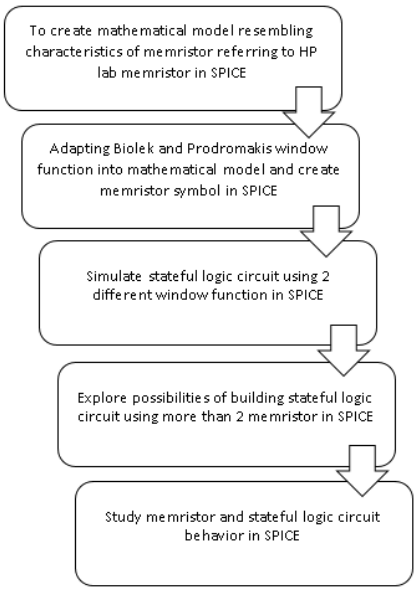


Figure 3: flow of the project

As depicted in Figure 3, the process starts with creating the mathematical model for resembling characteristic of memristor and followed by adapting the window function model in the developed mathematical model and creating symbol in SPICE. The complete stateful logic circuit using two different window function will be simulated in the fourth stage. Based on the result, the possibilities of building stateful logic circuit using more than 2 memristor in SPICE is explored. Last stage will investigate the memristor and stateful logic circuit behavior in SPICE. The detail methodology will be highlighted in the respective sub-section.

3.1 Proposed Nonlinear Drift memristor model

Memristor presented as thin semiconductor film consist of two region which is doped region and undoped region, place between them is platinum (Pt) plate function as electrode for the device [1]. Doped region contributes conductive part when device is ON state because present of Oxygen deficient Titanium Oxide (TiO2-x), thus contribute to low resistance in the device. Undoped region consist of pure titanium Dioxide (TiO2) which has high resistance and behave like insulator, take effect when device is OFF state.

Region with lowest resistance represent R_{ON} while region with highest resistance is R_{OFF}. w is width of doped region and *D* ,is total length of TiO_2 layer [4]. The total resistance of the memristor represent as, RMEM, which define as

$$R_{MEM} = R_{ON}x + R_{OFF}(1 - x) \tag{4}$$

$$Where \qquad x = \frac{w}{D} \in (0.1) \tag{5}$$

In equation (4) and (5), x represents as boundary between doped and undoped region with condition limit w is between 0 and D. Then, relation between memristor voltage and current from Ohm's Law,

$$v(t) = R_{MEM}(x)\, i(t) \tag{6}$$

In equation (4) and (6) notice that R_{MEM} value is determined by value of *x*. When external voltage bias applied, the voltage will cause ion charged to drift. Therefore,

$$v(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) i(t) \tag{7}$$

the memristor is modelled as two series connected resistor, linear ion drift is assumed in uniform field and ions have similar average ion mobility denoted as, μ_v .From,

$$\frac{dw}{dt} = f(w, i) \tag{8}$$

where *f* explicit of time and *w* is a set of state variable and current with respect to the time, respectively. Moreover,

$$\frac{dw}{dt} = \mu_v \frac{R_{ON}}{D} i(t) \tag{9}$$

μ_v is average mobility of the charges. As in (7) and (9) yield the following equation for state variable *w*(*i*), which

$$w(t) = \mu_v \frac{R_{ON}}{D} q(t) \tag{10}$$

where *q*(*t*) is the total charge passing through the device. Inserting (10) into (7), neglect R_{ON} for condition $R_{ON} << R_{OFF}$, we obtain

$$M(q) = R_{OFF}\left(1 - \frac{\mu_v R_{ON}}{D^2} q(t)\right) \quad (11)$$

which $M(q)$ is the memristance of the system. The process is visualized as in Figure 4.

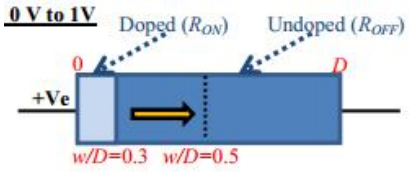


Figure 4(a)

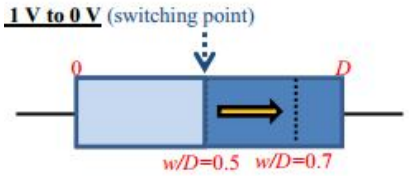


Figure 4(b)

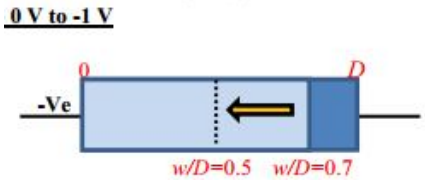


Figure 4(c)

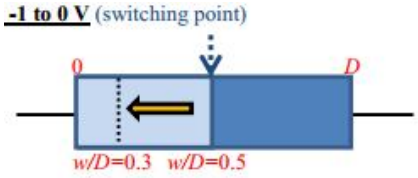


Figure 4(d)

As depicted in Figure 4 which is adapted from [13], the Fig 4(a) & Fig 4(b) ion boundary position moving toward undoped region when applied 0 to 1 volt and 1 to 0 volt, increasing doped TiO_2 length. Fig 4(c)& Fig 4(d) ion boundary position moving toward doped region when applied 0 to -1 volt and -1 to 0 volt, increasing undoped TiO_2 length.

Due to memristive behavior, small voltage changes in the device causing the ion boundary position to move towards non-linear ways. As to ensure nonlinear dopant drift within zero and unity, addition of window function, $f(x)$ is needed. As state variable drift speed approaches either boundaries, the window function decreases. There are several factors that control the speed of motion of the boundary between doped and undoped region. According to state equation from [5]

$$\frac{dx}{dt} = ki(t)f(x), \qquad k = \frac{\mu_v R_{ON}}{D^2} \quad (12)$$

where the speed of the boundary between doped and undoped region gradually decreases as approach to 0.

3.2 LT SPICE Memristor Subcircuit Model

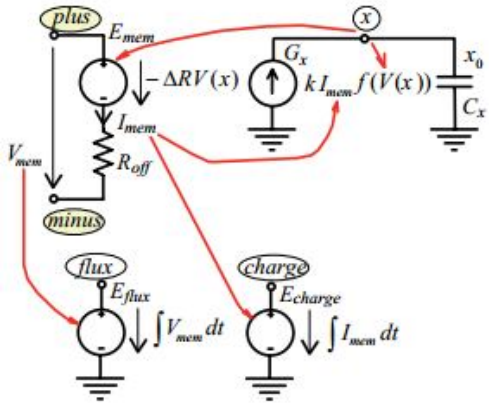


Figure 5: Structure of SPICE model from [5]

Simulation for the memristor model is according to sub circuit model proposed by [5] on Figure 5, where E_{mem} is connected in series with R_{OFF}. E_{mem} is a voltage source in which terminal voltage is controlled according to the formula *"-xΔR"* from modified (4), where $R_{MEM}(x)$ is defined as

$$R_{MEM}(x) = R_{OFF} - x\Delta R, \; R_{OFF} - R_{ON} \quad (13)$$

where x is representing normalized width of doped layer which model after voltage across capacitor C_x, the initial value of x depends on initial voltage across C_x. I_{mem} and V_{mem} modeled to be input voltage across and current through the memristor. Therefore, by integrating V_{mem} and I_{mem} calculation of flux and charge can be acquired.

The memristor model is based on mathematical equation discussed at the proposed Nonlinear Drift memristor model section, which the memristor model used the following parameter as in Table 1.

Parameter	Value
R_{ON}	100
R_{OFF}	16K
R_{INIT}	12K
D	10n
Uv	10F
P	10

Table 1: Parameter for memristor model

As stated in Table 1, both Biolek and Prodromakis memristor model used same mathematical model and parameter given in except for their own window function. Moreover, the memristor model was built using syntax command, which all parameter stated in Table 1 was used to develop the subcircuit model for both Biolek and Prodromakis memristor. Both symbols were created as shown in Figure 5.

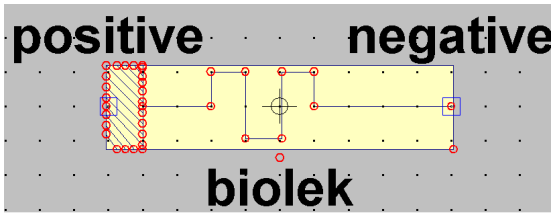


Figure 5(a): Memristor symbol for the Biolek window function

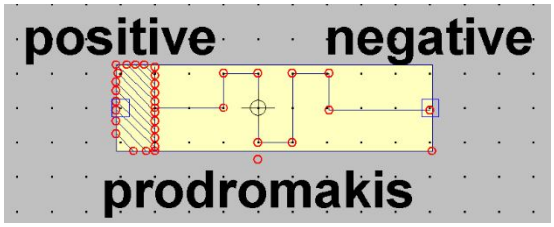


Figure 5(b): Memristor symbol for the Prodromakis window function.

Figure 5: memristor symbol for each window function.

As depicted in Figure 5, both SPICE symbol for the Biolek and Prodromakis window function were developed.

After the symbols created, both memristors were applied with sine input voltage with $2.4V_{p-p}$ with different range of frequency. As shown in Figure 6, both memristors exhibit memristance behavior which it is become more linear when a memristor is supplied with sinusoidal input voltage with high frequency. Moreover, the pinched hysteresis loop of memristor that represent Current-Voltage forming into a straight line as magnitude of frequency increases starting from 1Hz to 3 Hz were recorded in Figure 6(a) until Figure (d) for both of the Biolek and Prodromakis window function model.

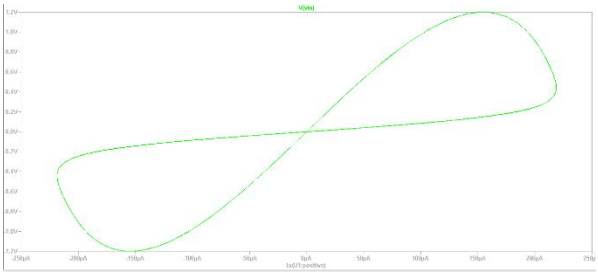


Figure 6 (a): Biolek memristor is supplied with sinusoidal input voltage with Frequency=1.

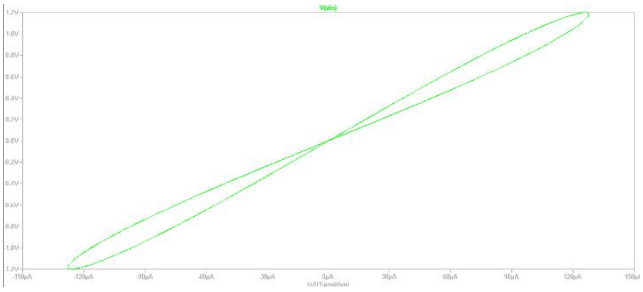


Figure 6 (b): Biolek memristor is supplied with sinusoidal input voltage with Frequency =2.

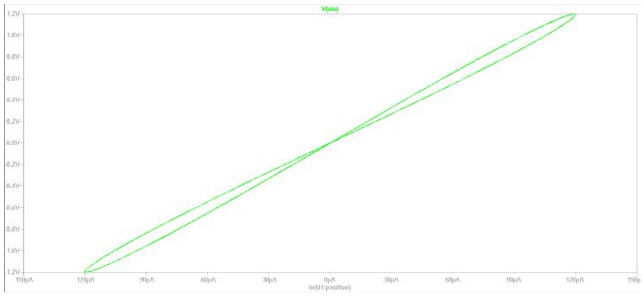


Figure 6 (c): Biolek memristor is supplied with sinusoidal input voltage with Frequency =3.

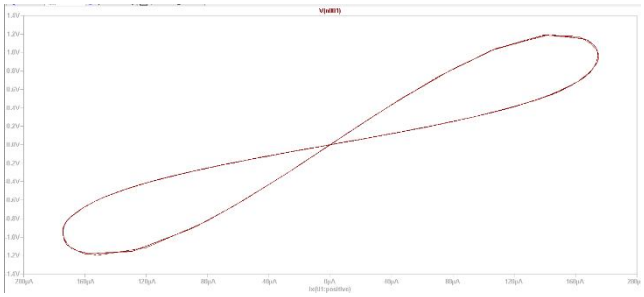


Figure 6 (d): Prodromakis memristor is supplied with sinusoidal input voltage with Frequency=1.

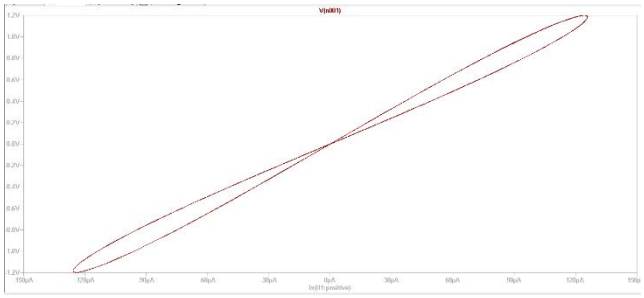


Figure 6 (e): Prodromakis memristor is supplied with sinusoidal input voltage with Frequency=2.

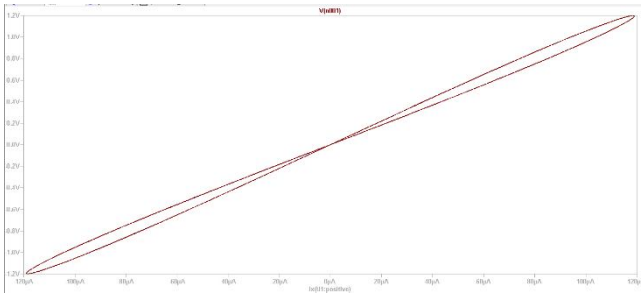


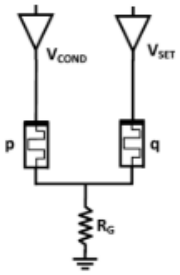
Figure 6 (f): Prodromakis memristor is supplied with sinusoidal input voltage with Frequency=3.

3.3 Stateful (IMPLY) Logic

Stateful logic refer to logic that capable of store information and perform logical operation, its only has 2 logic families which is MAGIC and IMPLY logic [3], [6], [9], 10]. In this study, the IMPLY was used for the implementation, which the

IMPLY logic provides a basic logic element for a memristor-based circuit.

The basic logic element for the IMPLY logic is shown in Figure 7.



Figur`e 7:

As depicted in Figure 7, R_G is connected to two memristor which will act as a load resistor where the R_G value must be in the range of $R_{ON} < R_G < R_{OFF.}$ Moreover, the memristor p and q will act as digital switches where each of the memristor having their own role and individual voltage are set in logic operation. Therefore, the value of R_G is

$$R_G = \sqrt{R_{ON} R_{OFF}} \qquad (14)$$

which the R_G value is depending on number of memristor in parallel as to ensure voltage of horizontal wire depend on conductance of the memristor.

The logic truth table for the IMPLY logic is stated in Table 2.

Table 2: IMPLY logic truth table

Case	*p*	*Q*	*p→q*
1	0	0	1
2	0	1	1
3	1	0	0
4	1	1	1

As tabulated in Table 2, the initial memristance of p and q are the input of the gate and the output of the gate is the final memristance of Q (logic state at q). p is applied with voltage condition, V_{COND} while q is applied with voltage set, V_{SET}. In this case, V_{SET} must has higher magnitude than V_{COND} which in range of $V_{COND} < V_{SET}$ and both values are fixed. Notice that for every initial value q tend to drift toward ON state.

In case 1, output memristance of Q is depend on write time of the circuit, when external voltage applied, output memristance Q will reduce for brief of time and this will affect the correct logical behavior. For case 2 and 4, initial logic state of q is one and the output also one, is come from magnitude voltage of V_{SET}. In case 3, when initial logic state of p is high and initial logic state of q is low, the output memristance Q is low remain unchanged and become lower than case 1.

For IMPLY logic simulation, both Biolek and Prodromakis memristors were connected with the same V_{SET} and V_{COND} with both respective value of *1.2V* and *0.12V*. R_G value for the IMPLY circuit is satisfy with (14) and the complete simulation connection were shown in Figure 8.

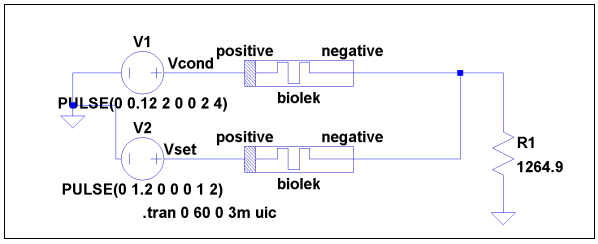


Figure 8(a): Circuit connection for IMPLY logic using Biolek memristor.

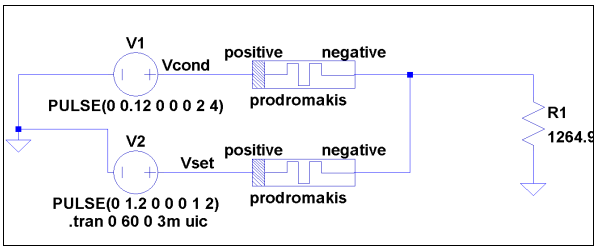


Figure 8(b): Circuit connection for IMPLY logic using Prodromakis memristor.

5. RESULT AND DISCUSSION

The IMPLY logic output pulse for Biolek and Prodromakis memristor is shown in Figure 9.

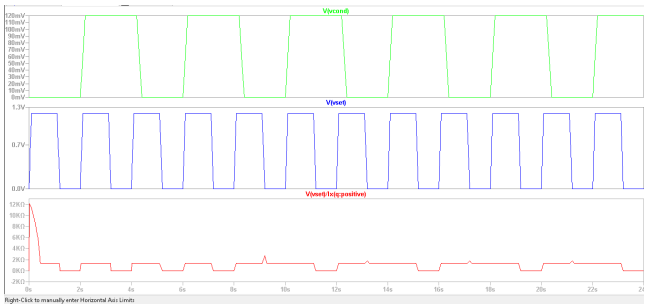


Figure 9(a): Output memristance for Biolek memristor IMPLY logic

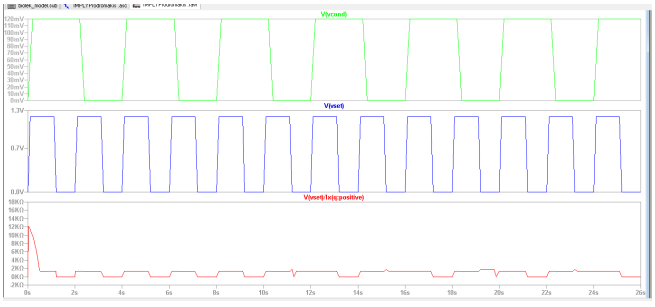


Figure 9(b): Output memristance for Prodromakis memristor IMPLY logic

As depicted in Figure 9, both were run in transient response in 60 seconds and needed initial external voltage to get correct logic behavior. The green pulse is a V_{COND} voltage, the blue pulse is V_{SET} voltage and red pulse is voltage output logic at memristor *q*. At 0 second both Biolek and Prodromakis memristor resistance is set to 12 kΩ as initial value.
At case 1 which is *p* and *q* is low, the memristance at *Q* is high or equal to high resistance, R_{OFF}. Case 1 is an indication that *q* reaches the desired state (correct logical behavior). Figure 9(a) and 9(b) is the output pulse of IMPLY logic for Biolek and Prodromakis memristor, both memristor follows the truth table at Table 2. Biolek memristor required 8.16 second to obtain correct logic behavior while for Prodromakis takes 10 seconds. In case for one minute, both Biolek and Prodromakis required 60% of the time for correct logic output obtained.

The influence of frequency in logic output was conducted by using series of difference frequency based on setup in Figure 8. The result is tabulated in Table 3.

Table 3: The table shows result of Biolek and Prodromakis memristor when applied different frequency.

Frequency (Hz)	Correct output percentage (%)		Time taken (second)	
	Biolek	Prodromakis	Biolek	Prodromakis
0.5	60	60	8	8
1	13.33	16	4	6
2	51.667	60	3	5
4	66.67	72.25	1	1
8	41.25	40	0.75	0.7

As stated in Table 3, both memristors given almost the same pattern of result for the series of frequency used. Both memristors recorded 60% of correct output for 0.5Hz frequency with similar time taken of 8 second. But, the highest percentage of correct output recorded at 4Hz frequency with Biolek at 66.67% and Prodromakis at 72.25% at similar time taken of 1 second. Both recorded the lowest percentage of correct output 1Hz with 13.33% and 16% respectively. Biolek memristor has less accurate logic behavior compared to Prodromakis except for the simulation at 8Hz frequency with 41.25% as compared to 40%. Moreover, the time taken for Prodromakis is faster than Biolek at 0.7s and 0.75s respectively at the same frequency.

As depicted in Figure 9 (a) and Figure 9 (b), the correct logic behavior is not consistent where the memristance *Q* is producing inaccurate logic output at certain point. The same issue happened during different frequencies simulation as recorded in Table 3. Although the logic gate speed is important for faster computational result, but the correct logic state behavior much more important. For the memristor model simulation, as the magnitude of input frequency getting higher, there is no consistency for correct logic state behavior produced.

Therefore, on the basis of a one-minute transient response simulation, Biolek produces less correct logic state behavior compared to Prodromakis. In terms of the switching speed from R_{OFF} to R_{ON}, Biolek memristor is faster than Prodromakis memristor at 325 ms compared to 360 ms when both memristor are applied at 1.2V.

It is impossible to build a circuit connection of NAND IMPLY logic in LTSPICE since it required two memristors in parallel. Moreover, when the number of parallel memristor increases, both current and step size will become very small, which the LTSPICE cannot accept time step size smaller than 10^{-6}.

5. CONCLUSION

As a conclusion, the Biolek memristor model is faster when switching than the Prodromakis memristor model. Moreover, both recorded the highest percentage of correct output at 4Hz with similar time taken. On the other hand, the nonlinear changes of the output which not proportional to the change of input influence the performance although the pattern for both models remain the same. This shows that the influence is reflect by the mathematical model used in the developing both Biolek and Prodromakis. Finally, the exceeding limit of memristor number influence the simulation performance since LTSPICE exceeding the small current time step limitation.

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