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# Design and Performance Evaluation of D-Flip-Flop using Various Technology Nodes

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## ABSTRACT

This work focus on design and analysis of various types of Master-Slave D FFs, as sequential circuits are essential for all synchronized circuits we focus on designing and evaluating different D FFs at different technologies. In this work it is observed that Low Power D FF i.e., Proposed D FF has given the better results when compared to the one we studied i.e., master-slave negative edge triggered D FF and the results are as follows, 106% in 22nm technology, 101.4% times better in 45nm technology, 0.8% better in 90nm technology, 5% better in 130nm technology when compared with conventional D FF or Master-Slave Negative Edge Triggered D FF in terms of Propagation Delay. Low Power D FF is 40.37% better in 22nm technology, 87.8% times better in 45nm technology, 92.4% better in 90nm technology, 63.5% better in 130nm technology when compared with conventional D FF or Master-Slave D FF in terms of power dissipation.

**Key words:** D-Flip Flop, Master-Slave, Propagation Delay, Low Power, Power Dissipation.

## 1. INTRODUCTION

In modern VLSI circuits, less power and high-speed designs are the essential parameters. To improve the performance of the system it is necessary to enhance the timing elements like latches and Flip-flops [7]. One of the major concerns is the construction of D Flip-Flop (FF) with optimistic power consumption and time delay. The most important categories to design any type of electronic system are sequential logic circuits [8]. We already know that D FFs (DFF) are the basic blocks for any type of digital integrated circuits. FFs are known as data storage elements [3]. For any sequential circuit, FFs are necessary components. There are different FFs among them D FF is most widely used. During the rising and falling edge of the clock pulse, it acquires the value of the D at the input and the outcome is unaltered at the reminder of the clock [4]. A D FF is also a clocked FF having two stable states. D FF works with a delay of one clock cycle. Delay created by data storage elements grabs a significant segment of the cycle from timing viewpoint as long as the frequency of operation rises. In the previous forty years, CMOS technology has been rapidly scaled with enormous speed and minimized power loss. As the CMOS method is coming towards nanometers scale, several parameters of many electronic devices get affected due to the scaling down dimensions. So the performance of the devices becomes challenging [5]. There is a huge demand for fast and robust devices [16]. Therefore choosing a flip-flop is essential for meeting the required functionalities of the higher system [12]. In this work we designed the five non-identical types of master-slave D FFs namely Clocked CMOS D FF, Push-Pull Isolation D FF, Master-Slave Negative Edge Triggered D FF, Master-Slave D FF that using CMOS logic gates and pass transistors and Low power D FF and their performance estimation of individual master-slave D FF has been evaluated. The paper is arranged in different sections. Section 2 provides all the working mechanisms of five different D FFs. Section 3 discusses the simulation results which include power dissipation, delay, and power delay product. Section 4 will give a conclusion.

## 2. MASTER-SLAVE D-FLIP FLOP TOPOLOGIES

This section explains the different Master Slave D-Flip flops considered for analysis in this paper.

### 2.1 Clocked CMOS D-Flip-flop

Clocked CMOS D FF consists of twenty transistors. This circuit comprises two parts, the first part is master and second is slave. The technique used here is clocked CMOS, where there is a usage of a clock and inverted clock for the functioning of a master-slave circuit. When the clock is active high the master acquires the input D, whereas the slave portion remains in off state and the feedback stage at the slave portion maintains in working condition such that it maintains the previous outputs it obtained from the previous stage, which is illustrated in figure 1 [13].

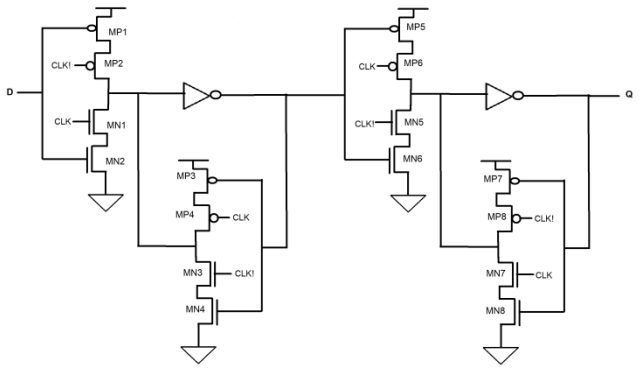


**Figure 1:**Clocked CMOS D-Flipflop (20T)

Now, to pass the data from the master to the slave portion of the circuit for this we provide active-low clock such that the master portion of the circuit becomes inactive and feedback at master remains active to pass the data acquired from master to slave portion [10]. Coming to the slave part, it is active and it provides stored input data at the master circuit part and the feedback stage at the slave part is in an off state which indicates that it has erased the previous outputs. In this way, the data is acquired by the slave from the master [13].

### 2.2 Push Pull Isolation D-Flip-flop

Push-Pull (P-P) Isolation D FF circuit consists of eighteen transistors. This circuit works on the push-pull effect occurring at the latch of a slave which is attached in the middle of the outcome of master and slave—latch, it helps the inverter to be moved by opposite logic values [13]. There are is an increase in delay of the circuit due to the addition of two PMOS FETS in the feedback loop part which makes the circuit more robust compared to the other circuits[13]. In Push-Pull Isolation D FF there are 18 transistors. It minimizes 16% of total power and enhances the speed by 25% of push-pull D FF[14]. This is circuit is a modification of push-pull D FF but there are PMOS in feedback path one at the master side and the other at the slave part[11]. The circuit diagram is shown in figure 2

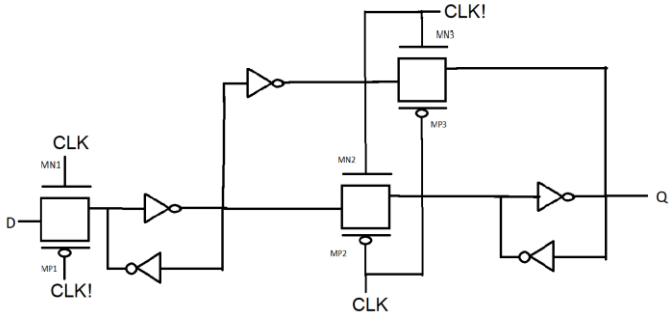


**Figure 2:** Push-Pull Isolation D flip-flop (18T)

This D FF plays a vital role in those devices where speed and performance have at most importance. From the above figure, the mechanism of the circuit is analyzed based on the functioning of the clock. Assuming the condition of the clock in Peak state, the master acquires the data for the time at which the clock is in Peak state, and the slave keeps hold of previous output. When the clock is at the peak state master stops acquiring the data and the slave fetches the data stored from the feedback of the master and generates the corresponding output at the slave [13].

### 2.3 Master Slave Negative Edge Triggered D Flip-flop

This circuit is called Negative Edge triggered D FF as the name suggests it acquires the input at the negative edge of the clock. It comprises of sixteen transistors. This is a type of a Master-Slave D FF that functions on the negative edge of the clock which shows that it is Negative edge Triggered Flip-Flop. It is formed by combining two D latches. The master part follows the clock and the slave part follows an inverted clock. The master part is positive level sensitive and the slave part is negative level-sensitive as shown in figure 3.

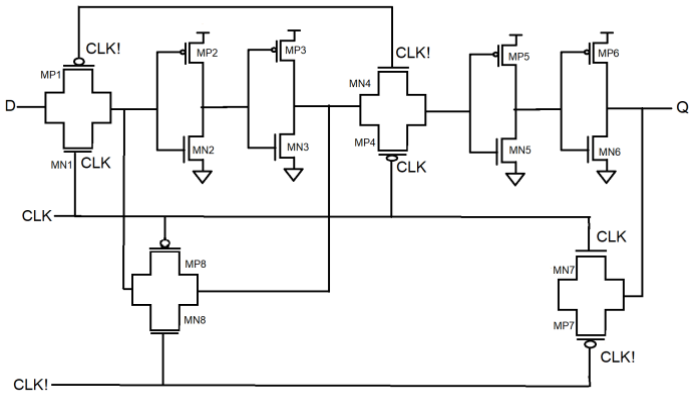


**Figure 3:** Master Slave Negative Edge Triggered D Flip-Flop

When the clock is at the peak state, the master follows the inputs given by D as it indicates master is in ON condition and at the slave part it is OFF state whereas the feedback loop maintains previous values. During the transition from 1 to 0, the master latch stops acquiring inputs and maintains a record of values of D during the transition of the clock while the slave latch is in ON condition due to this it gives the output values stored by master part. The output is not affected by input as the master stage is in OFF condition. While the clock moves from low to high the master acquires the values of input signal D and the slave latch maintains the output obtained from the master latch. One thing to be noted that the circuit is affected if the master part experiences a set-up time violation. In this case, the input D transits from low to high just before the clock transition is observed, in other words, it is set up time violation. Due to this the master part is unable to latch the true value and the slave stage produces the enormous output. To avoid and control these sorts of the situation there should be synchronization of the relative timing of input and clock signals.

### 2.4 Master–Slave D flip-flop that using CMOS logic gates and pass transistors

This D FF comprises of fourteen transistors. In figure 4 is the design of D FF consists of pass-transistors and inverters.

There are two memory loop circuits in this architecture. As a D FF is a memory storage cell. This structure is designed using one master memory cell towards the left and slave memory cell towards right [15].

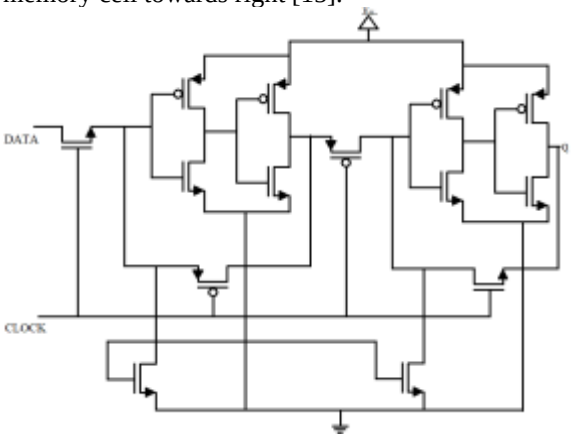


**Figure 4:** Master–Slave D flip-flop that using CMOS logic gates and pass transistors(14T)

In this figure 4 whenever clock is in high state then the value which is given near input D is updated near the master latch. Since the master latch is working, the slave latch stores the previous state of the input D and produces the same as output Q. Now, if the clock is in low state then the slave circuit is updated with the new output and in the meantime master latch maintains the previous value. The active edge of the clock is regarded as the change of the clock from 1 to 0(high to low). So it is a negative edge triggered flip-flop[15].

### 2.5 Low Power D Flip-Flop

Low Power D FF comprises of sixteen transistors. This FF is alike to that of a transmission gate based FF, but the change lies in the feedback part which comprises two PMOS and NMOS which are attached in the end to end at the up and downwards respectively as shown in figure 5 below [13].

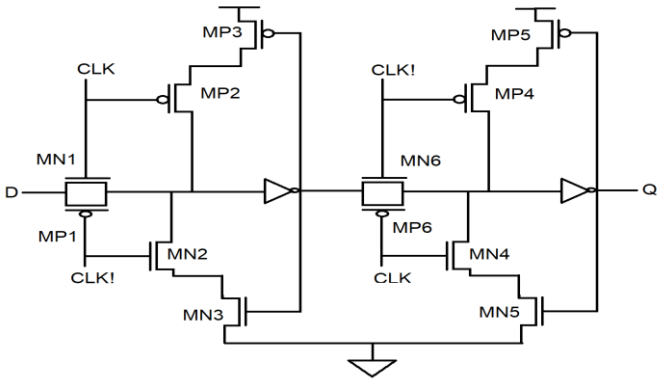


**Figure 5:** Low power DFlip-Flop(16T)

Considering the case of a clock being active high, the master is enabled and it takes the input and slave part is disenabled and the feedback part is in working condition where it maintains the previous outputs. In this case, the MP4 and MP5 are functioning and the remaining MN4 and MN5 are in OFF state which indicates the feedback of NMOS transistors is OFF. However, the loop is made by MP4 and MP5 which holds the previous outputs generated. Coming to the master side it is taking the input signal D and the feedback loop is not active [13]. When the clock is active low, the master is disabled as the transistors MP1 and MP2 are OFF state and it does not take any input and the slave part is enabled where it takes the previously stored values from input D and process to the output side [13].

## 3. RESULTS AND DISCUSSION

This section presents the simulation setup and various D-Flip-flop topologies taken in this paper. The comparison of the propagation delay and power consumed is done and the results are reported below

### 3.1 Simulation Setup:

Here we present the simulation results. As we considered various D FFs, all the simulation results are compared with each other. The table 1 below shows the Simulation Setup at Different Technologies. This table shows the properties and several parameters that have to be considered while designing a circuit at different nanometer (nm) technologies i.e. VDD(V), P & N Length, PWidth, N-Width. The values we considered are shown in the below mentioned table 1.

**Table 1:**Simulation setup at Different Technologies

| **CMOS Technology** | **130nm** | **90nm** | **45nm** | **22nm** |
|---|---|---|---|---|
| **VDD (V)** | 3.2 | 1.8 | 1.2 | 1.0 |
| **P & N Length** | 0.13 | 0.09 | 0.045 | 0.022 |
| **P-Width** | 0.26 | 0.18 | 0.09 | 0.044 |
| **N-Width** | 0.13 | 0.09 | 0.045 | 0.022 |

### 3.2 Propagation Delay:

It is the amount of time taken for a circuit to get the desired output for a given input. There are many topologies while designing a circuit so we look for the circuit which has the minimum delay [4]. While comparing all the circuits we discussed the delay(ns) results are as follows in table 2.

**Table 2**: Propagation Delay for D Flip-Flops at Different Technologies

| **CMOS Technology** | **130nm** | **90nm** | **45nm** | **22nm** |
|---|---|---|---|---|
| **Clocked DFF** | 258.27 | 257.74 | 25.70 | 20.20 |
| **Isolated DFF** | 258.21 | 201.94 | 20.202 | 20.228 |
| **CMOS Negative edge triggered** | 80.05 | 50.103 | 20.02 | 39.9 |
| **Master Slave DFF using Pass Transistor &cmos gates** | 80.50 | 50.103 | 2.803 | 1.3 |
| **Low power DFF** | 76.40 | 50.037 | 0.03158 | 2.4302 |

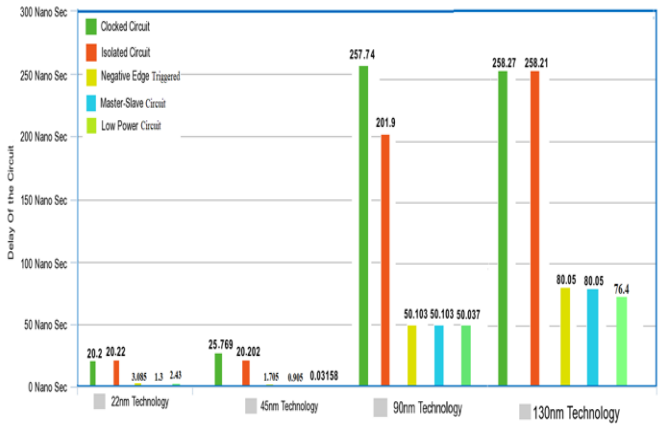


**Figure 6:** Propagation Delay Graph

In 130nm we can see Low power D flip flop is the best circuit which has 16 transistor count and Vdd is 3.2V. In 90nm technology, we find Low power D flip flop is the best which contains 16 transistors having Vdd is 1.8V. In 45nm technology, we can see Low power D flip flop is the best one having 16 transistor count and Vdd is 1.2V. In 22nm technology, we observe that master-slave D flip flop is the best circuit that has 14 transistor count and Vdd is 1.0V.

While comparing the Master-Slave Negative edge-triggered circuit the Clocked CMOS circuit is 50.6% better in 22nm technology. Master-Slave Negative edge-triggered circuit is 27.22% better in 45nm technology, 414.3% better in 90nm technology, 222.56% better in 130nm technology. Isolated D FF is 50.6% better in 22nm technology. Master-Slave Negative edge-triggered circuit is 0.8% times better in 45nm technology, 302.9% better in 90nm technology, 222.5% better in 130nm technology. Master-Slave D FF using pass-transistor is 103.2% better in 22nm technology. 113.8% times better in 45nm technology. Low Power D FF is 106% better in 22nm technology, 101.4% times better in 45nm technology, 0.8% better in 90nm technology, 5% better in 130nm technology.

### 3.3 Power Dissipation:

Power dissipation occurs when there is a switching activity between ON and OFF state. The total power consumed by all the transistors for getting the desired output is called the power dissipation of the circuit. It varies with the number of transistors used in the circuit and they are as follows.

**Table 3**: Power Dissipation for D Flip-Flops at Different Technologies

| CMOS Technology | 130nm | 90nm | 45nm | 22nm |
|---|---|---|---|---|
| **Clocked DFF** | 185.04 | 11.082 | 1.6295 | 2.3517 |
| **Isolated DFF** | 249.84 | 39.63 | 27.507 | 6.2329 |
| **CMOS Negative edge triggered** | 406.58 | 11.447 | 1.7051 | 3.0859 |
| **Master Slave DFF using Pass Transistor &cmos gates** | 448.07 | 1.5 | 0.90526 | 7.7 |
| **Low power DFF** | 148 | 0.8597 | 0.2081 | 1.84 |

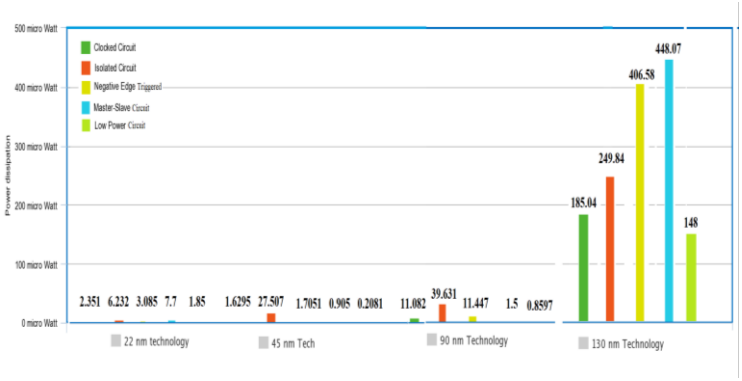


**Figure 7**: Power Dissipation Graph

In130nmwecanseeLowpowerDflipflopisthebestcircuit which has 16 transistor count and Vdd is 3.2V. In 90nm technology we find Low power D flip flop is the best which contains 16 transistors having Vdd is 1.8V. In 45nm technology we can see Low power D flip flop is the best one having 16 transistor count and Vdd is 1.2V. In 22nm technology we observe that master slave D flipflop is the best circuit which has 14 transistor count and Vdd is1.0V.

While comparing the Master-Slave Negative edge-triggered circuit the Clocked CMOS circuit is 23.79% better in 22nm technology, 4.43% times better in 45nm technology, 4.6% better in 90nm technology, 54.48% better in 130nm technology. Isolated D Flip-flop is 38.55% better in 130nm technology, Master-Slave Negative edge-triggered circuit 246.2% times better in 90nm technology, 150% better in 45nm technology, 101.8% better in 22nm technology. Master-Slave D Flip-flop using pass-transistor is 10% better in 130nm technology, 86.89% times better in 90nm technology, 93% better in 45nm technology, 150% better in 22nm technology. Low Power D Flip-flop is 40.37% better in 22nm technology, 87.8% times better in 45nm technology, 92.4% better in 90nm technology, 63.5% better in 130nm technology.

### 3.4 Power Delay Product

It is figure of merit associated with the energy efficiency of a circuit. Power Delay Product (PDP) is the result obtained from the product of Power of the circuit with the delay of that circuit. The PDP values of different circuits are as follows in table 4.

**Table 4**: Power Delay Product for D Flip-Flop at Different Technologies

| CMOS Technology | 130nm | 90nm | 45nm | 22nm |
|---|---|---|---|---|
| **Clocked DFF** | 47790.28 | 2856.274 | 41.865 | 47.507 |
| **Isolated DFF** | 64513.93 | 80002.882 | 555.696 | 126.079 |
| **CMOS Negative edge triggered** | 32546.72 | 573.529 | 34.134 | 123.091 |
| **Master Slave DFF using Pass Transistor &cmos gates** | 35868.003 | 75.1545 | 2.536 | 10.01 |
| **Low power DFF** | 113.3776 | 42.9817 | 0.00655 | 4.4715 |

**Table 5:** Total values of all the circuits

| D Flip-Flop Type | Transistors Count | Different NM | Delay(ns) | Average Power(µW) | Power Delay Product =Delay*Avg power (fJ) |
|---|---|---|---|---|---|
| **Clocked CMOS DFF** | 20 | 22 | 20.2 | 2.3517 | 47.504 |
| | | 45 | 25.7 | 1.6295 | 41.865 |
| | | 90 | 257.74 | 11.082 | 2856.274 |
| | | 130 | 258.27 | 185.04 | 47790.28 |
| **Push-pull isolation DFF** | 16 | 22 | 20.228 | 6.2329 | 126.079 |
| | | 45 | 20.202 | 27.507 | 555.696 |
| | | 90 | 201.94 | 39.63 | 80002.882 |
| | | 130 | 258.221 | 249.84 | 64513.934 |
| **CMOS negative edge-triggered master-slaveDFF** | 16 | 22 | 39.9 | 3.0859 | 123.091 |
| | | 45 | 20.02 | 1.7051 | 34.134 |
| | | 90 | 50.103 | 11.447 | 573.529 |
| | | 130 | 80.05 | 406.58 | 32546.729 |
| **Master–Slave D flip-flop that using CMOS logic gates and pass transistors** | 14 | 22 | 1.3 | 7.7 | 10.01 |
| | | 45 | 2.803 | 0.90526 | 2.536 |
| | | 90 | 50.103 | 1.5 | 75.1545 |
| | | 130 | 80.05 | 448.07 | 35868.0035 |
| **Low power D Flip-Flop** | 16 | 22 | 2.4302 | 1.84 | 4.4715 |
| | | 45 | 0.03158 | 0.20819 | 0.00655 |
| | | 90 | 50.037 | 0.859 | 42.9817 |
| | | 130 | 76.4 | 148 | 113.3776 |

Nano Seconds(ns)=10-9 S, Micro Watt(µW)=10-6 W, Femto joule = 10-15 J.

The above table 5 will give a glance at the different circuits we used with different technologies and their transistor count. As we know that the power dissipation, delay of a circuit varies with technology we used, the logic behind the circuit, and the transistor count. Some recent developments were also presented in references [17-20].

## 4. CONCLUSIONS

This work is focused on identifying high-performance Master-Slave D FF at different technologies namely 22nm, 45nm, 90nm, and 130nm. There are few techniques like adaptive body biasing, device length upsizing, etc. which can be used for improving the performance of the circuit. It makes a hefty task for a circuit designer easier in selecting suitable the design one from among those available topologies to meet the design specifications. Considering the results from table 3 low power D FF is found to produce minimum delay among the five different D FFs in most of the cases under different nm technologies. Low Power D FF or Proposed D FF had shown with a significant percentage of 106 in 22nm technology, 101.4% times better in 45nm technology, 0.8% better in 90nm technology, 5% better in 130nm technology when compared with conventional D FF or Master-Slave Negative Edge Triggered D FF in terms of Propagation Delay. Low Power D FF is 40.37% better in 22nm technology, 87.8% times better in 45nm technology, 92.4% better in 90nm technology, 63.5% better in 130nm technology when compared with conventional D FF or Master-Slave D FF in terms of power dissipation. This is concluded that Low Power D FF is showing better performance at various technologies when compared with remaining.

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