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Reference Signatures and Selective Test Pattern Generator based Model Predictive Control Technique for Test Response Prediction in Low power BIST

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ABSTRACT

Power reduction is an important aspect for achieving high quality tests. The proposed work in this paper is a modern technique for reduction of power consumption by way of reducing number of switching cycles. The model predictive technique which works on the principle of prediction of output results for a given input. Prediction technique wherein reference signatures are used for analysis of test responses and future prediction of test patterns to be injected to carry out testing. The future prediction is based on past test patterns and corresponding test responses. The trained intelligent system is implemented using selective test patterns from test pattern generator. The selectiveness in test patterns reduces switching cycles and hence power consumption.

Key words: Power reduction, Model Predictive Control (MPC), Redundant (RD), Non-Redundant (NRD).

1. INTRODUCTION

Reducing test cost is essential for VLSI chip testing. In scan based test operations, high data activity causes circuit to dissipate more power. Reduction in test power is the topic of concern from testing point of view [1]. The increased power dissipation during test might cause thermal issues, power droop, voltage noise or excessive peak power. It may further result in instant device damage, short product lifetime, device malfunction or decrease in reliability of the chip. Abnormal switching can cause failure in fully functional chip die to crosstalk, IR drop phenomena or di/dtissue [2]. Various methods are proposed for reduction of power during testing. The major objective of producing a test is to guarantee reliable as well as high quality for the semiconductor products. With new sorts of imperfections that one should consider to give the ideal test quality to the following innovation hubs, for example, 3D, it is fitting to offer the conversation starter of what coordinating DFT strategies should be conveyed. Test compression, presented 10 years prior, rapidly turned into the standard DFT philosophy. In any case, it is vague whether test compression will be fit for adapting to the quick pace of mechanical changes throughout the following decade. Curiously, Logic Built In Self Test (LBIST), initially created for board framework, in the field level test which is presently picking up acknowledgment for generation test as it gives exceptionally strong DFT and is utilized progressively frequently with test pressure. This cross breed approach is by all accounts the following legitimate developmental advances in designs for testability (DFT) technologies. There are benefits in terms of improvement in test quality, this might significantly enlarge capacities to keep running for speed power testing and it may decrease the expenses of assembling test with saving overall LBIST and advantages of scan compression. The main areas in VLSI which are more challenging are Area, power, reliability, performance and cost. There is a rapid increasing need for handy computing instruments, equipment required for daily life and communication systems. Built in self testis a design methodology in which the components / parts of a circuit are utilized to test the circuit within itself. BIST means the ability of circuits to test them. BIST appears as an amalgamation of the concept of self-test and built-in-test [3].

A new method is proposed, offers behavior closely related to Model Predictive Control (MPC) concept. It observes output test responses for given test patterns and carry out further analysis by referring to reference signatures for each pair of test pattern and test response. The end result of this analysis derives don't care conditions as far as test patterns is concerned. These conditions are further used to cut down number of scan cycles. The entire exercise is executed by an entity hereby termed as a Test Controller. The test patterns generator like a free wheel, generates pseudorandom test patterns continuously but it is a Test Controller , decides what test patterns are to be moved further to execute scan cycles. The Test Controller does this by making use of Toggle-Hold mechanism. With the use of model predictive control based test compressor to reduce the size of tests. In hold state current pattern is locked at Toggle/Hold logic block and hence not passed to the Circuit Under Test (CUT). These test patterns are termed as Don't Care (DN) Test Patterns or Redundant (RD) Test Patterns. Non-Redundant (NRD) Test

Patterns are allowed to move further to carry out tests. The Toggle state is where NRD Test Patterns are allowed to move further and carry out test and in Hold state; RD Test Patterns are kept on hold and not allowed to move further to carry out tests. This is similar to enabling and disabling of a latch. When latch is enabled, test patterns move through latch, may be termed as a transparent state of a latch. When latch is disabled, test patterns do not move through latch, may be termed as a non-transparent state of a latch. The transparent state may also be termed as Toggle state and non-transparent is Hold state. This selective approach while operating Toggle/Hold state reduces switching cycles drastically and hence power consumption [3, 4].

2. LITURATURE SURVEY

A design methodology has been proposed by way of formulation in the context of on-chip BIST for pattern generator. This pattern generator mainly consisting of 2 components i.e. first one is a GLFSR acts as a PRPG (pseudo random pattern generator), as proposed previously and another is combinational logic, which is useful to suitably synchronize the outputs of the PRPG. Using lesser test patterns in conjunction with a unique area overhead which is small, this amalgamated logic block may be developed to achieve about cent-percent single stuck at fault coverage [4]. New low power built n self-test, TPG method is proposed. The method uses mux and transition monitoring window block. Transitions of random patterns developed by LFSR match with pseudorandom Gaussian distribution. These are represented by using k values obtained from TMW distribution. Scan transitions can be reduced up to 60% by this method [5]. A hybrid BIST approach was proposed. This hybrid BIST extracts the frequent occurrence sequences from the systematized test patterns. The stored sequences are used in sequence extraction which is done in cluster analysis which is encoded systematized patters. The results of experiments for ISCAS-89 benchmark circuits depicts that the proposed approach always need minimum on-chip storage and the volume of test data as compared to other BIST techniques recently developed [6]. The architecture of mixed mode BIST, scan based is put forth. Storage needs of systematized patterns depend upon 2-Dimesional compression method which utilizes advantages of horizontal and vertical compression methodologies. Decreased storage space was shown in experimental results [7]. The combination of statistical coding and LFSR (linear feedback shift register) reseeding and is utilized in lossless test vector compression scheme as an efficient way. By getting a solution of linear equations, test vectors can be encoded as linear feedback shift register seeds. Quite large space of solution of the linear equations may be obtained. Benefit of the large solution space is considered by the proposed methodology to explore seeds which may be efficiently encoded by utilizing statistical code. There are dual architectures which are described for implementation of LFSR reseeding with seed compression [8].
While using a bit-swapping technique, a modified LFSR diminishes the transition counts at inputs of the CUT by approximately25%. Power reduction upto45%is shown during test in results of the experiments on ISCAS-85 and ISCAS-89 benchmark circuits. IT is also seen that the design under consideration may be amalgamated with another methodologies to get success of power reduction i.e. up to 63% [7,9]. Girard proposed a technique titled as Random single input change (RSIC) test generation. A maximum level of fault coverage for low power BIST circuit is provided by it. Implementing BIST and analyzed for RSIC generator is executed [10]. The work presented focuses on the carry look ahead adder to speed up the addition operation placed at most significant bit position. The results for the power reduction along with speed and area were synthesized using Xlinix and Verilog [13].

Various operational models of varied fault modeling methods of random memories and flash memories are taken into consideration. BIST methodologies are demonstrated to decrease the fault [11]. LP test method is proposed that is in conversant for BIST and test compression. Using micro-controller that allows decrease in switching rates during feeding the scan chains power reductions may be obtained; it results into low toggling activity. Voltage drop and hence decrease in power dissipation [7, 8]. Advantages of deterministic external testing and pseudorandom LBIST are combined by Deterministic logic BIST (DLBIST) test strategy. DLBIST synthesis method has linear complexity for memory and computation. The algorithms which are based on binary decision diagrams are eventually tested on industrial designs with maximum 2M gates [12]. Ordered binary decision diagrams are used for functional representation causes significant impetus to algebraic CAD techniques. Gate level ATPGs are generated using OBDDs [16]. In this paper author focused on the regression testing technique to improve the fault detection while executing the test cases. Genetic algorithm used for test case prioritization gives better results observed not only for solving regression testing problem. Author observed the changing in the vital parameters such as crossover and mutation [17].

Hybrid approach of combined Built in Logic Test and external testing is formed for test data compression scheme. This methodology is dependent on weighted pseudorandom testing. To store the weights efficiently two methods are given [6, 8]. A new method for on chip generation of test pattern is proposed by the author. Test patterns are developed by LFSR i.e. pseudo-random pattern generation. It helps to get desired fault coverage. The logic of mapping is used to decode the sets of patterns. Combinational mapping logic is placed between PSPR and the CUT. This method decreases the test length which is needed for fault coverage by considering magnitude orders which are compared by using LFSR [7, 14]. To reduce switching activity of CUT, author proposed inhibiting technique for test vector. It helps to reduce switching activity hence reduces power consumption. Vector inhibiting and reseeding techniques are combined to work with hard-to-test a circuit which contains pseudo

random resistant faults. These methods help to decrease power consumption while testing, which also helps to achieve high fault coverage [14]. A new method called low power test per clock with BIST TPG is used. It helps to reduce toggling activity during the test operation. Clock system is changed in the said method for test pattern generation and clock free feeding is done for TPGs [16].

3. TEST COMPRESSOR WITH TOGGLE / HOLD LOGIC

Figure 1 shown below is a block diagram of the methodology envisaged. Test Controller observes test response for a given test pattern. It carries out further analysis by referring to reference signatures with each pair of test pattern and test response. The end result of this analysis is identification of RD and NRD test patterns. Hence test patterns are segmented into two segments. Test Controller makes use of this segmentation while selection of Toggle and Hold state [4]. The circuit is comprised of 8 bit Pseudorandom Test Generator and custom design CUT. The Figure 2 describes the architecture of CUT custom design.

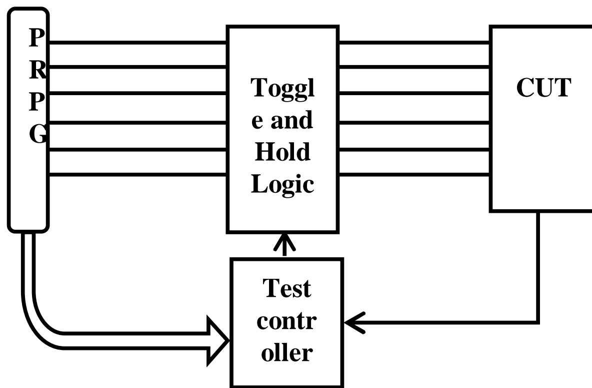

Figure 1: Block diagram of Test Controller

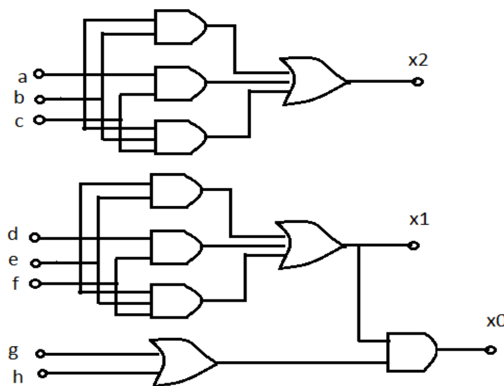

Figure 2: 8-bit circuit under test

With reference to Figure 2, Test pattern size is 8 bits and size of test response is 3 bits. After applying 8 bit patterns as input to the CUT, 3 bit output is generated. By observing truth table of CUT and solving the Boolean expression of circuit, RD/NRD states are identified. Test Controller further carries out analysis by referring to reference signatures and each pair of test pattern and test response. The end result of this analysis is usage of selective approach as far as selection of Toggle and Hold states. It can be further simplified as follows.

- With reference to Figure 2, the size of test pattern is 8 bits.
- It means, there may be 256 test patterns at max.
- To carry out testing, it is necessary for each test pattern to be injected into the system.
- Proposed method does not use all 256 test patterns and still manages to test CUT successfully. It reduces switching cycles and hence power consumption too.

Test Controller Algorithm:
Algorithm Precursor:

1. Construction of truth table comprising 8 bits Test Patterns and corresponding Test Responses.
2. Identification of RD and NRD Test Patterns.
3. Identification of reference signatures for each NRD Test pattern.

Actual Algorithm:

4. Receive Pseudorandom Test Pattern.
5. Check whether it is NRD or RD Type.
6. If NRD, observe Test Response
   6.1. Compare Test Response with Reference Signatures.
   6.2. If result is true, check whether all NRD Test Patterns checking is over. If no, carry on exercise for rest of test patterns.
   6.3. if result is not true, discontinue the exercise.
7. If RD, check the result of NRD processing. If all successful, ignore RD Test pattern otherwise discontinue the exercise.

4. RESULT AND DISCUSSION

Figure 3 shown below shows the simulation output of test controller with toggle and hold logic. Test patterns are passed to CUTif the 'reset' signal is high. It is the toggle mode of system. When redundant test patterns are arrived at toggle and hold logic, 'reset' signal becomes low and test patterns are not passed to CUT. System is at hold mode when reset signal is low. X is the 3 bit output of CUT.

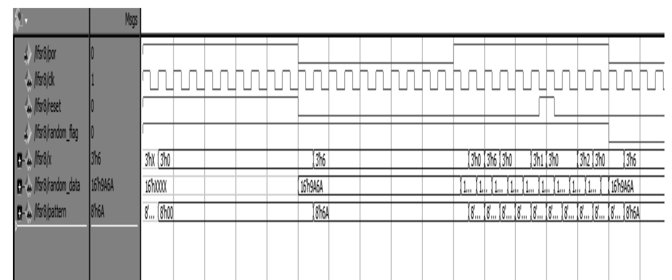

Figure 3: Simulation output of Test Controller with Toggle and Hold logic

Table 1 shows the area utilization of proposed Test controller with toggle and hold logic. Table 2 shows power utilization of proposed Test controller with toggle and hold logic. Figure 4 shows the RTL schematic of CUT interface with pattern generator.

Table 1: Area Utilization of Test Controller

		Used	Available	Utilization (%)
Slice Logic Utilization	Number of Slice Registers	16	4800	0
	Number of Slice LUTs	2	2400	0
	Number used as Logic	2	2400	0
Slice Logic Distribution	No. ofLUT Flip Flop pairs used	17		
	Number with an unused Flip Flop	1	17	5
	Number with an unused LUT:	15	17	88
	Number of fully used LUT-FF pairs	1	17	5
	Number of unique control sets	1		
IO Utilization	Number of IOs	39		
	Number of bonded IOBs	30	102	29
	IOB Flip Flops/Latches	1		
Specific Feature Utilization	Number of BUFG/BUFGCTRLs	1	16	6

Table 2: Power Utilization of Test Controller

Power Consumption (mW)	Total Power Consumption	Dynamic Power Consumption	Static Power Consumption
	110.83	96.16	14.68

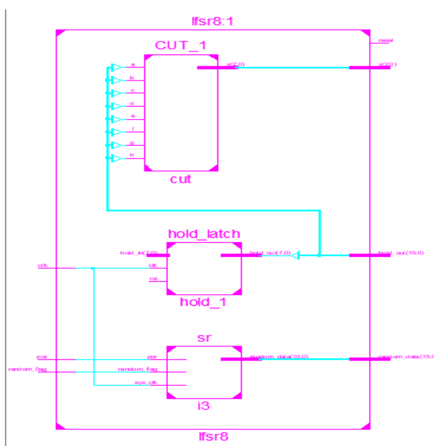

Figure 4: RTL schematic of CUT interfaced with Test Pattern Generator

Figure 5 shows simulation output of CUT interfaced with Test Pattern Generator. 8 bit pattern is applied to CUT for 3 bit output signal 'x'. Table 3 shows area utilization of CUT with Test Pattern Generator. Table 4 shows power consumption of CUT with test pattern generator.

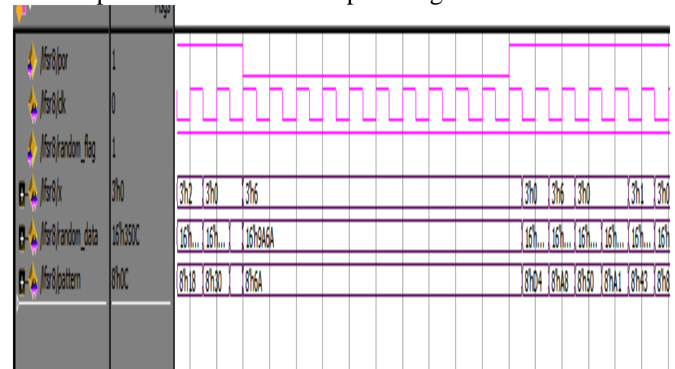

Figure 5: Simulation output of CUT

Table 3: Area utilization of CUT with Test Pattern Generator

		used	Available	Utilization (%)
Slice Logic Utilization	Number of Slice Registers	16	4800	0
	Number of Slice LUTs	5	2400	0
	Number used as Logic	5	2400	0
Slice Logic Distribution	Number of LUT Flip Flop pairs used	17		
	Number with an unused Flip Flop	1	17	5
	Number with an unused LUT:	12	17	70
	Number of fully used LUT-FF pairs	1	17	23
	Number of unique control sets	1		
IO Utilization	Number of IOs	39		
	Number of bonded IOBs	22	102	21
	IOB Flip Flops/Latches	1		
Specific Feature Utilization	Number of BUFG/BUFGCTRLs	1	16	6

Table 4: Power consumption of CUT with Test Pattern Generator

Power Consumption (mW)	Total Power Consumption	Dynamic Power Consumption	Static Power Consumption
	129.75	114.86	14.88

It is observed and demonstrated that power consumption of the CUT integrated with pattern generation system is lesser than the conventional testing system due to the use of Test Controller. As Toggle and Hold logic reduces switching, it helps to reduce power consumption.

5. CONCLUSION

Test Controller with Toggle or Hold logic is implemented for the purpose of reducing number of tests. It uses Model Prediction Control based concept which considers present and past input /output states to implement the control logic. As limited test patterns are forwarded to the CUT, switching activity is reduced. Reduced switching helps to reduce power consumption. The design is evaluated on Xilinx's Spartan 6 FPGA. From experimental results it is observed that Test Controller is beneficial to reduce the power consumption of the system as hold logic limits all patterns from testing through CUT. For achieving high quality tests with reduced power consumption this methodology can be used.

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