ISSN 2347 - 3983
Volume 8. No. 6, June 2020
International Journal of Emerging Trends in Engineering Research
Available Online at http://www.warse.org/IJETER/static/pdf/file/ijeter52862020.pdf
https://doi.org/10.30534/ijeter/2020/52862020

High Speed and Energy Efficient FIR Filter Using Concatenation Incrementation Carry Skip Adder

Sasikala S[1], Chitra M[2], Kawya M [3], Kiruthika S[4], Lavanya R G [5]
[1]Associate Professor, [2]Assistant Professor, [3,4,5]Student
Department of Electronics and Communication Engineering, Kongu Engineering College, TamilNadu, India
sasikalapriyaadarsan@gmail.com, chitra.ece@kongu.edu

ABSTRACT

Finite Impulse Response (FIR) filter is the most important digital filter used for noise removal. The performance of the FIR filter gets degraded due to the presence of multipliers and adders. Number of research work has been carried out to improve the speed, area and power of the FIR filters. In this project, Concatenation Incrementation Carry Skip Adder (CI-CSKA) is proposed to increase the speed and to reduce the power consumption of the adder. Using CI-CSKA, the multiplier units are designed and FIR filter is constructed further. The proposed adder is coded using verilog and implemented in Spartan FPGA. The performance of the adder, multiplier and the FIR filter is analyzed and compared with conventional carry skip adder. From the analysis, it is observed that the area of the FIR filter using 4 bit CI-CSKA adder and multiplier is reduced by 58.33% compared with conventional CSKA adder and multiplier. Also the delay of the FIR filter is reduced to 12.15% compared with the conventional CSKA. The area of FIR filter using 8 bit CI CSKA adder and multiplier is reduced by 58.11% compared with conventional 8 bit CSKA adder and multiplier. The delay of FIR filter is reduced to 3.56% compared with conventional 8 bit CSKA.

Key words: Carry Skip Adder, Concatenation Incrementation CSKA, FIR Filter, Xilinx FPGA.

1. INTRODUCTION

Finite Impulse Response **(**FIR) filter is a fundamental processing element in many Digital Signal Processing (DSP) systems. FIR filters are used in DSP applications ranging from image and video processing to wireless communication. Arithmetic circuits like adders and multipliers are basic building blocks of FIR filter[11]. The performance of the FIR filter is largely influenced by the multiplier, which is the slowest block out of all. Hence to increase the speed[2] and to reduce the power consumptions of multipliers various techniques were proposed in literature. The Finite Impulse Response Filter has been proposed using two different multipliers namely Array multiplier and Booth Multiplier and both the proposed FIR filters have been compared for various parameters [1]. Vedic Multiplier [6] and various Carry Skip Adders(CSKA) were used in multiplier design to reduce the power and to increase the speed [3]. Error Tolerant adder and modified Wallace tree multipliers [7] consume less power compared to conventional adder and multipliers. To reduce both the delay and power consumption CSKA are used [4][5][8]. Anurupye multiplier [9] was proposed to design the FIR filter which has 18.99% of reduction in delay and 4% reduction in area. 4-tap FIR filter was designed using modified ETA and multipliers was reported in [4]. In [10] Kartsuba and computation sharing multiplier were incorporated to design adaptive filters. The measurement of counting WBCs, RBCs and platelets were discussed in [12]. The presentation of the paper is as follows. Introduction of FIR filter and various multipliers is provided in Section I. Section II deals with the FIR filter, Section III incorporates the conventional CSKA. Section IV presents the CI-CSKA Section V Implementation results and Section VI deals with conclusion.

2. FINITE IMPULSE RESPONSE FILTER

An FIR filter is based on feed-forward difference equations. Feed-forward means that there is no feedback of past or future outputs to form the present output, just input related terms. Equation 1 represents the FIR filter equation.

$$y[m] = \sum_{k=0}^{N} b_k x[m-k] \quad (1)$$

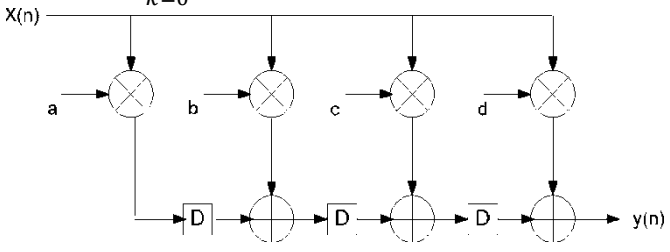

Figure 1: 4-Tap FIR Filter

Figure 1 show the basic 4-tap FIR filter structure. The basic building blocks of the 4-tap FIR filter are shown in the Figure

2.

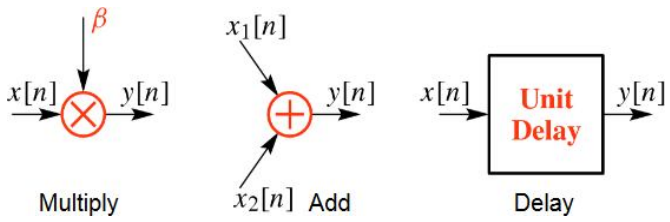

Figure 2: Basic building blocks of FIR Filter

A high quality filter will in general require more multiplications than one of lesser quality, so throughput suffers if the multiplier is not fast. There are classes of filters that do not require multiplies. FIR filters having 50 coefficients or more are not that uncommon. Signal addition is a very basic function. In an FIR filter, additions are required in combination with multiplications; hence microprocessors feature Multiply Accumulate (MAC) units. Adders generally operate with just two inputs at a time. The unit delay provides a one sample signal delay. A sample value is stored in a memory slot for one sample clock cycle, and then made available as an input to the next processing stage. An M-unit delay requires M memory cells (note each memory cell must store say B-bits) configured as a shift register(B-bits wide).

To build an efficient FIR filter it is needed to design high speed and energy efficient adder and multiplier circuit.

3. CARRY SKIP ADDER

A Carry Skip Adder (CSKA) has the advantage of reducing the delay in the addition process compared to the Ripple Carry Adder (RCA). The enhancement of the delay is achieved by using N number of carry skip adders forming a block of carry skip adder. The Carry of the CSKA is skipped and hence its implementation is used to increase the speed the additional operation and the carry bit is added in the last entire portion of the adder. The worst case for a simple one level carry-ripple-adder occurs, when the propagate-condition is true for each digit pair. In CSKA multiplexer is used to skip the carry which is represented if Figure 3. The MUX selects the carry for next state during propagation of every input waiting for addition of last bit in previous state. To decrease the delay and area of the skip logic static AOI and OAI gates are used instead of static 2:1 multiplexer. To decrease the area full adders are replace by half adders. The power consumption and the area utilized by the CSKA are same as it is in the RCA, but delay path is better and lesser when compared to RCA. This greatly reduces the latency of the adder through its critical path, since the carry bit for each block can now "skip" over blocks with a group propagate signal set to logic 1 (as opposed to a long ripple-carry chain, which would require the carry to ripple through each bit in the adder).

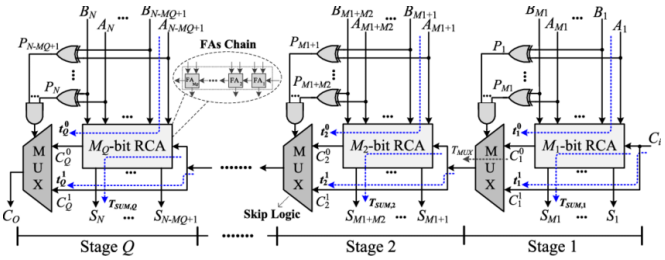

Figure 3: Block Diagram of 4 Bit Carry Skip Adder

3.1 Carry Skip Logic

The skip logic consists of an input AND gate and one multiplexer. The skip logic comprises of OR-AND-Invert and AND-OR-Invert instead of 2:1 multiplexers. Comparing with the multiplexers the OAI and AOI in the skip logic have smaller delay and less number of transistors which forms its advantage. The main aim of utilizing the skip logic is the number of transistors. The number of transistors when using the OAI or AOI skip logic complex gates is only six when compared to the Conventional method of using CSKA having the 2:1 multiplexer which has 12 transistors. The increase in the number of transistors leads to the increase in the area consumption which may further increase the power and delay of the circuit. Two operational cases exist in the operation of AOI and OAI viz., i) carry that propagates from the previous state and ii) carry is doesn't propagates. The intermediate bits will become logic '1' if the carry propagates from earlier stage and all input bits are in the condition of carry propagation then it will be transferred to AOI. The presence of AND gate in the first gate of AOI generates logic '1' only if there is a carry from preceding stage is logic '1'. The NOR gate in the second stage of AOI produces logic '0' if its input is logic '1' which is the inverted value of carry from its preceding stage. This bit is yet again inverted by a NOT gate and applied to incrementation block.

4. CONCATENATION INCREMENTATION CARRY SKIP ADDER

The CI-CSKA contains two inputs and N stages. Each single stage comprises of a Ripple Carry Adder block with the block size of Mj. The input carry of all the Ripple Carry Adder blocks, is zero excluding the initial block which denotes the concatenation of all the Ripple Carry Adder blocks. Therefore, all the execution of all the blocks is done at the same time period. During the computation of the sum of the initial block the other blocks also simultaneously computes their intermediate results and carry out (Cj) signals. In the CI-CSKA structure, the initial stage has an only single block of Ripple Carry Adder. The remaining stages consist of two blocks of Ripple Carry Adder and incrementation block. To provide the final sum of the stage, the results obtained from the RCA and the carry output of the preceding stage is used. The incrementation block comprises of array of half adders. The carry input of all the stages except first stage is given as

zero. Thus when giving an input, all the RCA block produces their individual sum and carry output. Since the carry input of each stage is zero simultaneous addition is takes place and each stage does not wait for the previous carry out .When the first block compute the summation of its corresponding input all other block compute the intermediate result. The output of all RCA block except first block is called as intermediate result because the actual carry is not structure of modified carry skip adder (CI-CSKA) added in this stage. Then on adding the carry input as zero for performing simultaneous operation. This is the concatenation process, therefore the obtained output of RCA block is not an actual result, thus it is mentioned as an intermediate result. The incrementation block is used to add the intermediate result with the carry output of preceding stage. The carry output of next stage is determined by the skip logic which is predicted depending on the in-between result and carry output of preceding stage as well as carry out of corresponding RCA block. If AOI gate is used in skip logic next skip logic should use OAI gates. These gates are alternatively used because of their inverting function. The critical path of CI-CSKA includes first RCA bloc k then all the skip logic and the last incrementation block. In the case of conventional carry skip adder critical path contain all RCA block and multiplexer logic. In CI-CSKA adder less number of gates are used in the critical path than the conventional one.

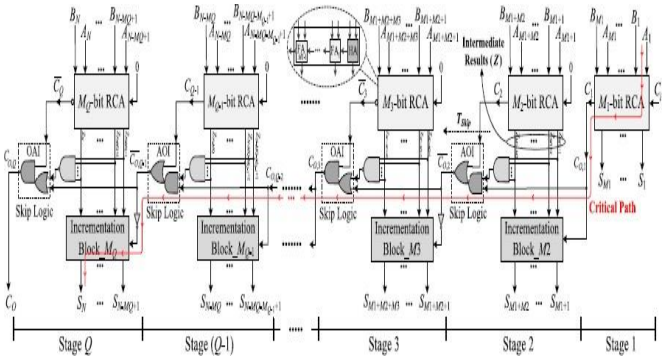

Figure 4: Structure of CI-CSKA

Figure 4 represents structure of CI-CSKA obtained by combining the concatenation and the incrementation with the Conventional CSKA structure. Carry bounce logic is used to reduce the delay in the propogation of carry. AOI and OAI gates are used to construct the carry bounce logic.

4.1 Incrementation Block

Figure 5 shows the internal block diagram of the incrementation unit, which contains a array of half adders.

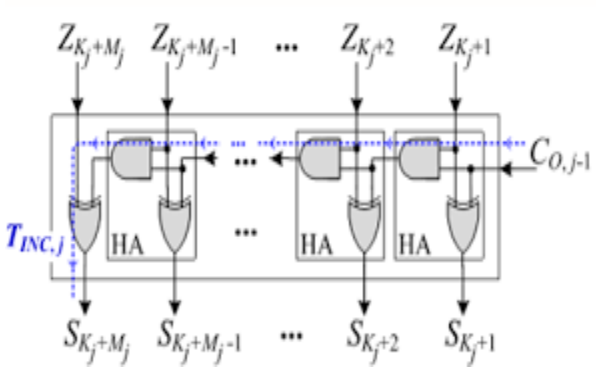

Figure 5: Block Diagram of Incrementation Block

The carry output carry of jth stage is known by the intermediate results of jth stage, carry out of preceding stage and carry out of RCA block. The carry out of RCA block equals to carry in of that stage if the product of the intermediate stages results in logic '1'. The delay in the incrementation unit is reduced further by using variable size of stages instead of fixed size of stages. The delay of CI-CSKA is improved further with parallel prefix adders in main stage.

4.2 4-Bit Multiplier Using CI-CSKA

To improve the speed and delay can be minimized by using AOI and OAI compound gates .CI-CSKA is used to design multiplier, the concatenation and incrementation blocks are used to improve the speed. The incrementation block consists of half adders. The AOI and OAI logic requires 15 transistors, whereas 2:1 multiplexer requires 20 transistors. FIR filter is widely used in Digital Signal Processing (DSP) and communication systems. Multiplication is an essential and complex building block used in the realization of FIR filters.

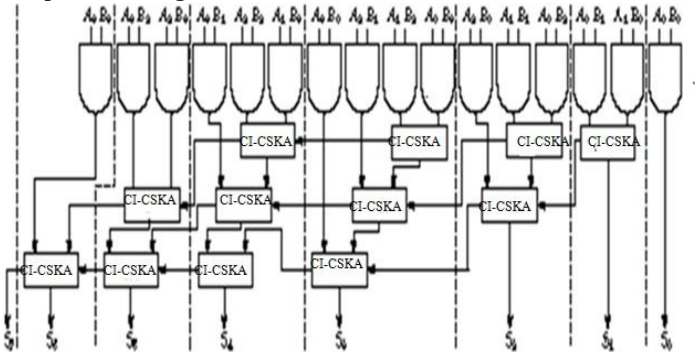

Figure 6: 4-Bit Multiplier using CI-CSKA

To improve the performance of FIR filter, an efficient multiplier showed in Figure 6 is required. The improvement in the multiplier design will make the change in the FIR filter. In depth for multipliers adder is the main system. By reducing the parameters of both adder and multiplier will get a better result in computing the filtering operations. The parameters like energy consumption and delay is calculated for carry skip adder and multiplier in 4 tap and 8-Tap FIR filter. Concatenation incrementation carry skip adder and multiplier

using CI-CSKA are implemented in 4-Tap and 8-Tap FIR filter and analysis of the implemented design is carried out.

5. RESULTS AND DISCUSSION

Each multiplier is designed individually to check its functionality with variety of inputs. Then the FIR filter is Verilog coded using the designed multipliers and are implemented in the FPGA Spartan Board.

5.1 Simulation output

The output of conventional carry skip adder is shown in Figure 7.The conventional CSKA consists of RCA block and 2:1 multiplexer. It improves on the delay of the RCA with slight effort compared to other adders.

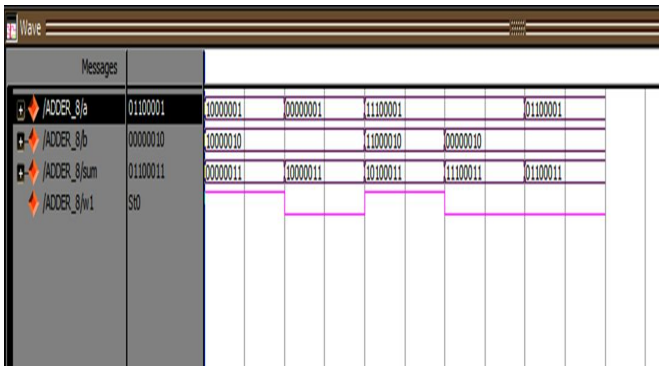

Figure 7: Output of Conventional CSKA

The Figure 7 shows the output of 8 bit Conventional carry skip adder with input as a and b of 8 bit with output sum as 8 bit and carry(w1) as 1 bit. The inputs a=10000001, 00000001, 11100001, 11100001, 01100001 and b=10000010, 10000010, 11000010, 00000010, 00000010 and the outputs are sum=00000011, 10000011, 10100011, 11100011, 01100011 and w1(carry)=1, 0, 1, 0, 0.

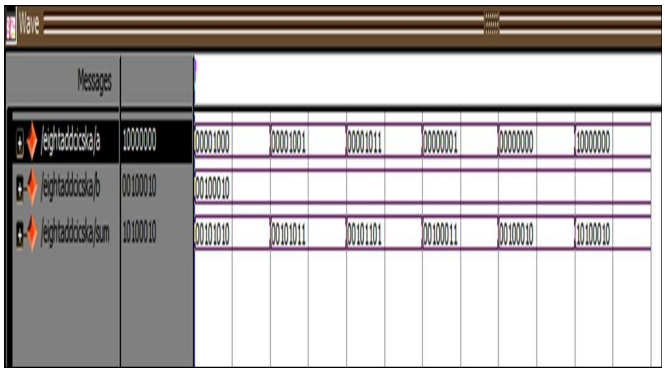

Figure 8: Output of 8 bit CI-CSKA

The Figure 8 shows the output of 8 bit Concatenation incrementation carry skip adder with a and b of 8 bits and the output with the sum of 8 bits. The inputs are a=00001000, 00001001, 00001011, 00000001, 00000000, 10000000 and b=00100010, 00100010, 00100010, 00100010, 00100010, 00100010 and output sum=00101010, 00101000, 00101101, 00100011, 00100010, 10100010.

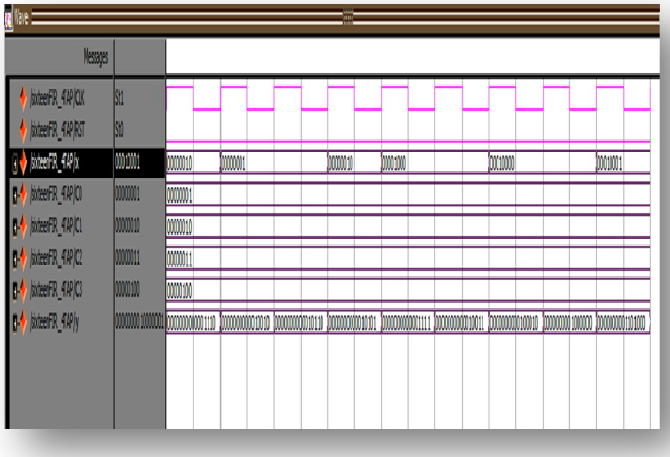

Figure 9: Output of FIR filter using 8 bit conventional CSKA and normal multiplier

The Figure 9 shows the output of FIR filter using conventional CSKA and normal multiplier. The inputs are CLK, RST, x, C0, C1, C2, C3 and output is y. The inputs are x=00000010, 00000001, 00000001, 00000010 and C0=00000001, C1=00000010, C2=00000011, C3=00000100 and y=0000000000001111 respectively.

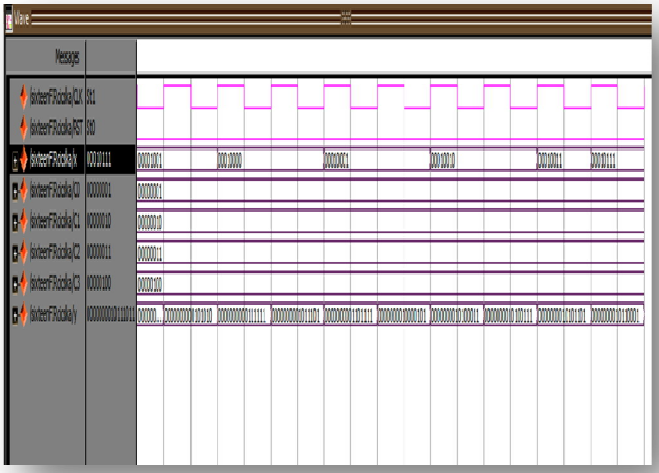

Figure 10: Output of FIR filter using 8 bit CI-CSKA and CI-CSKA Multiplier

The Figure 10 shows the output of FIR filter using CI-CSKA and multiplier. The inputs are CLK, RST, x, C0, C1, C2, C3 and output is y. The inputs are x=00010000, 00010000, 00010001, 00010001 and C0=00000001, C1=00000010, C2=00000011, C3=00000100 and y=0000000010000101 respectively.

Table 1: Comparison of Parameters among 4 Tap FIR Filter

Parameters	FIR Filter using Conventional CSKA	FIR Filter using CI-CSKA
Number of Slice LUTs (out of 19200)	108	45
Number used as Logic (out of 19200)	108	45
Maximum combinational path delay (in ns)	8.467	7.438
Clock cycle	5	5
Power Consumption (mW)	277	273

The Table 1 shows the comparison of parameters of conventional CSKA and normal multiplier with CI-CSKA and CI-CSKA Multiplier. The parameters are number of slice LUTs, number used as logic, Maximum combinational path delay and clock cycle.

The number of slice LUT in FIR filter using CI-CSKA adder and CI-CSKA multiplier is reduced by 58.33 % compared to FIR filter using conventional CSKA adder and normal multiplier. The maximum combinational path delay in FIR filter using CI-CSKA adder and CI-CSKA multiplier is reduced to 12.15 % compared to FIR filter using conventional CSKA adder and normal multiplier, so speed increases. The power consumption of 4 tap filter using CI-CSKA adder and CI-CSKA multiplier consumes less power compared to 4 tap filter using conventional adder and multiplier.

Table 2: Comparison of Parameters among 8-Tap FIR Filter

Parameters	FIR Filter using Conventional CSKA	FIR Filter using CI-CSKA
Number of Slice LUTs (out of 19200)	585	245
Number used as Logic (out of 19200)	585	245
Maximum combinational path delay (in ns)	17.954	17.315
Clock cycle	5	5
Power Consumption (mW)	328	303

The Table 2 shows the comparison of parameters of conventional CSKA and normal multiplier with CI-CSKA and CI-CSKA Multiplier. The parameters are number of slice LUTs, number used as logic, Maximum combinational path delay and clock cycle.

The number of slice LUT in FIR filter using CI-CSKA adder and CI-CSKA multiplier is reduced by 58.11 % compared to FIR filter using conventional CSKA adder and normal multiplier. The maximum combinational path delay in FIR filter using CI-CSKA adder and CI-CSKA multiplier is reduced to 3.56 % compared to FIR filter using conventional CSKA adder and normal multiplier, so speed increases. The power consumption of 8 tap filter using CI-CSKA adder and CI-CSKA multiplier is reduced by 7.6% power compared to 8 tap filter using conventional adder and conventional multiplier.

6. CONCLUSION

Concatenation Incrementation Carry Skip Adder is designed to improve the speed and to reduce the area requirement and power consumption. Here CI-CSKA adder, multiplier are used to implement FIR filter. The area of the 4-Tap FIR filter using CI-CSKA adder and multiplier is reduced by 58.33% compared with Conventional CSKA adder and multiplier. The delay of FIR filter is reduced to 12.15% compared with Conventional CSKA. The area of 8-Tap FIR filter using 8 bit CI CSKA adder and multiplier is reduced by 58.11% compared with conventional 8 bit CSKA adder and multiplier. The delay of FIR filter is reduced to 3.56% compared with conventional 8 bit CSKA.

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