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Design and Analysis of Braun Multiplier Using CMOS/GDI Technique for Signal Processing

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ABSTRACT

Efficient arithmetic circuits are needed for cost effective and computation intense signal processing applications. Electronic appliances such as pagers, notebook computers and laptops demands high reliable and portable circuits. With the advent of high performance chips, power dissipation has gained its importance for efficient chip design. The need to explore efficient design techniques has increased to achieve high throughput and reduced power dissipation. Addition is an obligatory and crucial arithmetic operation used in application specific and general purpose systems. This paper discusses the design of efficient adder and its implementation in Braun multiplier using different logic styles like Gate Diffusion Input (GDI) logic and Complementary Metal Oxide Semiconductor (CMOS). The design is implemented in Cadence Virtuoso tool for 45 nm technological node. The GDI logic style reduces the delay of Braun multiplier by 42.38% with power optimization compared with CMOS logic style.

Key words: Braun Multiplier, Kogge Stone Adder, GDI, CMOS, Digital Filter

1. INTRODUCTION

Arithmetic circuits are extensively used in Very Large Scale Integration (VLSI), Signal Processing and video processing applications. The current cutting-edge technologies pay the way for the end user to improve the flexibility and make the device portable. Arithmetic circuits play a vital role since performance metrics like die-area, speed of operation and power dissipation depend on the efficiency of the data path elements. The CMOS technology is used to optimize the performance of the logic circuit. As the feature size of the CMOS technology continues to scale down, leakage power has become an ever-increasing important part of the total power consumption of a chip. A reduction in the transistor count will have a drastic influence in the performance of the VLSI circuits. The reduction in the transistor size is much essential to increase the chip density. But the scaling of transistor leads to short channel effects [1]. The dynamic power of the circuit depends on frequency of operation and activity factor [2].The delay reduction can be obtained due to less no of interconnections and reduction the node capacitance. In GDI technique the voltage drop across the N-channel is reduced which in turn reduces the power consumption of the transistor [3]. The GDI logic helps to the reduce the transistor count and allows to obtain the reduction in power consumption.

2. RELATED WORKS

Multipliers play an important role in today's digital signal processing. As the technology improves over a period of time the need of efficient multiplier attract its significance which offer reduced power consumption with optimized speed for VLSI implementation. The transistor count is reduced by 8T full adder to improve the performance [4]. The adder performance has huge impact on the optimization of the multiplier [5]. Braun multiplier is the simplest parallel multiplier, with optimized dynamic range and throughput compare to traditional multipliers [6]. [7] Leakage power increases when scaling is performed to increase the chip density. [8] Improves the Area Delay Product (ADP) and Power Delay Product (PDP) by decreasing the transistor count of adder elements. [9] Reduced the sub threshold leakage current intern reduces the leakage power using 8T cell design. [10] To optimize the threshold voltage the substrate bias

voltage of MOS transistor is controlled. [11] Proposed inner gate engineered Metal Oxide Semiconductor Field Effect Transistor (MOSFET) to reduce the leakage current in turn reduce the power consumption of the transistor. In Sub micron CMOS technology temperature drift plays the major role in designing efficient systems [12]. The MOSFET transistor switches are not able to operate at high voltages even the it has advantage in terms of speed and transistor size [13]. The power efficient memory cell is implemented using GDI logic [14].[15] Designed a CMOS invertor with second function to reduce the total number of gates.[16] designed and simulated CMOS logic to obtain high fan out and less delay circuits. [17] Implemented Braun multiplier using various full adders with different transistor count to obtain high speed circuits at the expense of increased in the chip area. [18] Utilized parallel adders to improve the speed of an arithmetic circuit. The conventional Braun multiplier will have ripple carry adder at the final addition stage. It is replaced by Kogge stone adder with 14T XOR and 12T XOR gate to decreases the delay [19].The multiplier like Braun multiplier, Vedic multiplier and Baugh Wooley multiplier using Kogge stone adder is implemented to optimist the delay. The Braun multiplier outperforms other multipliers in terms of throughput [20].

The high speed Kogge stone adder of various bits is designed and simulated using Xilinx ISE tool. The result shows the Kogge stone adder outperformed the other conventional adders in terms of speed with increase in die area [21]. The power consumption and transistor count can be reduced by GDI technique [22].[23] Designed and implemented Kogge stone adder using CMOS and GDI logic and simulated using Cadence design suite for 180nm technology. The results show that the Kogge stone adder designed using GDI logic consumes less no of transistor. [24] Compared the performance of CMOS and GDI logic styles. [25] Designed 64-bit Kogge stone adder and simulated using Mentor graphics EDA tool in 130nm technological node. Due to less fan-out and minimum logic depth Kogge stone adder designed using GDI technique has higher throughput. [26] Using faster adders like carry select, carry save and Kogge stone adder designed multiplier to improve the performance. [27] Designed a full adder circuit based on GDI and transmission gate technique to optimize the power dissipation. [28] Optimized the full adder using GDI technique. The simulation is done using CADENCE tool at 45nm technology reveals an optimization in terms of power dissipation

3. BRAUN MULTIPLIER

Braun multiplier saves an array of carry to optimize the speed. The structure comprises of cluster of AND gates and adders arranged in the iterative way. It is called as non-additive multipliers. A z*z bit Braun multiplier can be planned with (z-1) adders and z^2 AND gate as shown in Figure 1. In parallel with AND gate each product term is generated. The partial product at a particular row is added with previously generated sum of partial products.

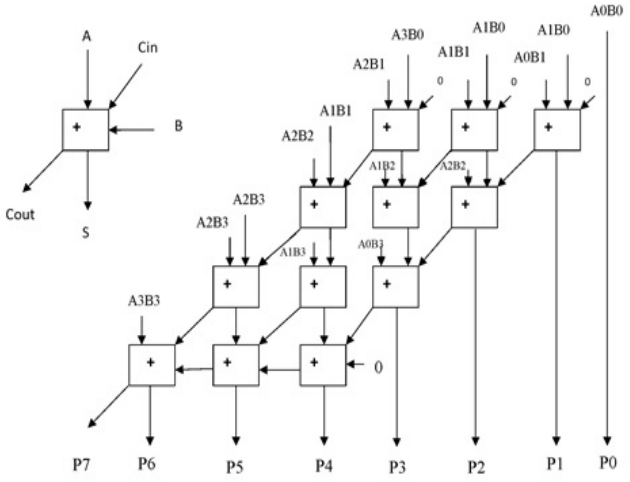

Figure 1: Braun Multiplier

With the generated sum has to be added with one bit shifted carry out. The Carry Save Adder performs the carry out shifting operation and final stage addition to obtain the final partial product term is carried by Ripple carry adder (RCA). For less than 16 bits these multiplier optimize the circuit in terms of speed, die area and power consumption. The delay depends on the Full Adder and RCA adder in the last stage. The power and area can be reduced by using bypassing techniques like row bypassing and column bypassing techniques. The modified adder cell in two-dimensional bypassing consists of a FA, tri-state buffers, 2-to-1 mux and AND gate at the carry output of FA as represented in Figure 2.

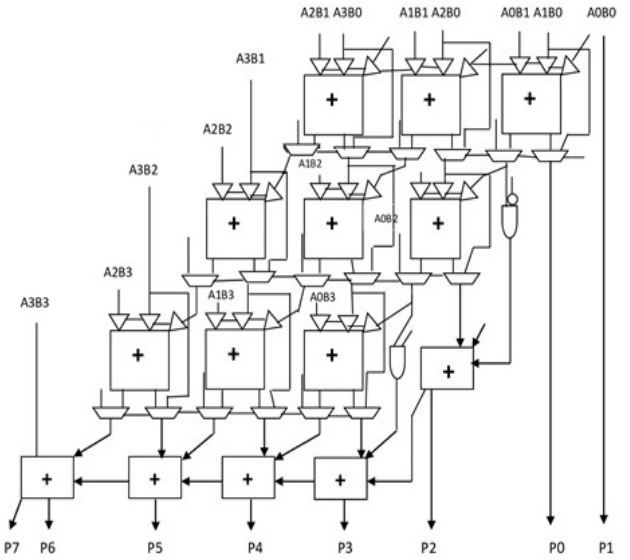

Figure 2: 4*4 Bypassing Braun Multiplier

4. IMPLEMENTATION OF BRAUN MULTIPLIER USING CMOS & GDI TECHNIQUE

To verify the performance of the Braun multiplier it is implemented in Cadence Virtuoso tool for 45 nm technology The GDI logic and CMOS logic for different components are implemented.

4.1 Inverter

The inverter is the fundamental gates in electronics. It consists of a PMOS and NMOS connected as shown in Figure 3. It produces the output which is exact inverse of input. The circuitry of inverter while designed using CMOS & GDI technique is unique. The no of transistor required for implementation of inverter is 2.

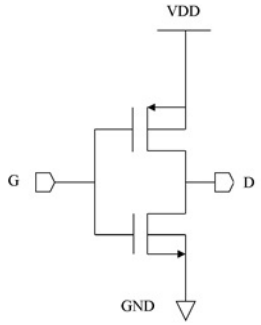

Figure 3: Inverter

4.2 AND Gate

The AND gate is a basic digital logic gate that implements logical conjunction. A logical high output is generated when the applied inputs are all high value even if one input value is low logic then it gives logic low output. A two input AND gate is implemented using CMOS and GDI logic. The total number of transistor required to implement two input AND gate is 6 using CMOS logic and 2 when implemented using GDI logic. The Figure 4 shows the logical diagram for AND gate using CMOS and GDI styles.

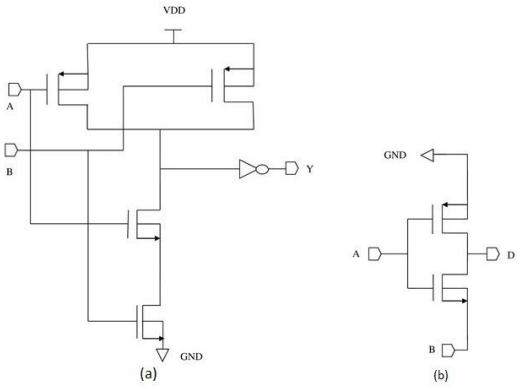

Figure 4: AND Gate Using a) CMOS b) GDI

4.3 OR Gate

The OR gate implements logical disjunction. The OR gate will produce logic low only when the applied all input value is low. The OR gate will be used to find the logic low value among the applied input values. The number of PMOS and NMOS transistor required implementing two inputs OR gate is 6 and 2 for CMOS and GDI logic respectively. Figure 5 represents CMOS and GDI two input OR gate.

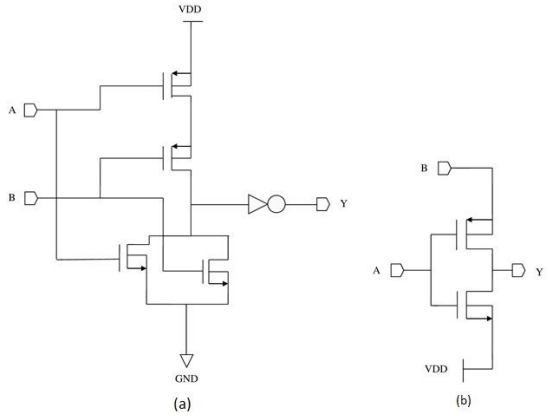

Figure 5: OR Gate Using a) CMOS b) GDI

4.4 EXOR Gate

The Exclusive OR (EXOR) gate produces high output when the applied numbers of true inputs are odd. The modulo-2 addition will be performed by EXOR gate. The total no of PMOS required implementing EXOR gate is 7 for CMOS and 2 for GDI and the NMOS required is 7 and 2 respectively. Figure 6 shows the EXOR gate implementation using CMOS and GDI logic.

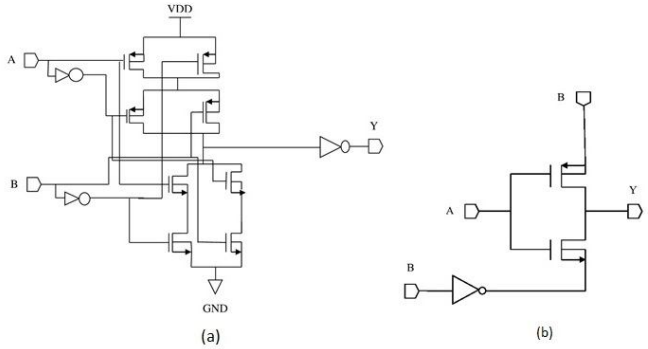

Figure 6: EXOR Gate Using a) CMOS b) GDI

4.5 Multiplexer

Multiplexer (MUX) is a device that permits the digital signal from various sources and routed it onto a single line for

transmission. A multiplexer of 2^n inputs has ⌈n⌉ select lines, which decides which input line has to be transmitted to the output. Figure 7 shows the MUX architecture design. The MUX can be designed by using 12 MOSFETs in CMOS logic, in which 6 PMOS, 6 NMOS are used, whereas GDI logic requires 1 PMOS and 1 NMOS to implement.

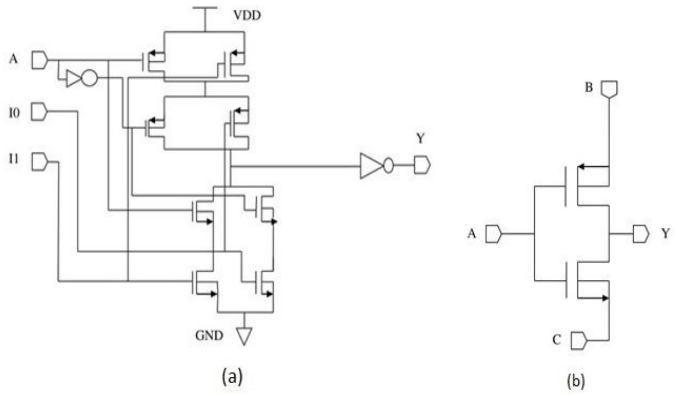

Figure 7: MUX Architecture Using a) CMOS b) GDI

4.6 Full Adder

The full-adder circuit adds two input bits (A, B) with the input carry(C). It outputs two one-bit binary numbers, sum (S) and carry (C1). The full adder circuit is shown in Figure 8. The full-adder is usually a component in a cascade of adders, which add 4, 8, 16, 32 bits of binary numbers. The full adder shown in Figure 8 consist of AND, OR and EXOR gates. These gates are implemented using CMOS and GDI technique. When a full adder is implemented using CMOS logic the total no of transistor required is 46. The number of transistor need is 14 while implemented in GDI logic.

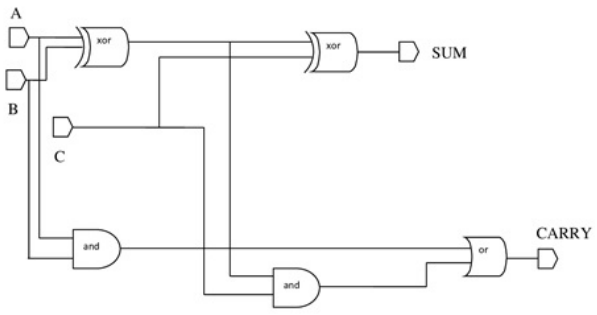

Figure 8: Full Adder Circuit

4.7 Kogge Stone Adder

To obtain the high performance arithmetic circuits Kogge stone Adder is used. The Kogge stone adder is a 4-bit adder in which the number of inputs is 8 with a carry bit, which are summed to get 4 sum bits and 1 final carry out bit. It consists of pre-processing, carry generation and post processing stage. Figure 9 represents the logical diagram of Kogge stone Adder.

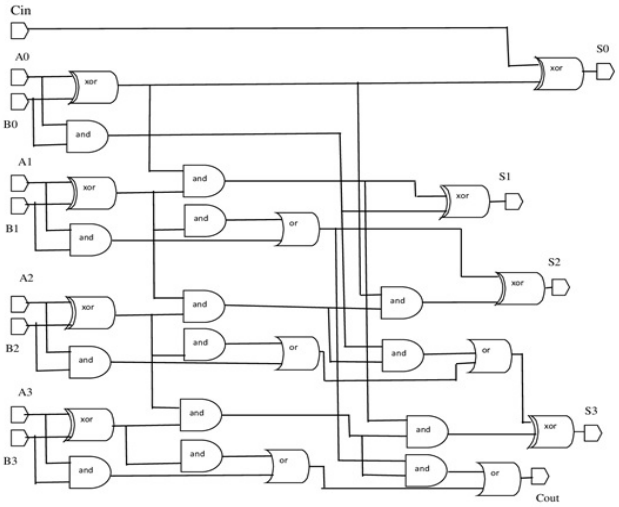

Figure 9: Kogge Stone Adder

Figure 10 shows the output wave form sum and carry bits for the given input condition. The bits a_0, b_0, c_{in} are added and the corresponding sum is obtained. Whereas, the carry out generated is sent to next stage as c_{in}. Similarly for a_1, b_1, a_2, b_2, a_3, b_3 the similar performance is carried and the final carry is taken as c_{out}.

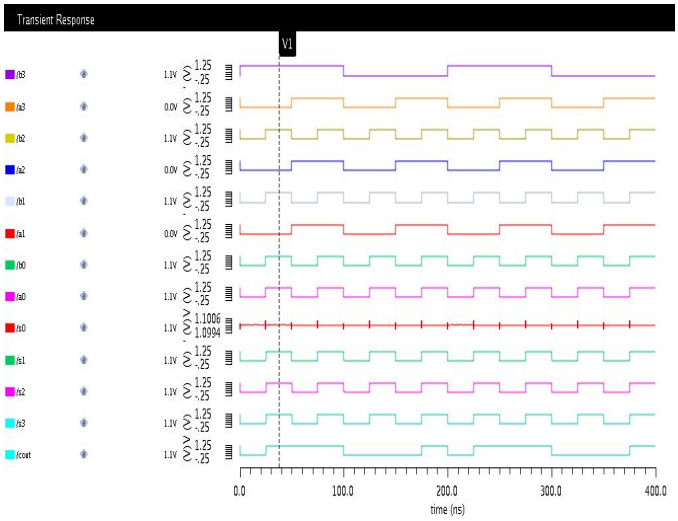

Figure 10: Kogge Stone Adder Output Waveform

Table 1 show the transistor count of Kogge stone adder designed using CMOS and GDI logic. The number of gates required to design a Kogge Stone adder is 14 AND gate + 5 OR gate + 8 EXOR. The transistor count of the Kogge Stone adder is 226 when designed using CMOS logic. While design the Kogge Stone adder using GDI technique the transistor count is 82.

Table 1: Transistor Count of Kogge Stone Adder

Adder	Gate type	Using CMOS	Using GDI
		Transistor Count	Transistor Count
Kogge stone Adder	AND	84	56
	OR	30	10
	EXOR	112	16

4.8 Braun Multiplier

In Braun multiplier parallel computation of the partial products are done and the end result will be obtained by collection of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. Figure 11 shows 4*4 Braun multiplier design. The inputs are applied to the AND gates and the output of AND gate is applied to the adder cells. The adder cells gives two outputs sum and carry which are propagated to next stage as inputs.

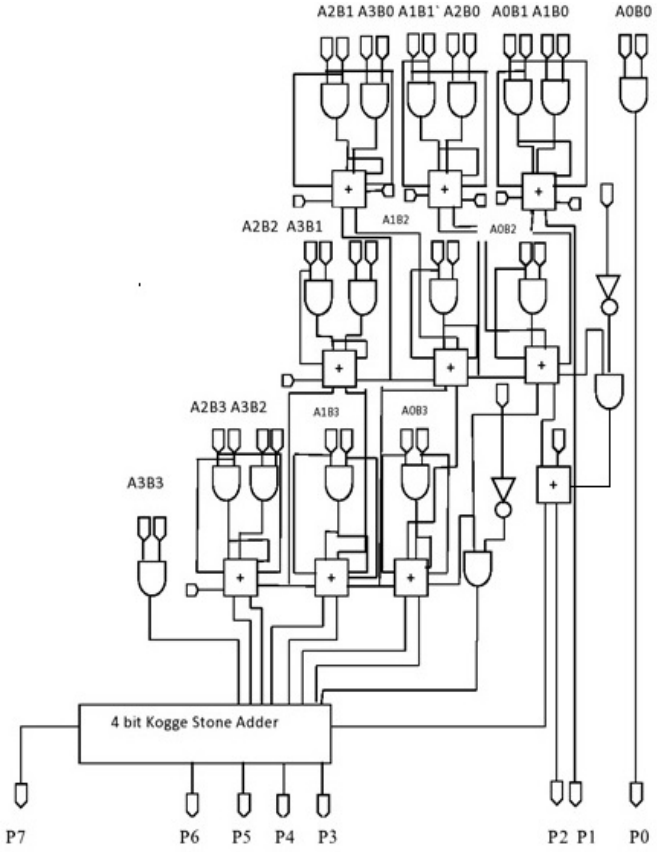

Figure 11: 4*4 Braun multiplier using Kogge Stone Adder

Here, all the bits from p0 to p6 are obtained by adding the respective terms in those columns, whereas p7 is the final propagation carry bit. If in any cases we get 0 bits in product of two binary numbers, all those terms are directly bypassed and the product output is generated. Kogge Stone adder is used at the final addition stage to optimize the power and critical delay. Figure 12 shows the waveforms of the Braun multiplier using Kogge stone adder. The circuit is simulated for an input conditions A = 1101 and B =0110, the final output values are 01001110 as shown in Figure 12. Similarly random inputs are applied to verify the functionality of the circuit. The Braun multiplier is designed using CMOS logic style and GDI logic style and the output is verified.

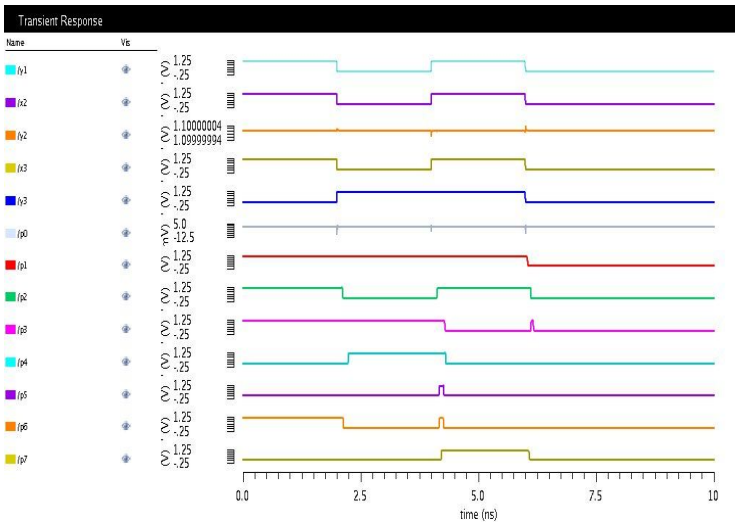

Figure 12: Braun multiplier Output waveform

Figure 13 to 16 shows the power and critical delay of the Braun Multiplier implemented using Kogge stone adder in CMOS and GDI logic.

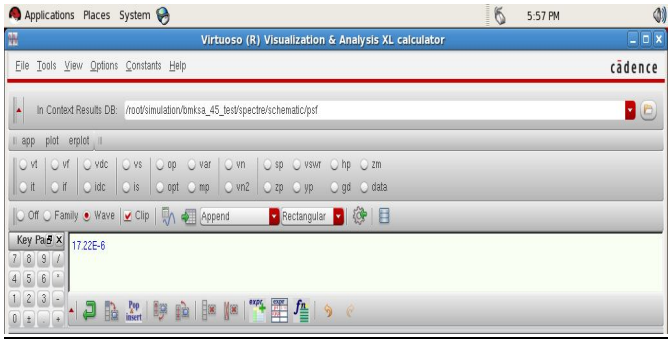

Figure 13: Average Power of Braun multiplier designed using CMOS Logic

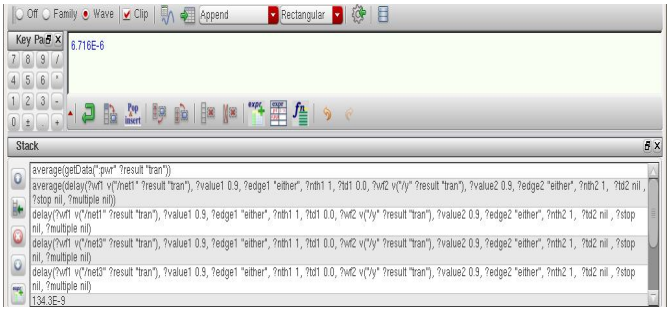

Figure 14: Average Power of Braun multiplier designed using GDI Logic

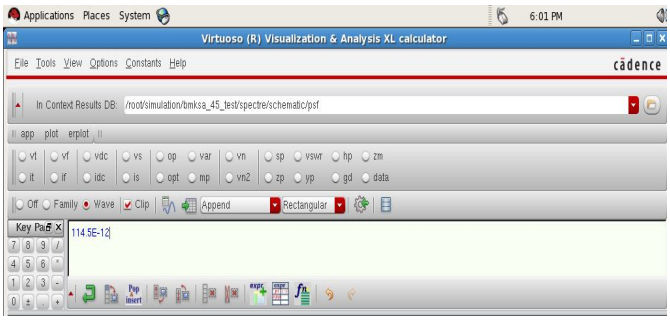

Figure 15: Dealy of Braun multiplier designed using CMOS Logic

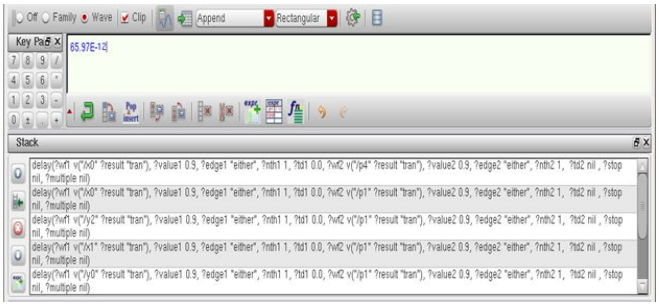

Figure 16: Dealy of Braun multiplier designed using GDI Logic

5. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

The Braun multiplier is implemented in 45nm technology in Cadence Virtuoso tool. The circuit schematics designed and are simulated for functional verification. The Braun multiplier is designed using ripple carry adder, 14 transistor adder circuit, Kogge stone adder for both CMOS/GDI logic. The power, delay and Power delay product (PDP) is shown in the Table 2. From the reports, it is observed that the Braun multiplier designed using ripple carry adder and 14 transistor adder consumes power of 10.33 µW and 20.01 µW respectively. It can observed from the table that power consumption of the Braun multiplier designed using the Kogge stone adder in GDI logic is reduced by 34.99% and 61% compared with Braun multiplier designed using ripple carry adder and Kogge stone adder in CMOS logic due to the minimization of the switching activity and leakage current reduction.

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Table 2: Performance Comparisons of Braun Multiplier

Performance Metrics Multiplier Design	Power (µW)	Delay (ps)	PDP (µW-ps)
Using ripple carry adder in CMOS	10.33	143.9	1486.487
Using 14 transistor adder in CMOS	20.01	34.45	689.344
Using kogge stone adder in CMOS	17.22	114.5	1971.690
Using kogge stone adder in GDI	6.716	65.97	443.054

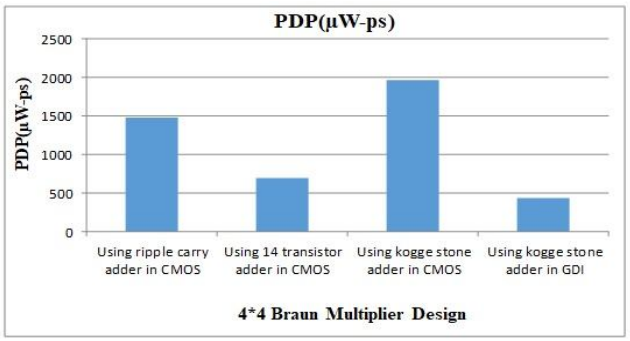

Figure 17: PDP of 4*4 Braun Multiplier

The delay of the Braun multiplier designed by Kogge stone adder in GDI logic is reduced by 42.38 % compared with CMOS logic. This is due to the minimization of the critical path delay. The reduced power dissipation demonstrates the PDP reduction as shown in Table 2.

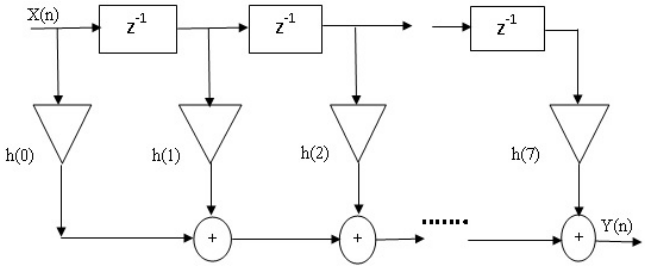

Figure 18: Direct Form I FIR Filter Structure

A plot of power delay product for 4*4 Braun multiplier designed using different logic for 45 nm technological nodes is shown in Figure 17. The performance of the Braun multiplier designed using different logic styles is verified by implementing in 8 tap 8-bit coefficient band pass filter. Direct form 1 FIR filter is represented in Figure 18. The band pass filter described using Verilog-HDL is simulated in Xilinx ISE tool and its functional verification is done. The FIR filter module is synthesized using Cadence Virtuoso tool with respect to 45 nm technological library.

Table 3: Performance Estimates of Digital Filter Implemented Using Braun Multiplier

Digital Filter Design	Power (µW)	Delay (ps)	PDP (µW- ps)
Using 8*8 Braun multiplier designed using ripple carry adder in CMOS	109.2	569.8	62197
Using 8*8 Braun multiplier designed using 14 transistor adder in CMOS	208.7	135.1	28184
Using 8*8 Braun multiplier designed using kogge stone adder in CMOS	179.3	445.4	79843
Using 8*8 Braun multiplier designed using kogge stone adder in GDI	69.7	253.9	17706

The band pass filter designed using Braun multiplier with various logic styles are designed for comparison. The delay, power dissipation and PDP extracted from the simulation analysis are given in Table 3. Band pass filter using Braun multiplier designed using kogge stone adder in GDI logic style reveal a power and PDP reduction of 36.14% and 37.17% compared to the best of design used for comparison

6. CONCLUSION

This Braun Multiplier is implemented with CMOS and GDI logic. The Braun multiplier using different adder is implemented in 45 nm technology using Cadence Virtuoso tool. Braun multiplier designed using Kogge stone adder in GDI technique achieves a better performance with the average power value of 6.71µw. The reduced power consumption reflected in its PDP value. Band pass filter when implemented using Braun multiplier with kogge stone adder in GDI reveals a PDP reduction of 37.17% compared with other techniques. From the results, it is evident that Braun Multiplier implemented using Kogge Stone Adder in GDI technique reveals reduced critical path delay with minimized power consumption which suits for efficient DSP applications.

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