ISSN 2347 - 3983
Volume 8. No. 7, July 2020
International Journal of Emerging Trends in Engineering Research
Available Online at http://www.warse.org/IJETER/static/pdf/file/ijeter32872020.pdf
https://doi.org/10.30534/ijeter/2020/32872020

Energy Efficient Arithmetic Full Adders using various Technology Nodes

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ABSTRACT

We observe many CMOS circuits that consume very high power in recent times. In addition to that of the CMOS family, many logic styles were improved to increase the performance of full adder circuit. Designing existing full adder logic styles in both 90nm and 130nm and compared with proposed logic style. To through the power item, introducing energy efficient full adder with 10 transistors in both 90nm and 130nm technology. All the full adders are planned to investigate in terms of power. The results show that all the models proposed are energy efficient. Finally, power consumed by the full adder cell in comparison with the old designs has been achieved. For meeting the demands of fast progressive era of electronics most efficient full adder structure is developed.

Key words: Full adder, Power, Transistor, Technology Nodes.

1. INTRODUCTION

Modern electronic devices are today an indivisible part of daily life. Digital circuits, for example, a large section of electronic systems are comprised of microprocessor, communicating devices and signal processors. VLSI Designers have different options in different design stages to reduce power dissipation. For example, by manufacturing technology, the supply voltage can be decreased; circuit layout is dynamically through the level of the device [1-3].

Today's developers face more obstacles as rapidly evolving technologies. Portable electronics demand and popularity forces developers to aim for reducing power, to increase speed and make energy efficient device, and greater reliability. For developing energy efficient system power and number of transistors are the key factors. A digital circuit which performs arithmetic operations is the major power consumption in electronic device; this is due to full adder designing and the block diagram shown in Figure 1.

In this work, power comparison between inbuilt designs and hybrid styles in 90nm and 130 nm technology is implemented, also the full adder with reduced number of transistors, to achieve reduced overall delays and outputs, respectively, and to transfer fewer logic types of transistor power to diminish power consumption. The resulting full-adder displays more flexibility in power utilization and setback compared to previously reported low-power arithmetic modules as good candidates.

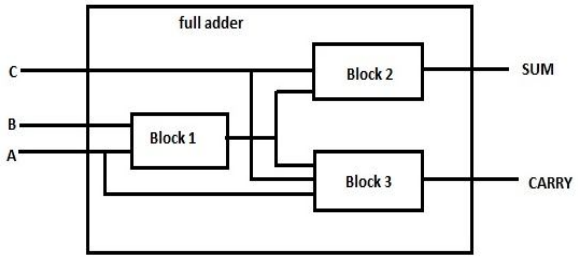

Figure 1: Full adder block diagram.

As compared to CMOS, transmission gate, pass transistor and other logic styles GDI uses less transistors and provide effective output. GDI has less transistors, low power dissipation and low delay. The major drawback of GDI is on the voltage regulations in the output point.

The proposed new GDI full adder overcomes all the drawbacks of the previous models. The wished-for adder is compared with the earlier models. The proposed full adder is strictly investigated in both 90nm and 130nm technology in high end tool.

This work mainly comprises in three sections. The first section gives details about the previous full adder designs and their power consumptions. The second section mainly comprises on the comparison between the GDI and previous full adder designs and final section comprises about the results and analysis.

2.LITERATURE SURVEY

Generally Full adder is used in Processors and Computers in Arithmetic and logical unit for the addition or subtraction or multiplication of two bits. The Full Adder is also used in processors for other purposes like Address addition and increment or decrement operations. Generally the full adder is made of with two modules that is XOR/XNOR and Multiplexer [1]. In full adder the majority of the Power consumption is carried out by XOR/XNOR gates. To reduce the power consumption in full adder XOR/XNOR gates must be optimised. The power consumption of the Transmission gate and pass transistor logic is less but the pass transistor doesn't allow the weak judgment 0 and strong judgment 1 through it. In Transmission gate logic the number of transistor are more compared to the other logics, if there are more transistors then the delay will be more, if delay is high then the resulting PDP will be more. The power consumption is reduced and also it will pass strong logic 1 and weak 0. Information about the Differential Full adders and the full adder cell characterization is observed [4]. How to implement multiplexers in different logic styles and which logic style provides less power consummated full adder is made of with the arithmetic gates and the multiplexer [5]. It provides the less delay and the speed [6-12]. The delay and speed depends on the transistors count, if the transistors are less than the delay will be less.

3. EXISTING FULL ADDER CHARACTERIZATION

3.1 CMOS based full adder

There are many logic styles to implement full adder circuit design. It consists of PMOS and NMOS. It is a technology for constructing or designing low power circuits, which can also be called as small amount of memory in computers. If any one of the inputs is high then carry is 0, whereas sum will be 1. If two inputs are elevated then carry is 1, while sum is 0. This is the basic CMOS logic for full adder circuit design and the same was shown in Figure 2.

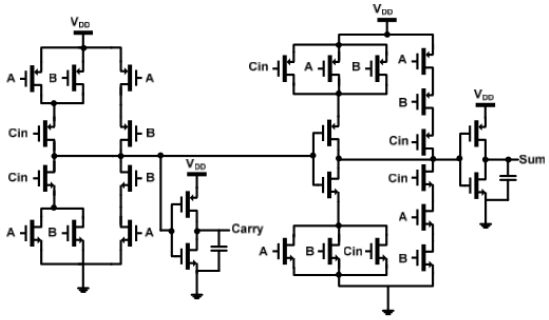

Figure 2: CMOS logic based full adder circuit.

We observed that implementation of CMOS based full adder has three inputs A, B, and C_{in} as well as two outputs as Sum and Carry.

The main drawback of the circuit is the chip area which is large in CMOS logic. It includes large power consumption and also high input data. PMOS has high mobility compared to NMOS in CMOS logic based full adder circuit. The transistors at the output stage are connected in series, so the driving capacity of the circuit will decrease accordingly. The only drawback is it is a straightforward circuit and gives a full voltage swing which is the main in complex design circuits. It gives an improved output rather than that of the transistors count and size.

3.2 Transmission gate based full adder

It has three inputs source, NMOS gate, PMOS gate and one output drain. Driving capability is lower compared to that of other logic designs. Consumption of power is high in transmission gate logic compare to that of CMOS logic. Voltage at output point can be succeeded by this logic style. The major drawback is transistors count is a smaller amount to that of CMOS logic style. So, it is simpler than other logic styles.

3.3 Pass transistor logic based full adder

Pass transistor logic (PTL) in electronics defines many logic families that are used in the development of integrated circuits. Through removing redundant transistors, the volume of the transistors will be reduced. The inputs are connected to gate terminal in other logic styles, while in pass transistor logic the inputs are connected to drain or source terminal [4].

The threshold voltage fall through the NMOS transistors requires preserving the rate of output voltage. Minimum 17 Transistors are required to build this logical full adder.

3.4 Double pass transistor logic based full adder

Generally, in logic design input supply is not a strong voltage. So, some buffers should be used to get a strong input voltage in double pass transistor logic. All these problems are because of nmos transistor which cannot pass voltage correctly. To overcome this situation complimentary PMOS is connected parallel to that of nmos for strong voltage supply.

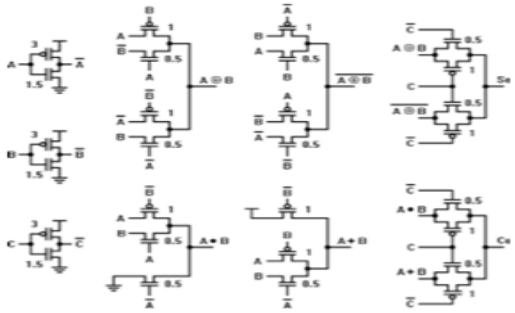

Figure 3: Double pass transistor based full adder

The figure 3 represents the full adder accomplishment in Double pass transistor logic. Advantages are it improves gate rate without escalating the input capacitance. It gives the circuit performance at reduced supply voltage. Drawbacks are it doesn't perform full swing operations [1]. The main drawback of DPL is transistor handling is high. If the transistors are more the delay will be high.

3.5 Complimentary pass transistor based full adder

Advantages are it performs full swing operations. Drawbacks are rectified in DPL full adder. It also reduces the complexity of circuit which shown in Figure 4.

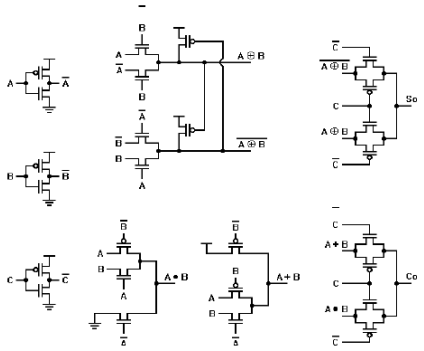

Figure 4: Complementary pass transistor based full adder

3.6 GDI

GDI is the high-flying technology to design the circuits with fewer amounts of transistors and less power dissipation. As the transistor count decreases then there will be decrease in the delay of the circuit [4]. This logic style has three terminals G, p and n i.e. one is from PMOS and other is from NMOS and output is taken from the drains of both PMOS and NMOS and is shown in Figure 5.

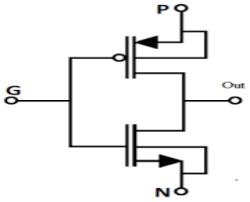

Figure 5: GDI based cell

Table 1: Operations of GDI cell

N	P	G	D	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

The modified GDI technique overcomes the drawback and produces the full swing operations. From the Table 1 when the gate is in on state the nmos is on and pmos turned off hence the nmos input passed through the output. If NMOS is judgment '0' the output will be feeble judgment '0'. If the gate is in off state (Logic '0') then PMOS is in on state hence the PMOS is passed through the output. If there is Logic '1' in the PMOS the output is a weak Logic '1'. In order to overcome this new modified GDI adder is proposed [4].

4. PROPOSED FULL ADDER

If the full adder is implemented with mux then there will be huge reduce in the gates count than other logic styles. So reducing the complex full adder and make it simple by using multiplexer. Below equations shows the derivation for outputs of full adder.

SUM =A ' (B ⊕ C) + A (B ⊕ B) ' — (1)

CARRY =A' (BC) + A (B+C) — (2)

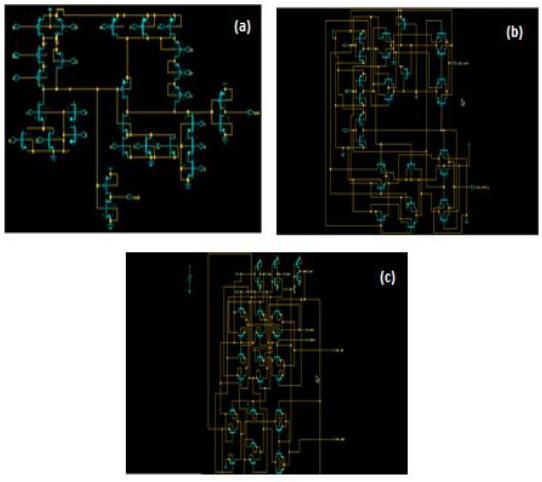

Figure 6: Designing of various full adders in 130nm technology (a) CMOS logic, (b) CPL logic and (c) DPL logic

The Figure. 6(a) shows implementation of the CMOS full adder in 130nm by using high end tool, figure 6(b) represents the CPL full adder, figure 6(c) represents the DPL full adder IN 130nm.

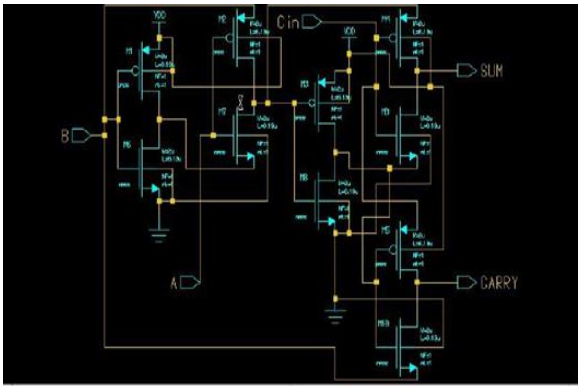

Figure 7: Schematic of modified GDI full adder in 130nm

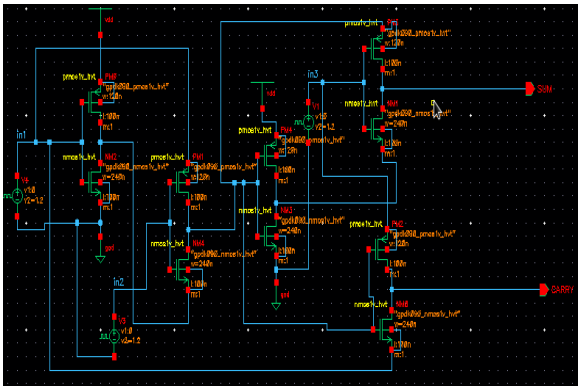

Figure 8: Schematic of modified GDI full adder in 90nm

The Figure 7 represents the customized GDI technique full adder in 130nm technology. The Figure 8 represents the customized GDI technique full adder in 90nm technology. The modified GDI full adder is power efficient than CMOS full adder but slightly higher than the GDI. The advantage of modified GDI technique full adder is full swing operations.The main difference between the 90nm and 130nm technology is transistor sizing. The transistor sizing plays a key role in power reduction. As in this modern electronic era every electronic user wants to reduce the compatibility of the circuit. So, this works comprises also the comparing of power dissipation in both 90nm and 130nm.

5. RESULTS AND DISUCUSSION

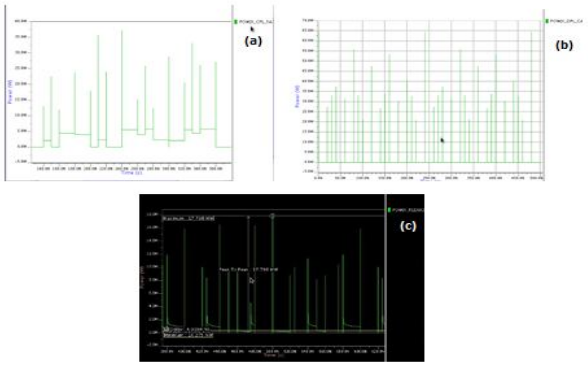

Figure 9: Various power consumptions of full adders in 130nm

Figure 9(a) explains the power utilization of CPL logic based full adder in 130nm. Figure 9(b) explains the power utilization of DPL logic using high end tool in 130nm. Figure 9(c) shows power expenditure of planned full adder in 130nm technology.

Table 2: Power consumption in 130nm

TECHNOLOGY	NUMBER OF TRANSISTORS	POWER(µW)
CMOS	28	60.9
TGL	16	63.45
DPL	28	67.0
CPL	26	37.5
PROPOSED (THIS WORK)	10	17.73

Table. 2 explains the transistors count and the power utilization in each technology. The above results are investigated in 130nm technology in high end tool.

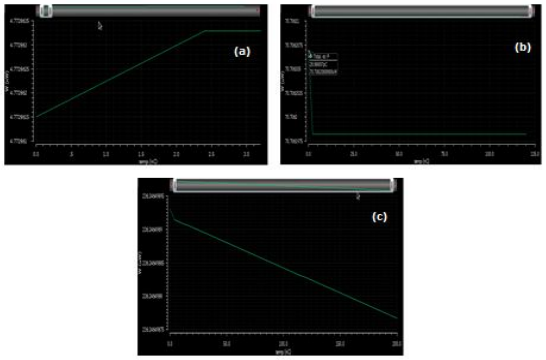

Figure 10: Various power consumptions of full adders in 90nm

Figure 10(a) explains the power utilization of CMOS based full adder in 90nm technology. Figure 10(b) shows power utilization of transmission gate full adder in 90nm technology. Figure 10(c) shows the power utilization of planned full adder technique in 90nm.

Table 3: Power consumption in 90nm

TECHNOLOGY	NUMBER OF TRANSISTORS	POWER(nW)
CMOS	28	99.31
TGL	16	34.14
PROPOSED (THIS WORK)	10	27.94

The Table 3 explains the transistors count and the power utilization in each technology. The above results are investigated in 90nm technology in high end tool.

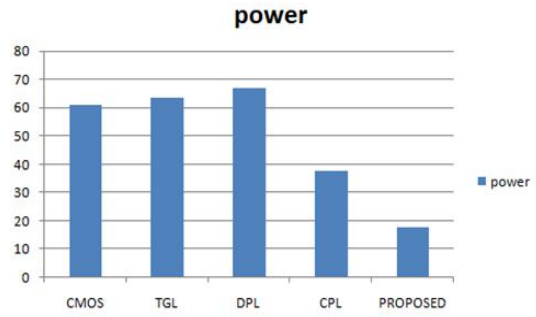

Figure 11(a): Power use of full adder in 130nm

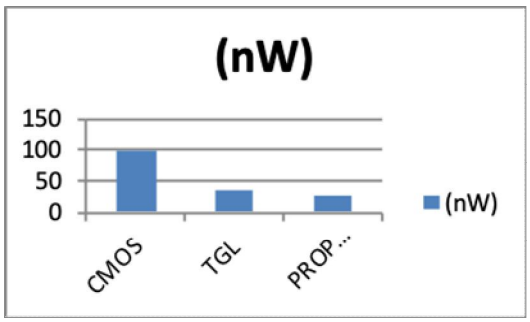

Figure 11(b): Power use of full adder in 90nm

The Figure 11(a) and 11(b) represents the power waves of different logic full adders in both 130nm and 90nm. The proposed represents the work carried out which is power efficient than other logic styles.

6. CONCLUSION

Finally, the planned design is implemented and compared with the earlier techniques. An alternate internal logic structure is implemented to model full adder cells. They were designed and compared with other efficient full adders in 90nm and 130nm technology. It is practical that the power utilization in 130nm is higher than the 90nm technology.

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