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A Review on Reversible Computing and it's applications on combinational circuits

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ABSTRACT

In this era of nanometer semiconductor nodes, the transistor scaling and voltage scaling are not any longer in line with each other, leading to the failure of the Dennard scaling. Thus, it poses a severe design challenge. Reversible computing plays a vital role in applications like low power CMOS, nanotechnology, quantum computing, optical computing, digital signal processing, cryptography, computer graphics and many more. The primary reasons for designing reversible logic are diminishing the quantum cost, profundity of the circuits and the garbage outputs. It is impossible to determine the quantum computing without implementing the reversible computation. This paper will represent the literature survey based on several papers on combinational circuits using reversible computing and also the future scope is to be discussed.

Key words: Logic circuits, Reversible logic, Garbage outputs, Quantum cost, Constant Input, Hardware Complexity.

1. INTRODUCTION:

As the transistors get smaller, the power density of those transistors remains constant so that the used power is proportional with area and this law is called as Dennard's Scaling or MOSFET scaling.
Dennard's scaling failed mainly due to the fact that supply voltage remained constant but the power densities subsequently increase on the chip. Therefore, a major quantity of on-chip resources has to stay in power-gated situation, so as to avoid thermal emergencies. In this scenario, transistor and voltage scaling don't seem to be in line with one another [1]. In recent years, reversibility assumes a major role when computations with least energy dissipation are examined. The primary reason for conspiring reversible logic is to cut back the number of reversible gates, garbage outputs, constant inputs, area, power, delay, and quantum cost and hardware complexity of the reversible circuits. In 1991, Landauer [2, 3] proposed the answer for the question that why computers use most energy. From the Thermodynamics concept, he proposed that the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where, K denotes the Boltzmann's constant and T denotes the absolute temperature at which operation is performed. This is known as the 'Landauer Principle'. A circuit is alleged to be reversible if the input is recoverable from the output. Reversible computing holds up for each forward and backward movement method in concert generates inputs from the outputs. The primitive combinable logic circuits scatter energy for all of data that's lost throughout the activity. This can be as a result of per the actual fact of second law of thermodynamics; data once lost cannot be recovered by any methods. In 1973, Bennett[4] showed that circuits built using reversible logic gates escaped the energy dissipation problem.

In the online Conference of Physics and Engineering Issues in Adiabatic/Reversible Classical Computing (October 5-9, 2020), it had been proclaimed that need for reversible computing has become widely recognized. Today's approach towards general digital computation based on standard combinational and sequential digital architectures constructed out of standard (irreversible) Boolean logic elements implemented using CMOS (complementary metal/oxide/semiconductor) transistor technology, is approaching fundamental cut-off points to additional enhancements for its energy effectiveness and power-limited performance. The final (2015) edition of the International Technology Roadmap for Semiconductors (ITRS), furthermore recent editions of its successor roadmap, the International Roadmap for Devices and Systems (IRDS), suggest that a sensible limit will be reached by round the year 2030. By the end of the CMOS roadmap, logic signal energies at the gate of a minimum-sized transistor basically cannot diminish a lot further without crossing paths of fundamental limits on efficiency and stability arising from thermal fluctuations. Even moving to "Beyond CMOS" switching devices cannot improve this situation considerably, since identical elementary thermodynamic limits still continue to apply.
Hence, there is an expanding need to investigate new fundamental standards for the designing execution of general

computing systems (at all scales from tiny embedded devices to large-scale supercomputers and data centres) in search of novel ideas for computation which will transcend the above limits that are inherent to the standard irreversible digital paradigm. The area of ideas that have been contemplated include a diversity of concepts for "physical" computing (computing that leverages fundamental physics to do computing in a very additional direct approach than in the traditional digital paradigm), including numerous analog and stochastic computing ideas likewise, quantum computing (for issues amenable to quantum speedups).

Accordingly, we see the fundamental science and designing of reversible computers as being at present a very ready area of focus for future large-scale federal research initiatives, for the following reasons:

1. The reversible computing field is absolutely fundamental for there to be any expectation of propelling ordinary general digital computing beyond the energy-efficiency limits that apply to the conventional computing paradigm, which will definitely be reached in the near future.

2. There is a spread of important foundational physical science analysis within the reversible computing field that might have the potential revolutionary impact that still must be done.

3. This field has so far been forward-looking for the industry to invest in directly, although at least one major industrial research lab is presently considering starting up a project to investigate the boundaries of computing, including reversible computing.

4. To have designs with minimal power consumption for transistors has been recently dominated by the semiconductor industry as mandated by the growing electronic industry especially dominated by cell phone. On the other hand the requirement for more dense transistors as per Moore's law continues to rise.

The 8086 microprocessors had fewer than 30,000 semiconductors, contrasted with current CPU and GPU's which comprises of billions of semiconductors prompting complex administration of cost, and power. There are billions of semiconductors on a chip; yet, those semiconductors can't be utilized all the while. This reality has had a major effect in how CPUs are planned, and this issue will just increase later on. A processor which can utilize just 5% of its transistors at some given time will fluctuate with the processor which can utilize half of its semiconductors in a few attributes, primarily timing and power [1], subsequently researchers are thinking about the utilization of reversible gates.

2. THE CONCEPT

Reversibility in computing gives the idea that the information about computational states can never be lost and be used when needed. Logical reversibility is the process in which any early stage can be recovered in computing backwards or un-computing the results. Physical reversibility is referred to no energy dissipation of heat. After Physical, logical reversibility is achieved [5]. The most prominent application of reversible computing stays in quantum computing. Quantum networks comprise of quantum logic gates; each gate performs an elementary unitary operation on one, two or more two–state quantum systems, which are called qubits. Each qubit is correspondent to the classical bit values 0 and 1. [6]
Reversible logic elements are utilized for recovering the state of inputs from the outputs. An NXN reversible network is represented as :
Iv = (I1, I2, I3, ... IN)
Ov = (O1, O2, O3, ... ON)
Where, Iv and Ov clarifies the input and output vectors respectively. Figure 1 shows the symbol of reversible logic gates with input and output vectors.

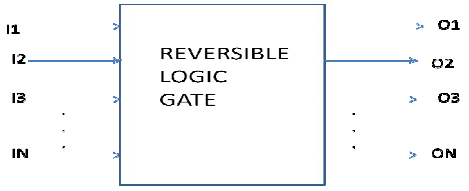

Fig. 1 represents the symbol of Reversible logic gate with input and output vectors.

3. BACKGROUND

By Moore's Law, the number of transistors will be doubled for every eighteen months. For every eighteen months, it is possible to create higher performance general purpose processors. In 1980, Toffoli[7] stated that utilizing invertible logic gates, it is feasible to create a sequential PC with zero internal power dispersal preferably. The basis of heat dissipation are as follows: Increase in the number of transistors on chip.[8], High Power dissipation leads to: Reduced time of operation, Reduced mobility and reliability, High efforts for cooling, Increasing operational costs.

Several parameters to determine the complexity and performance of circuits[9,10] are:

A. The number of reversible gates (N).

B. Constant inputs: Number of inputs which are to be maintained constant at 0 or 1 for synthesizing the given logic function.

C. Garbage output: Number of unused outputs used in the reversible gates. Garbage outputs are not avoidable as these are very essential to achieve reversibility. The

following formula which is used to deterine the relation between number of garbage outputs and constant inputs:
Input + Constant input = output + garbage output.

D. Quantum cost : Cost of the circuit with respect to the cost of a primitive gate. Some properties of quantum cost:

a. V*V = NOT
b. V*V+ = V+ *V = 1
c. V+*V+ = NOT

E. Hardware Complexity: It determines the number of logic operations in the circuit. That means number of AND, OR and EX-OR operations performed in the circuit.

F. Flexibility: It determines the universality of reversible logic gate for realizing more functions.

For achieving an optimized reversible circuit, the following points are needed to be considered:

- Minimum delay.
- Minimum garbage outputs.
- Feedbacks/Loops are not considered.

4. SOME BASIC REVERSIBLE LOGIC GATES

To implement the combinational circuits, the following functional block diagrams of some basic reversible gates like Not, Toffoli, Feynmann, Double Feynmann, Peres, Fredkin, HNG, TSG, DKG, NFT, RMUX1, TKS, BVF and TR are shown below.

The functional block diagram of 1X1 NOT Gate is illustrated in Fig. 2.

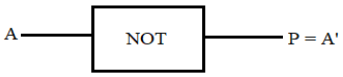

Fig. 2 shows functional block diagram of 1X1 NOT gate.

The functional block diagram of 3X3 Toffoli gate is illustrated in Fig. 3.

Fig.3 shows functional block diagram of 3X3 Toffoli gate.

The functional block diagram of 2X2 Feynmann gate is illustrated in Fig. 4..

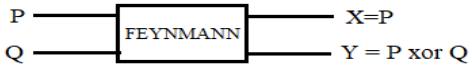

Fig.4 shows functional block diagram of 2X2 Feynmann gate.

The functional block diagram of 3X3 Double Feynmann gate is illustrated in Fig. 5.

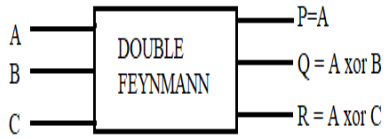

Fig.5 shows functional block diagram of 3X3 Double Feynmann gate.

The functional block diagram of 3X3 Peres gate is illustrated in Fig. 6.

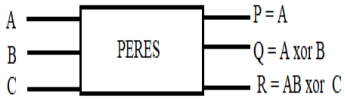

Fig.6 shows functional block diagram of 3X3 Peres gate.

The functional block diagram of 4X4 HNG gate is illustrated in Fig. 7.

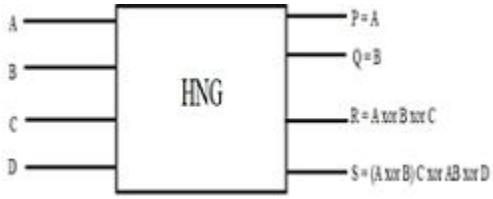

Fig.7 shows functional block diagram of 4X4 HNG gate.

The functional block diagram of 3X3 Fredkin gate is illustrated in Fig. 8.

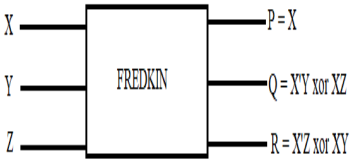

Fig.8 shows functional block diagram of 3X3 Fredkin gate.

The functional block diagram of 4X4 TSG gate is illustrated in Fig. 9.

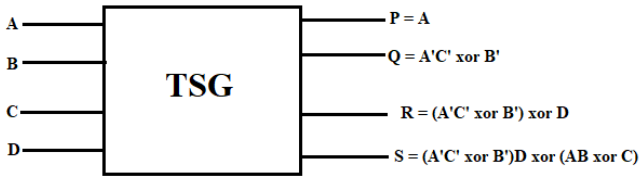

Fig.9 shows functional block diagram of 4X4 TSG gate.

The functional block diagram of 4X4 DKG gate is illustrated in Fig. 10.

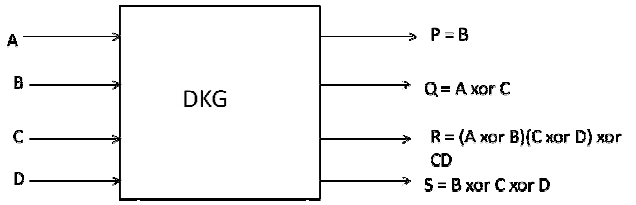

Fig. 10 shows functional block diagram of 4X4 DKG gate.

The functional block diagram of 3X3 NFT gate is illustrated in Fig. 11.

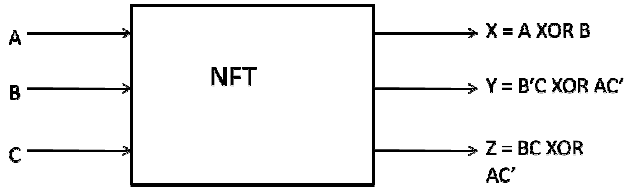

Fig. 11 shows functional block diagram of 3X3 NFT gate.

The functional block diagram of 3X3 RMUX1 gate is illustrated in Fig. 12.

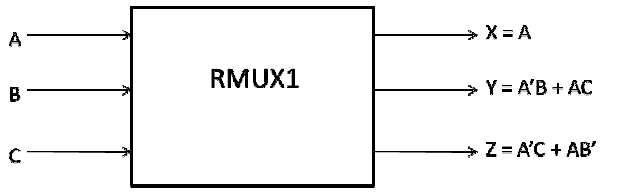

Fig. 12 shows functional block diagram of 3X3 RMUX1 gate.

The functional block diagram of 3X3 TKS gate is illustrated in Fig. 13.

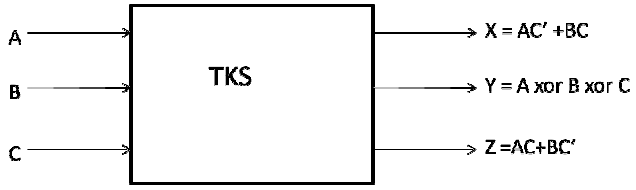

Fig. 13 shows functional block diagram of 3X3 TKS gate.

The functional block diagram of 4X4 BVF gate is illustrated in Fig. 14.

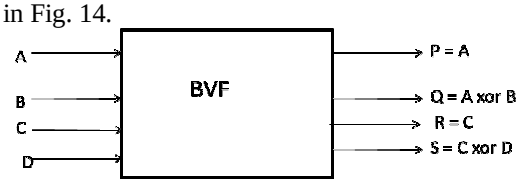

Fig. 14 shows functional block diagram of 4X4 BVF gate.

The functional block diagram of 3X3 TR gate is illustrated in Fig. 14.

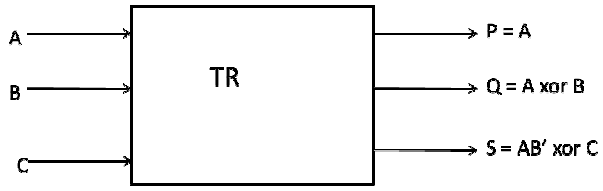

Fig. 15 shows functional block diagram of 3X3 TR gate.

5. A DETAILED ANALYSIS OF COMBINATIONAL CIRCUITS USING REVERSIBLE GATES

In 2012, the comparison between the reversible and conventional logic gates had been showed [11]. The authors collated the 4-bit reversible adder or subtractor circuit with the help of DKG gate. The comparison is based on low power consumption, delay, and number of gates, garbage outputs and constant inputs. The authors described that a 4x4 DKG gate can operate like a full adder and a full subtractor.

In 2013, a work described how the Reversible BVF gate can be useful to implement a one-bit reversible comparator [12]. The design is functional for the future computing techniques like ultra low power digital circuits and quantum computers. In [13], the authors proposed the transistor implementation of the reversible gates could be done by using a combination of CMOS-GDI circuit and TG Circuits, which provides the optimal solution for combinational logic, saving one-third of the power, half the area and ten percentage in delay relative to a CMOS implementation. GDI circuits provide some measure of enhanced hazard tolerance and are suited for low voltage operation mostly. The authors used the transistor implementation of reversible gates by using Tanner tools and H-spice tools. Moreover, the authors proposed the design of GDI and TG based reversible comparator circuit in 90nm technology.

In 2014, the authors in [14] proposed the design of different combinational circuits like serial adder, ripple carry adder, half adder and multiplexer using a method of applications of

reversible logic gates called as Quantum Cellular Automata (QCA). The authors also gave the comparison of the quantum cost of the proposed designs due to Coplanar Architecture. A comparative table of various QCA structures like Half Adder, Full Adder, Ripple Carry Adder, 2:1 Multiplexer, CDM and CSM were designed, simulated and analyzed with respect to parameters like number of cells and simulation time for the proposed coplanar based structure. From the paper, it had been showed that the coplanar architecture had reduced number of cells and simulation time than the previous structure. The table also gave a clear review on the percentage of reduced area between previous and proposed structures. Authors in [15] proposed that Reversible computing plays a vital role in Quantum computing had been described. The authors utilized the possibility of reversible logic to break the ordinary speed-power compromise, thereby getting a step closer to realise Quantum computing devices. Various combinational and sequential circuits such as a 4-bit Ripple-carry Adder, (8-bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of an 8-bit GCD processor using Reversible gates were used in the paper. The power and speed parameters for the circuits had been specified, and differentiated with their conventional non-reversible peers. The comparative study that the circuits designed using reversible logic gates were much faster and power efficient. Simulations of the designs were done using Xilinx 9.2 software. The authors in [16] described the design of High speed low power reversible logic BCD adder which was implemented using HNG gate. The design helped in reducing the number of reversible gates and also the cost of the circuit. Also, in [17], the VHDL implementation of Reversible Full Adder using a newly proposed Peres Gate had been indicated. The authors found that the PERES full adder is better than the irreversible full adder in terms of garbage outputs. By using proposed PERES full adder, it was proclaimed that a design of large reversible systems can be done and from there, the power consumption can be calculated and can be compared with the irreversible full adder. A proposition in [18] of a modified Fredkin gate can be utilized for implementing different types of reversible multiplexers such as 2:1, 4:1, 8:1 and 16:1 reversible multiplexers. The authors gave a comparison between quantum cost and power consumption of proposed reversible multiplexers with existing one.

In 2015, the authors in [19] presented a comparative study of efficacy of various reversible full adder and reversible full subtractor gate and their quantum cost values for obtaining energy efficient logic design. The article also gave a novel design approach for implementing reversible combinational circuits using the existing as well as newly improved reversible logic gates, in which the design and the implementations were done using HDL language called as Verilog.

In [20], the authors proposed different types of reversible encoders such as 4:2, 8:3 and 16:4, using Feynman and Fredkin gate. They were also compared with quantum cost of proposed reversible multiplexers with the existing one. The authors showed the quantum cost of 4:2, 8:3 and 16: 4 reversible encoders is 8, 19 and 48 respectively. The presentation of all the encoders using RTL view and also the waveforms had been done.

In 2016, the authors in [21] proposed a tremendous reduction in power consumption and delay of the reversible full adder circuits compared to the recently proposed one. The authors have designed the circuits using the 6T (Transistor) approach. So, the number of transistors is also reduced. Various voltages are applied to different technologies such as 0.35um, 0.18um, 0.6um, for the designer to choose the better architecture for the required power dissipation and delay easily.

The authors in [22] proposed a logarithmic depth quantum carry look ahead adder, which demonstrates two versions of addition namely in place and out-of-place method of addition for n-bit numbers, but the design is not optimized in terms of gates, garbage outputs, quantum cost and delay.

The authors in [23] proposed a novel methodology for reversible carry look-ahead adder, where presentation of improved designs of both in-place and out of place designs of reversible carry look-ahead adder had been made.

Also, in 2016, the authors in [24] proposed the different designs of ripple carry adder using Peres and HNG reversible gates. The modelling was done in Verilog HDL and the functional verification and synthesis was created using Xilinx ISE. The authors also did a look up table for the delay calculation of the Conventional ripple carry adder and reversible ripple carry adder using Peres and HNG gates including gate count, garbage output and Quantum cost. The conventional ripple carry adder had a delay of 8.162ns, whereas the reversible ripple carry adder using Peres and HNG gates were of 7.798ns and 7.644ns respectively. So, from the comparative table presented by the authors, it is seen that the reversible ripple carry adder using HNG gate had lesser delay in terms of the other two designs.

In 2017, the authors in [25] proposed that different combinational circuits such as half adder, full adder, full subtractor, multiplexer, comparator and decoder can be implemented using reversible logic gates. The authors proposed a reversible decoder using Fredkin gate with minimum quantum cost. A comparative chart in line with quantum cost, garbage outputs, and number of gates was also presented. The circuit had been implemented and simulated using Xilinx software. The authors also delivered the design of Programmable Read Only Memory (PROM) using reversible decoder on Field Programmable Gate Array (FPGA – SPARTAN 3E) which had less heat dissipation and low power consumption in [26]. The circuit was designed in terms of quantum cost, garbage outputs and number of gates.

In the same year, proposition of the design of 2:4 decoder using CMOS BSIM4 model had been showed [27]. The

designed circuit was implemented using Tanner EDA tools and the paper also gave a clear review on garbage outputs, quantum cost, and constant inputs.

In 2018, the authors in [28] presented some of the combinational as well as sequential circuits using Xilinx ISE. The authors also gave a clear comparison based on power supply, delay and temperature etc of the reversible circuits with respect to conventional circuits.
A presentation of the comparison of different reversible logic at two subsequent levels i.e. gates structural level and circuit design level, to provide a better solution for designing logic circuits had been expressed [29]. From the paper, it is known basic gates are 50% efficient at gate level and 33% at design level analysis in terms of gate cost, as compared to the most efficient gates proposed in the literature.
Moreover, in 2018, the authors in [30] proposed a novel approach to design n-bit arithmetic circuit with reversible design approach. The authors also presented a comparison table in terms of number of reversible gates, number of garbage outputs and number of constant inputs applied for the existing and proposed 1-bit arithmetic circuit, which is a vital component for ALU applications. The design was simulated and synthesized using Xilinx Software. The authors in [31] proposed a novel approach for the Reversible realization of 3:8 size decoder circuits with optimized performance parameters as compared to the earlier designs. The comparison had been done with respect to total number of Reversible logic gates, constant inputs, garbage outputs and quantum cost. The design is efficient for low power applications.

In 2019, the authors [32] proposed Half Adder, Half Subtractor and Full Adder circuit using TSG, HNG and Peres gates respectively. The authors gave a clear comparison on the Propagation Delay and also the on-chip power dissipation of the given circuits. The author proposed from the comparison table that in case of low Power dissipation, 4X4 reversible Full Adder using HNG gate and 4X4 reversible Half Subtractor and 4X4 reversible Half Adder using TSG gate as the best. In terms of Delay, for designing reversible 4X4 Full Adder, HNG gate for lesser delay and TSG gate for 4X4 reversible Half Subtractor and 4X4 reversible Half Adder are the best for designing these combinational circuits. The authors in [33] portrayed the reversible logic cryptography design (RLCD) and using which the encryption and decryption architecture had been designed. The application specified integrated chip (ASIC) and field-programmable gate array (FPGA) performances were evaluated for both existing and proposed method. ASIC performances which were more than 7% had been improved in RLCD-LFSR method compared to the conventional methods.

Moreover, in 2020, the authors gave a clear implementation along with the comparison table of the design of full subtractor, complex adders, parity generators, multiplexers and decoders using Toffoli, HNG, NFT and Fredkin gates [34, 35]. Moreover, several implementations of reversible gates have been done using VHDL in 2012 [36], where the authors proposed that reversible logic is of substantial significance. In [37], the authors presented that the reversible circuits are designed using parity preserving gates, which contains the property of detecting not more than a single error in the circuit's primary output. The authors presented the design and FPGA synthesis of optimized data selectors. The low switching power consumption characteristics of data selectors, which were typically around 1 to 3μW that finds its use in low power applications, which are targeted ultra-speed, had been highlighted by the authors. The authors in [38] proposed a new reversible ternary full-adder which is called as 'comprehensive reversible ternary full-adder', using the ternary logic capabilities over binary logic capabilities. Using the two proposed reversible circuits, the authors introduced a new reversible full adder or full subtractor. The comparison table displayed there are lower quantum costs in case of the proposed circuits than the previous circuits.

In 2021, author in [39] proclaimed a metric to measure the energy-efficiency of integrated circuits known as Q-Factor (a dimensionless parameter). Q = 1 is meant to be all energy input will be dissipated as waste heat, whereas, Q >1 is meant to be of greater energy efficiency. The author gave a clear table of Q- factor for conventional Business as Usual (BAU) semiconductor nodes and Reversible Adiabatic-CMOS nodes and beyond. The comparison table for transportation to IC technology with the actual energy efficiency was given. In case of transportation, the actual energy efficiency was 20 percent and that of IC Technology is of 0 percent, as portrayed by the author.

The below comparison table shows the analysis of the mostly used reversible gates for designing various combinational circuits based on some of the research articles utilized.

Combinational Circuits	Number of Reversible Gates Used	Names of the Reversible Gates
1. Half Adder	1	Peres Gate
	1	HNG Gate
2. Full Adder	1	Peres Gate
	1	HNG Gate
	1	TSG Gate
	1	DKG Gate
3. Half Subtractor	1	TSG Gate

		3	2 CNOT gates & 1 Toffoli Gate.
4.	**Full Subtractor**	3	1 HNG Gate, 1 Fredkin Gate & 1 Feynmann Gate
		1	DKG Gate
5.	**Decoder (2:4)**	6	4 Toffoli Gates and 2 NOT Gates
		3	Fredkin Gates
6.	**Multiplexer (2:1)**	1	NFT Gate
		1	RMUX1 Gate
7.	**Parity Generators**	1	Even – HNG Gate
		1	Odd – HNG Gate
8.	**4 -- Bit Ripple Carry Adder**	4	4 HNG Gates
		8	8 PERES Gates
9.	**2 -- Bit Carry Look Ahead Adder**	10	7 PERES Gates and 3 TKS Gates
10.	**Comparator**	3	PERES and BVF Gate.
		3	Toffoli and BVF Gate
		3	Fredkin and BVF Gate
		3	TR and BVF Gate

Fig. 16 shows the different combinational circuits which were implemented using different reversible gates, based on some of the research articles.

6. FUTURE WORK AND CONCLUSION

Reversible circuit is an arising innovation with a promising application due to low power dissipation. This review paper on combinational circuits using reversible gates helps the designer to get the best approach to design out of the given chart in Fig. 14. In future, by using these gates, a designer can design any of these combinational circuits with numerous advantages over conventional gates such as, low power, low complexity, less delay, high speed etc. Reversible computing has become a new emerging area for researchers in recent years in fields like Quantum Computing, Nanotechnology, Low Power CMOS Design and many more [40, 41, 42, 43].

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