ISSN 2347 - 3983
Volume 7, No. 12 December 2019
International Journal of Emerging Trends in Engineering Research
Available Online at http://www.warse.org/IJETER/static/pdf/file/ijeter287122019.pdf
https://doi.org/10.30534/ijeter/2019/287122019

Implementation of GDI Logic for Power Efficient SRAM Cell with Dynamic Threshold Voltage Levels

M Siva Kumar[1], Syed Inthiyaz[2], M Aditya[3], P Rupanjani[4], B Aravind[5], M Mukesh[6], Sanath Kumar Tulasi[7]
Associate Professor[1,2], Assistant Professor[3,7], Student[4,5,6]
[1,2,3,4,5] Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur.
syedinthiyaz@kluniversity.com

ABSTRACT

The main objective of this article is to implement the 4-bit SRAM array model to work with low voltage power. We used the GDI (Gate Diffusion Input) methodology in this application, it allows to minimize power usage and often reduces the number of transistors. The ambiguity of the model is eliminated by using this technique. To successfully nullify delays in static energy absorption and propagation, GDI logic and dynamic threshold logic will be used to model SRAM structures. Marginal components like preload circuit, row decoder, column decoder and sensor amplifier were also formed and acquired for the build SRAM array with the support of the Mentor Graphics Stimulation Tool. For both logic-1 and logic-0 read and write operations with transient response is evaluated, 25MHz operating frequency and access time is 10ns for both 90uW consumption of power is determined for entire SRAM array, read and write procedure, and Vs (supply voltage) is 0.4V. Higher performance compared to CMOS logic and different strategies for the development of transistor logic. Different methods compared to the area of design, number of machines, delay and energy dissipation. Technology compatibility, top-down layout, and pre-computing synthesis concerns are explored by illustrating advantages and disadvantages over other techniques in GDI Technique.

Key words : SRAM, dynamic threshold, read operation, Mentor Graphics

1. INTRODUCTION

First suggested GDI technique by Arkasiy Morgenshtein, Ida n Shwartz and Alexander. Usingthis approach, only two transistors are used in various complex logic functions.

The design of 6 T SRAM becomes a new challenge in the Nano meter engineering processing requirement of the SOC (System on Chip) due to the variations in voltage of threshold. Threshold voltage fluctuations can have an effect on the stability of the SRAM and reading / writing process. This paper expands the previous designs such as CMOS logic and resistive load based on inverters.

The output voltage swing relies on the VDD while using CMOS logic, which produces more power consumption and increasing power consumption by using more PMOS transistors and moving up and down networks. The effective method is the scaling of transistor to reduce leakage currents. The scaling of the voltage supply is a generally recognized method to increase the consumption of power of the circuit. Due to slight differences in voltage between the body of a transistor, source and the drain of the transistor, the leakage is reduced so that the whole digital blocks in the architecture of memory with the logic of GDI (Gate Diffusion Input).

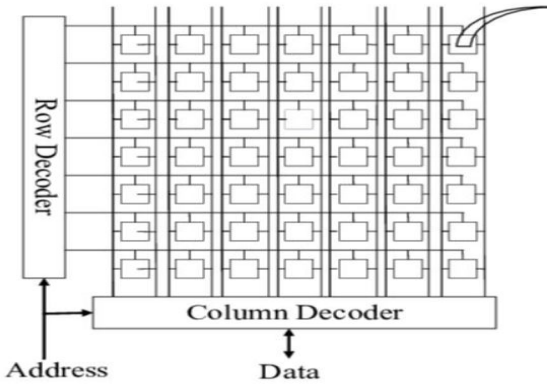

Figure 1: Architecture of SRAM Memory

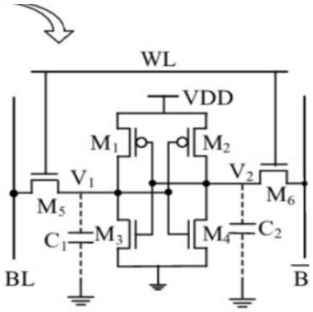

Figure 2: Structure of GDI Cell

The GDI cell is made up of three inputs, namely:
1. G (common entry gate for NMOS and PMOS)
2. P (Entry of PMOS / Drain)
3. N (source of input drain / source of NMOS)

Here low power consumption while retaining low logic complexity is maintained. Another relevant issue is the low voltage power supply, in this paper we use Dynamic Threshold logic to run the full circuit at 0.4V power supply. The idea at the rear of MOS dynamic threshold is, the Vbs voltage at input for NMOS is higher than Zero and is negative for PMOS, thereby reducing the threshold voltage.

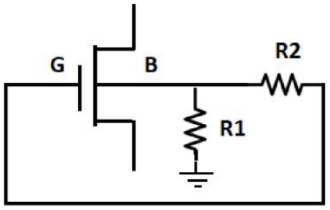

Figure 3: Dynamic threshold logic.

The DTMOS design will be utilizing the terminal of the body and the gate to provide the signal input and both are shortened by a resistive network serves as a voltage divider.

$$Vbs = Vg\ (R1 // R2) \text{ -------- } (1)$$

In terms of gate input, both reverse body bias and forward body bias occurred at the terminal of the body, as R1 and R2 are poly-resistant.

The formula shows the relationship between the input signal and Vt.

$$Vt = Vto + (\sqrt{(\varphi}s + Vbs - \sqrt{\varphi s}\ ) \text{ -------- } (2)$$

Where the threshold voltage of the body effect parameter and Vt is proportional to the body effect. With respect to variable body bias, variations in threshold voltage from equation 1 may be possible without affecting the SRAM's stability at low power supply.

2. SRAM CELL

The elementary SRAM cell is designed to form a latch with connected CMOS inverters to store one bit of information storage (either 0 or 1). Here GDI inverters with arbitrary threshold (Vt) variance replace CMOS inverters. The benefit of Gate Diffusion Input is a stronger logic swing, and a good advantage is information storage. Two (2) pass gates are designed to access the information that links the latch to (2) two complementary bit stripe columns (BL and BLB) and the two (2) pass gates are triggered when word line (WL=1) is asserted.

When WL=0 isolates the (2) two pass gates to the lock and unchanges the preceding latch information. The threshold voltage of the pass gates progressively decreases from the initial high to the WL=1 during the write / read process. The pass gate W / L ratios are adjusted accordingly and the GDI cell's Pull up and pull-down network is set at a ratio of 2 to 1 for non-destruction of information during writing operation and information adjustment.

$$Id = K\frac{w}{l}(Vgs - Vt)^2 \text{ -------- } (3)$$

This equation is due to the technique of the dynamic threshold

$$Id = K\frac{w}{l}(Vgs - (\gamma(\sqrt{\varphi s} + Vbs) - \sqrt{\varphi s}) + Vto))^2 \text{ -------- } (4)$$

from equation (2)

$$Id = \frac{w}{l}K(Vgs - (\gamma(\sqrt{\varphi s} + V_G(R_1 // R_2) + Vto) - \sqrt{\varphi s})))^2 \text{ -------- } (5)$$

If Vgs is more positive then if Vgs is negative, the current calculation (5) becomes reverse bias for the dynamic threshold technique.

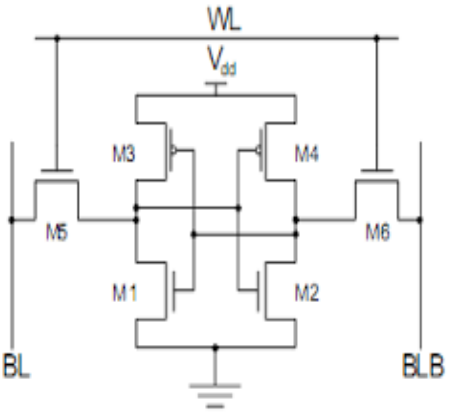

Figure 4: CMOS design of SRAM Cell

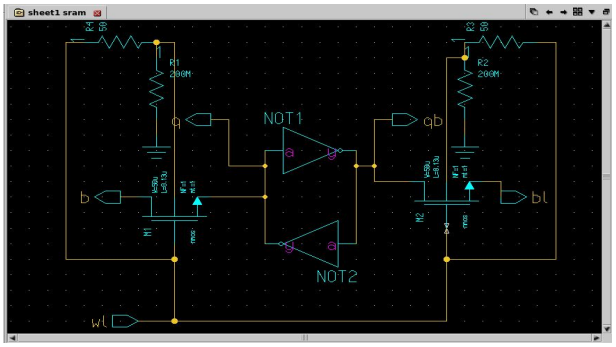

Figure 5: Dynamic Threshold SRAM Cell

2.1 Write Operation:

When WL=1 activates the two control transistors, the inform ation to be compiled. The cell data needed the difference in the bit lines.

2.2 Read Operation:

Based on the data stored in the cell during the reading cycle, the write logic, WL=1 and the bit lines are charged and discharged. To evaluate the processing value, the sense amplifier tests the voltages on the bit lines.

The parameters (dimensional) of PMOS and NMOS transistors in the control transistors and GDI cell.

Table 1: Parameters of GDI with dimensions.

Parameters	GDI-PMOS	GDI-NMOS
Length of the Channel(L)	130nm	130nm
Width of Channel(W)	50nm	20nm

3. COLUMN DECODER

In the 4X4 SRAM array model, decoder is one of the major peripherals. The 4X4 SRAM set requires a 2:4 decoder. The decoder's output is used to deselect or select the word line WL for each row/ column SRAM array. Schematics of the 2:4 decoder.

AND Gate is a key decoder development cell. The conservative Complementary MOS AND gate require four transistors, but here GDI uses AND gate in the 2:4 decoder design, which requires only two inverter-like transistors. The VDD is linked to the P-diffusion. One of the N-diffusion outputs is connected to the gate output and another to the source.

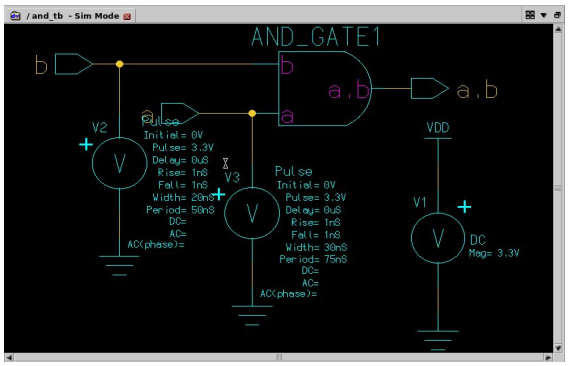

Figure 6: AND Gate using GDI Logic

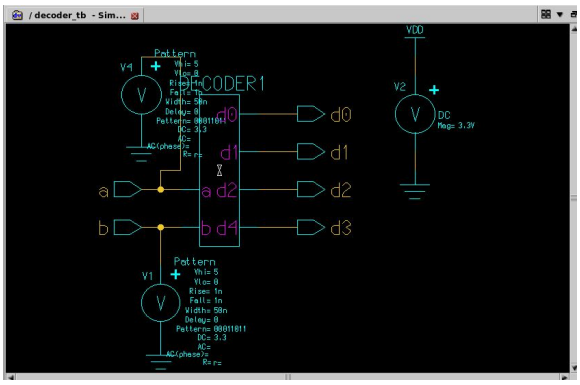

Figure 7: Decoder

4. SRAM ARRAY

Here 4X4 SRAM array is equipped with 2 KB (2nX m) storage capacity where m is the no of the memory cell and n is the number of the address outlines, measuring the equal for 16 bits. This comprises 4 difference sense amplifiers, 4 preload circuits, and 2:4 Read/Write decoder for specific word selection.

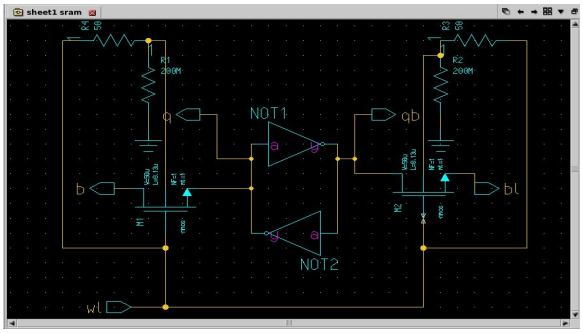

Figure 8: 4X4 SRAM array.

5. RESULTS

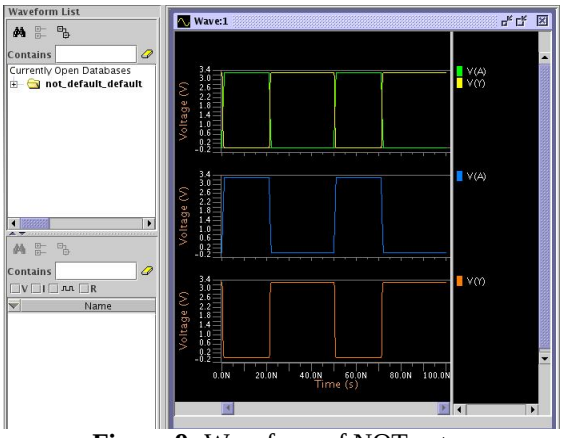

Figure 9: Waveform of NOT gate.

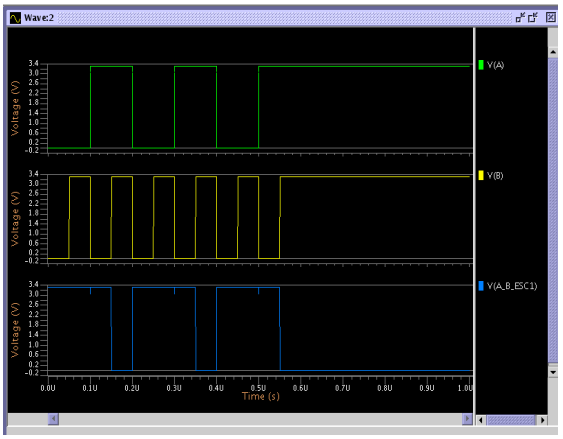

Figure 10: Waveform of AND operation.

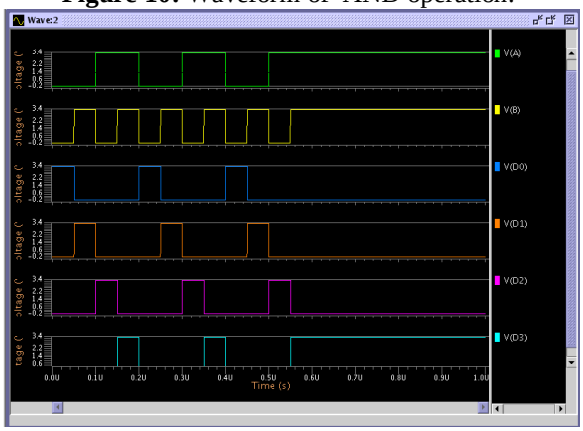

Figure 11: Waveform of Decoder

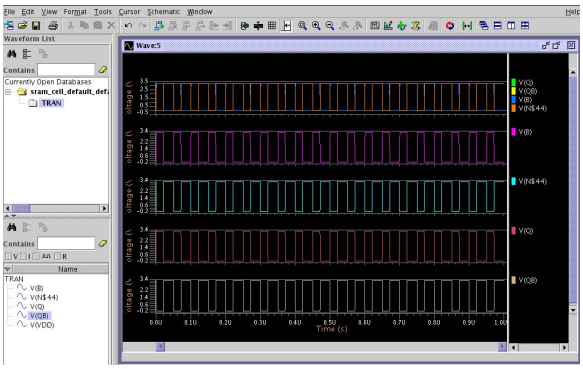

Figure 12: Waveform of SRAM cell

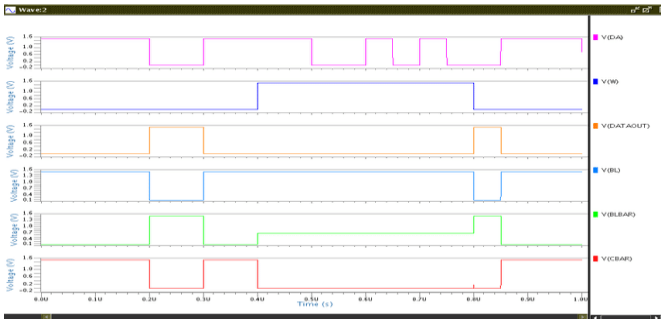

Figure 13: Waveform of SRAM array

Table 2: Performance Results

CONSTRAINTS	RESULTS
Supplied Voltage	0.4V rail to rail
Max-Operating Frequency	20 MHz
Current (total)	200 uA
Power Consumption (Avg)	90 uW

6. CONCLUSION

A 4X4 low-power SRAM array is implemented to store 16 bits. In order to form the SRAM array, peripheral components such as sensor amplifier, row decoder, including column decoder and preload circuit were created and assembled.
To reduce noise, the differential shape sense-amplifier is used. Logic SRAM with GDI processing cell is used to prevent dissipation of static heat. The voltage of 0.4V peak-to-peak (rail-rail) and the pulse input signal of 0.4V supply voltage is known to be Temporary responses for write and read operations of both-0 and 1. For the full range of SRAM, the power consumption is estimated at 90 uW. The SRAM set is built using the Mentor Graphics software Virtuoso Schematic Editor (version 6.1.5). For growth, the UMC130 standard library (i.e. 130 nm Node in technology) has been utilized. The 20MHz operational frequency is achieved.

ACKNOWLEDGEMENT

Authors like to express their gratitude to department of ECE of K L University and DST through ECR/2016/000569, SR/FST/ETI-316/2012 and EEQ/2016/000604.

REFERENCES

1. Siva Kumar, Syed Inthiyaz, Ch. Krishna Vamsi, Sk. Hasane Ahammad, K. Sai Lakshmi, P. Venu Gopal, A. Bala Raghavendra 2019. Power Optimization using Dual SRAM Circuit. 2019 International Journal of Innovative Technology and Exploring Engineering.
2. M.Siva Kumar, Syed Inthiyaz, P.Venkata Krishna ,Ch. Jyothsna Ravali, J.Veenamadhuri, Y.Hanuman Reddy, Sk. Hasane Ahammad 2019. Implementation of Most Appropriate Leakage Power Techniques In VLSI Circuits Using NAND and NOR Gates. 2019 International Journal of Innovative Technology and Exploring Engineering
3. Prasanna kumar.P,Siva kumar.MImplementation of digital beam former software on FPGA based system 2018 journal of advanced research in Dyanamical and control systems
4. R. Bisht, P. Aggarwal, P. Karki and P. Pande. 2016. 4 SRAM array design using CMOS logic and differential sense amplifier with low power and noise resistance. 2016 International Computing, Communication and Automation Conference (ICCCA), Noida. Pages 1474-1478. https://doi.org/10.1109/CCAA.2016.7813954
5. D. Ho, K. Iniewski, A. Ivanov, S. Kasnavi, S. Natarajan. 2006. Ultra-low 90 nm 6 T SRAM cell for applications in the wireless sensor network. 2006 IEEE International Circuit and Systems Symposium, Kos Island. P. 4, doi: ISCAS 10.1109.2006.169353.
6. A. I. Shwartz and A. Morgenshtein. Fih. 2010. Gate Diffusion Input (GDI) logic in the nanoscale process of standard CMOS. 2010 IEEE 26th Electrical and Electronic Engineering Convention in Israel, Eliat. Pp. 000776-000780.doi: 2010.5662107.10.1109/EEEI.
7. N. Lindert, T. Sugii, S. Tang and Chenming Hu. 1999. In IEEE Journal of Solid-State Circuits. 34(1): 85-89, doi: 10.1109/4.736659. Lindert, T. Sugii, S. Tang and Chenming Hu. 1999. https://doi.org/10.1109/4.736659
8. K. C. Shah, D. N. Gandhi and B. H. Nagpara. 2013. 4-bit SRAM model and analysis in Deep Submicron CMOS Technologies. Journal of Electronics and Communication Technology Data, Knowledge and Study. 2: 812-817.
9. P.S. Bellerimath and R. M. Banakar. 2013. 4X4 SRAM Flash Array Architecture using 180 nm Technology. European Journal of Current Engineering and Technology. pp. 288-292.
10. Syed Inthiyaz, M V D Prasad, R. Usha Sri Lakshmi, N.T.B. Sri Sai, P. Pavan Kumar, Sk Hasane Ahammad, "Agriculture based plant leaf health assessment tool: A Deep Learning perspective" International Journal of Emerging Trends in Engineering Research, 7(11), November 2019, 690-694. https://doi.org/10.30534/ijeter/2019/457112019
11. Ahammad, S.H., Rajesh, V., Venkatesh, K.N., (...), Rao, P.R., Inthiyaz, S." Liver segmentation using abdominal CT scanning to detect liver disease area" International Journal of Emerging Trends in Engineering Research, 7(11), November 2019, 664-669. https://doi.org/10.30534/ijeter/2019/417112019

12. Prasad, M.V.D., Inthiyaz, S., Teja Kiran Kumar, M., (...), Kumari, R., Ahammad, S.H.. "Human activity recognition using deep learning" International Journal of Emerging Trends in Engineering Research, 7(11), November 2019, 536-541. https://doi.org/10.30534/ijeter/2019/227112019
13. Syed Inthiyaz, Sanath Kumar Tulasi, R.S.L.Jayanthi, Ch.sahitya, Ch.jyothi, "Design Of Bi-Trigger Sram Using Schmitt Trigger For Low Power 13t Cmos Application. INTERNATIONAL JOURNAL OF SCIENTIFIC & TECHNOLOGY RESEARCH VOLUME 8, ISSUE 12, DECEMBER 2019,1466-1471.
14. 1. Myla, S., Marella, S.T., Swarnendra Goud, A., (...), Kumar, G.N.S., Inthiyaz, S. "Design decision taking system for student career selection for accurate academic system" in INTERNATIONAL JOURNAL OF SCIENTIFIC & TECHNOLOGY RESEARCH VOLUME 8, ISSUE 09, SEPTEMBER 2019, pp-2199-2206.
15. Mohanachandrika, O., Siva Kumar, M, "Design of high speed single ended 6T and 8T SRAM cells" in International Journal of Advanced Trends in Computer Science and Engineering, volume 8 Issue 3, June 2019, pp 470-478.
16. M.Siva Kumar, Syed Inthiyaz, J. Dhamini, A.Sanjay,U.Chandu Srinivas, "Delay Estimation of Different Approximate Adders using Mentor Graphics" in International Journal of Advanced Trends in Computer Science and Engineering, Volume 8, No.6, November – December 2019,pp:3584-3587.
17. Siva Kumar M., Inthiyaz S., Narsimha Nayak V., Bhavani M., Charan Teja K., Rajesh S.J.S., Eswar Reddy K., Sruthi Keerthana G." Analysis of low power conditional sum adder" in Indian Journal of Science and Technology, Volume 9, Issue 17, article no:93033. https://doi.org/10.17485/ijst/2016/v9i17/93033
18. Murali Krishna B., Siva Kumar M., Rajesh J., Inthiyaz S., Mounica J., Bhavani M., Adidela C.N., "FPGA implementation by using XBee transceiver" in Indian Journal of Science and Technology, Volume 9, Issue 17, article no:93032.