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Design of a Novel Isolated Single Switch AC/DC Integrated Converter for SMPS Applications

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ABSTRACT

A novel single-stage single-switch isolated converter is proposed for attaining high power factor and wide voltage conversion range. This converter interfaces a buck-boost type PFC circuit with a buck type Dc-Dc regulator to process the input power in a single step. By this integration, the proposed converter is able to attain unity input power factor, wide voltage conversion range, low switching voltage stresses and high efficiencies. By isolating the converter non-inverted output voltage is obtained which is an advantage over non-isolated topologies. The input buck-boost stage is operated in discontinuous conduction mode (DCM) to attain high input power factor and the output buck stage is operated in continuous conduction mode (CCM). A simple single closed loop voltage feedback controller is used to get well-regulated and fast output voltage response. A detailed principle operation and design of converter has been analysed theoretically. The performance of the proposed converter is simulated by using MATLAB-SIMULINK software to validate the simulation results with the experimental results.

Key words: Single switch, isolated, integrated converter, PFC, buck-boost, ac/dc converter.

1. INTRODUCTION

Currently AC-DC converters are much important because of their applications in all fields such as renewable, EV's, battery storage systems, uninterrupted (UPS) and switch-mode (SMPS) power supplies, LED drivers etc., These types of applications it requires PFC system to enhance the input power factor with low-harmonic distortion at input current [1-4]. In Conventional ac/dc converters normally consists of two stages, first stage performs the PFC operation and at second stage is Dc-Dc regulator. Based on this, different converters are designed to achieve unity input current, high efficiency and to get less input current percentage (%) THD [5-7].

A class of Dc/Dc converter that converts a source of DC from one voltage level to another. Linear and switched are comes under the types of Dc/Dc converter. A linear Dc/Dc converter uses a resistive voltage drop to create and regulate a specified output voltage. In Switched-mode Dc/Dc converter (SMC) converts one level of Dc voltage to another, which can be lower or higher, storage of the input energy temporarily and then discharging that energy to the output at a various voltage level.

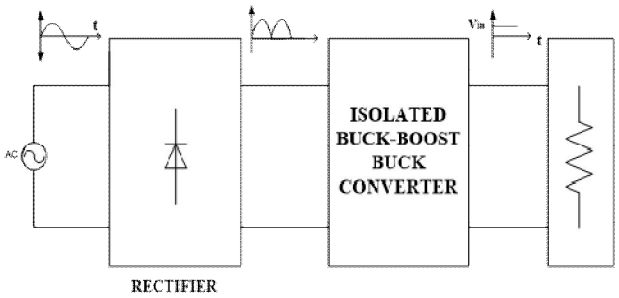

Figure 1: A Typical representation of integrated isolated buck-boost buck converter (BBBC).

These converters storage of input energy is in periodical manner and then discharging that energy to the output at a various voltage level [8-10]. The storage may be either a magnetic field component such as inductor, and or an electric field component like a capacitor. Transformer-based converters provide isolation between the input and the output. SMC offer three main advantages:

- The efficiency of the power conversion is very high.
- Usage of passive components number are less, switching frequency is higher and losses are lower this simplifies the thermal management.
- An inductor stored energy in a switching regulator, which can be transformed to output voltages that may be lesser than the input (step-down or buck), more than the input (boost), or buck-boost with reverse polarity (inverter).

A linear converter can only produce a voltage that is lower than the input voltage, unlike SMC. Among all the single-stage converters, the converter is divided into PFC stage and regulator stage [11-13].

The first stage of operation in the converter, i.e., PFC is obligatory in Ac-Dc converters. It permits the converter to encounter harmonic standards without necessity of a costly and bulky input filter that generally accompanies a passive Ac-Dc converter. So, to enhance the power factor buck-boost converter is used due their characteristics and outstanding capabilities for power range. The buck-boost converter output may be either smaller or larger than input voltage; by this it demonstrates the DCM technique to attain PFC from the first stage of the converter. When PFC stage operated in CCM it results in higher harmonic currents and less power factor correction [10].

An isolated dc-dc converter i.e., second stage of the converter employs a transformer to eliminate the dc path between its input and output, reduce noise and better power quality. Isolation defines the electrical separation between the input and output of a dc-dc converter. In contrast, a non-isolated dc-dc converter has a dc path between its input and output. By isolation voltage conversion ratio of this converter is wide. By isolation the following are the advantages of the proposed converter [10].

The advantages of proposed converter are-

(a) Non-inverted output is obtained.

(b) Multiple outputs can be achieved at the secondary side of transformer.

(c) Line current %THD can be reduced.

Buck converter is chosen as regulator stage for its step-down ability. It can be operated either in CCM or DCM. When buck converter is operated in discontinuous mode it draws high peak currents. When it operates in DCM there are many advantages like- unity input power factor, high efficiencies, voltage stresses of switch and capacitor are independent to load.

2. PROPOSED ISOLATED CONVERTER

2.1 The Topology

Fig. 2 illustrates the proposed converter and this converter represents buck-boost buck converter to the ac mains. Inductor L_1 of the selected converter is operated in DCM. Both buck-boost and buck inductors are energized when switch S_1 is activated.

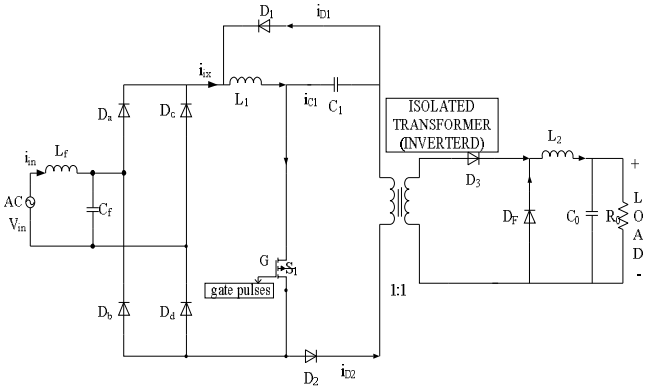

Figure 2: Isolated buck-boost buck converter

Inductor L_2 i.e., secondary side of transformer is operated in CCM. The switch S_1 operated at switching frequency (f_s) of the converter. To understand the current direction among the diodes, there are four modes which are explained briefly.

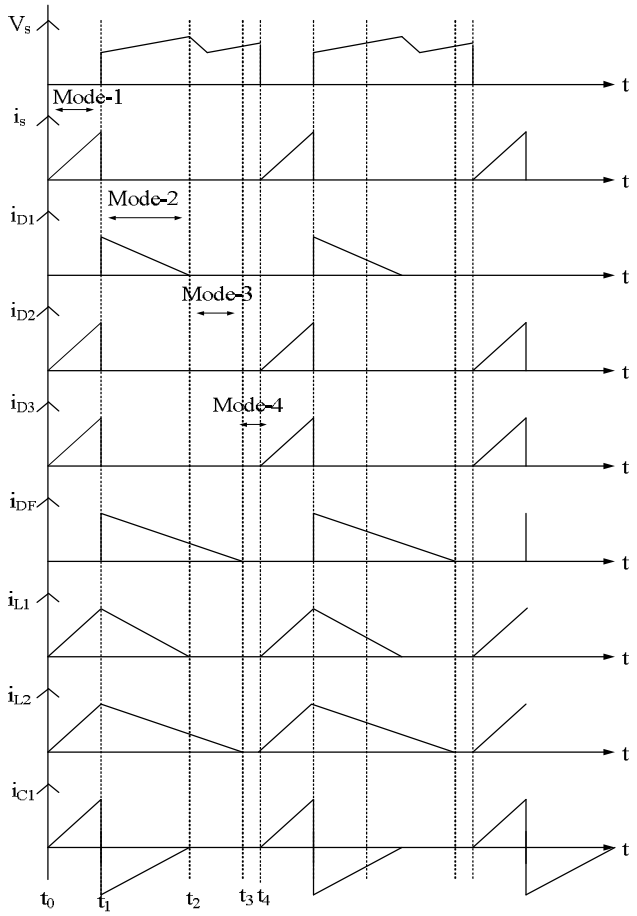

Figure 3: Model waveforms of buck-boost buck converter

2.2 Steady-state Operation of Proposed Converter

The converter operation and currents flow among diodes when switch S_1 is ON, and the four modes of operation is shown below.

(a)Mode-1:

Gate signal of the switch is set to high to turn on switch S_1. Fig. 4 shows the current flow path. Diodes D_2 and D_3 are in forward bias and L_1 and L_2 starts charging and D_1 and D_F are in reverse bias and current in capacitor C_1 is positive.

(b)Mode-2:

Gate signal of the switch set to S_1 is low to turn off. Fig. 5 illustrates the path of inductor currents during this mode. Inductors currents L_1 and L_2 gets discharge through D_1 and D_F as they are forward biased and current from capacitor C_1 is negative as energy stored in the capacitor gets discharge. In this interval D_2 and D_3 are reverse bias.

(c)Mode-3:

Gate signal of the switch S_1 is set to low to turn off. Fig. 6 illustrates the current path. The inductor L_2 discharged through free-wheeling diode D_F and the capacitor current remains zero at this instant.

(d) Mode-4:

The switch is in OFF state and diode D_f is in forward biased condition and stored capacitor energy C_0 discharges through the load and current in the inductor L_2 is in discontinuous mode.

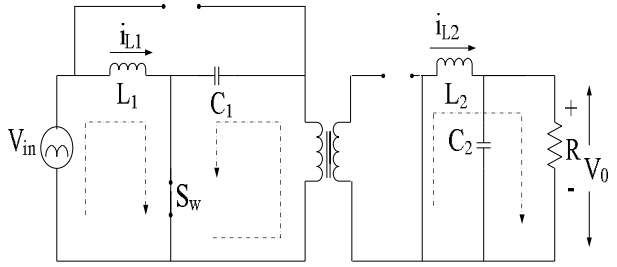

Figure 4: Operating mode-1 of isolated converter

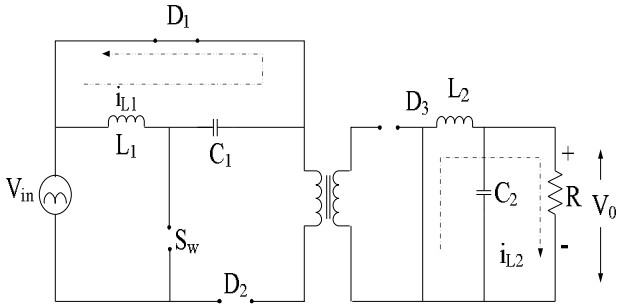

Figure 5: Operating mode-2 of isolated converter

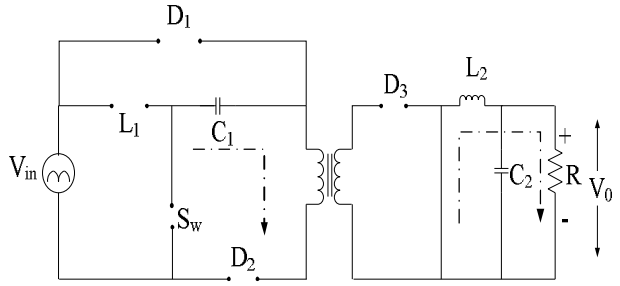

Figure 6: Operating mode-3 of isolated converter

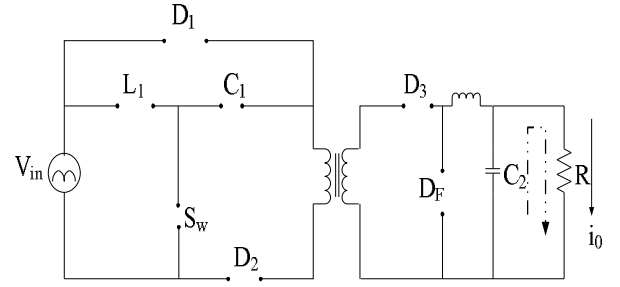

Figure7: Operating mode-4 of isolated converter

3. PROPOSED CONVERTER DESIGN PROCESS

The analytical model of proposed converter is validated with simulation results are derived in this section. Consider supply voltage as (V_{in}) is given as $V_{in}=v_{in}\sin(\omega t)$. During the interval of d_1T, the inductor input current iL_1 is same as that of input current i_s. Assume that input voltage v_s is constant when line frequency f_L is less than switching frequency f_s. So peak current pulse is directly proportional to the input voltage V_s. Hence, the average input current of each pulse can be expressed as-

$$(i_s) = \frac{i_{sp}}{2T_s} d_1 T_s = \frac{d_1^2 V_s}{2L_1 f_s} \sin \omega_L t \quad (1)$$

Where i_s = input current at t_1, i_{sp} = peak value of each current pulse and V_s= supply voltage. From equation (1), observed that input line current is in sinusoidal shape and in phase with V_s. By DCM, the inductor L_1 can achieve unity power factor. Thereby input power P_s can be written as

$$(P_s) = \frac{1}{2} V_s (i_{sp}) = \frac{d_1^2 V_s^2}{4L_1 f_s} \quad (2)$$

3.1 Output and Capacitor voltage Equations

As the converter operated in DCM, the voltage can be controlled independent to the load and following equation can be derived

$$V_{C1} d_1 N_1 = V_0 d_2 N_2 \quad (3)$$

Where V_{C1} is voltage across capacitor, d_1 is duty ratio of switch, N_1 is number of turns at primary side of the transformer, V_0 is voltage across load, d_2 is duty ratio and N_2-number of turns at secondary side of the transformer. As the load is resistive, the output power can be determined as

$$P_0 = V_0 I_0 \quad (4)$$

$$P_0 = \frac{v_0^2}{R} \quad (5)$$

Assuming lossless converter, by equating equations (2) and equation (5) we obtain the output voltage,

$$\frac{d_1^2 V_s^2}{4L_1 f_s} = \frac{v_0^2}{R} \quad (6)$$

$$\frac{d_1^2 V_s^2 R}{4L_1 f_s} = v_0^2 \quad (7)$$

$$V_0 = \frac{d_1 V_s}{2} \sqrt{\frac{R}{L_1 f_s}} \quad (8)$$

To evaluate the magnetizing inductance [2] of the primary side of a transformer L_p, is written as

$$P_f = \frac{V_{C1}^2 d_1^2}{2L_p f_s} \quad (9)$$

From equation (9) the capacitor voltage can be expressed in terms of line voltage as

$$V_{C1} = V_I \sqrt{\frac{L_p}{2L_{p2}}} \quad (10)$$

Where L_p is the magnetizing inductance.

3.2 Critical Voltage Equation

From equation (8), the voltage conversion ratio $M(d_1)$ can be written as

$$M(d_1) = \frac{V_0}{v_s} = \frac{d_1}{2}\sqrt{\frac{R}{L_1 f_s}} \quad (11)$$

where R- Load resistance, L_1-input inductor, f_s-switching frequency. For simplification equation (11) can be written in the terms of 'k' as

$$M(d_1) = \frac{v_0}{v_s} = \frac{d_1}{\sqrt{2k}} \quad (12)$$

where k is the critical factor,

$$k = \frac{2L_1 f_s}{R} \quad (13)$$

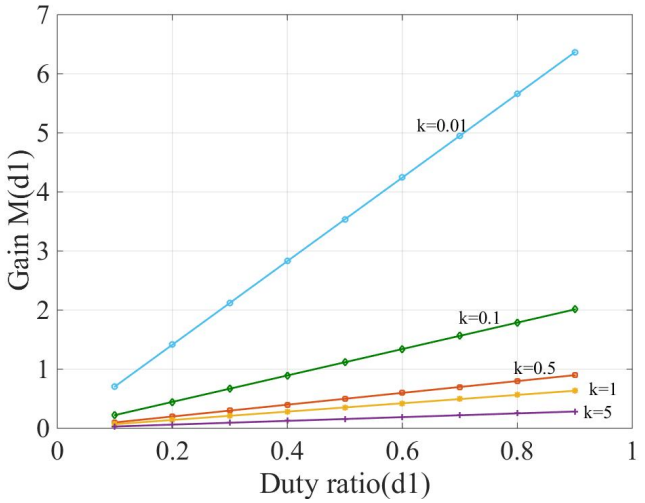

Figure 8: Voltage conversion ratio $M(d_1)$ versus duty ratio 'd_1' for different 'k' values

3.3 Conditions for DCM

To operate the converter in DCM, by applying volt-sec principle to the input inductor from figure (3) and it can be expressed as

$$\frac{v_s}{L_1} d_1 T_s - \frac{V_{C1}}{L_1} d_2 T_s = 0$$

$$d_1 = d_2 \frac{V_{C1}}{v_s} \quad (14)$$

where v_s = The instantaneous input voltage. And, for L_1

$$\left(\frac{V_{C1} - V_0}{L_1}\right) d_1 T_s - \frac{V_0}{L_1}(d_2 + d_3) T_s = 0$$

$$d_2 + d_3 = d_1 \left(\frac{V_{C1} - V_0}{V_0}\right) \quad (15)$$

where d_1 is in ON duration and d_2, d_3, d_4 are in OFF duration. To operate L_1 in DCM, the following conditions must be satisfied:

$$d_1 + d_2 + d_3 \leq 1 \quad (16)$$

To operate L_2 in DCM mode, following condition must be satisfied:

$$d_1 + d_2 + d_3 + d_4 \leq 1 \quad (17)$$

By solving equations (16) and (17) by using equations (14) and (15), we get

$$\frac{v_s}{V_0} \leq \frac{1 - d_1}{d_1^2} \quad (18)$$

$$d_1 \leq \frac{V_0}{V_{C1}} \quad (19)$$

3.4 Condition for 'k' Critical

From equation (17) the inductor L_1 operates in BCM. This condition improves the efficiency by reducing the current stress on switch.

From equations (13) and (19) 'k' value can be expressed in the form of duty ratio d_1 by

$$K \leq \frac{(1 - d_1)^2}{2d_1^2} \quad (20)$$

From equation (20) the critical value can be obtained to operate L_1 in DCM as

$$k_{critical} = \frac{(1 - d_1)^2}{2d_1^2} \quad (21)$$

From equation (21) it can be justified that the DCM region for voltage conversion ratio M(D) of the proposed converter is wide compared to basic buck-book converter. So L_1 is operated in DCM for $k \leq k_{critical}$, otherwise the converter is operated in CCM region.

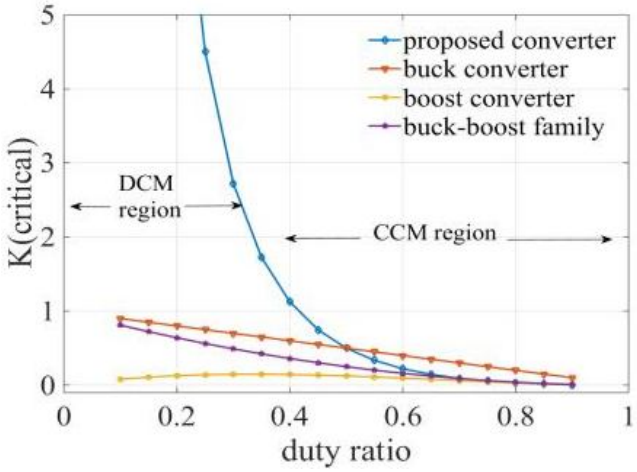

Figure 9: Graphical representation of $K_{critical}$ for different converters.

Table 1: Boundary conditions for CCM/DCM operations for different converters

Converter	CCM/DCM-boundary condition ($K_{critical}$)
Proposed converter	$\frac{(1 - d_1)^2}{2d_1^2}$
Buck converter	$(1 - d_1)$
Boost converter	$d_1(1 - d_1)^2$
Buck-boost family (Buck-Boost, CUK, SEPIC, ZETA)	$(1 - d_1)^2$

From Fig. 9 it shows that the proposed converter has more DCM region compared to other converters. So, the proposed converter has high possibilities to choose different values for parameter 'k'. Table-I shows the boundary conditions for CCM/DCM operations for different converters like boost converter, buck converter, buck-boost family and proposed converter and based on those equations' duty ratio and $K_{critical}$ are plotted.

4. DESIGN OF COMPONENTS

The design analysis of reactive components in the converter L_1, L_2, C_1, Co are discussed in this section. To minimize the output voltage ripple output filter capacitor C_0 is selected as large. So that output voltage V_0 will be constant and output filter will not affect the circuit operation. The input inductance L_1 for lossless converter can be written as

$$L_1 = \frac{d_1^2 V_s^2}{4P_s f_s} = \frac{d_1^2 V_s^2}{4P_0 f_s} \quad (22)$$

For the values d_1=0.30, V_s=60(rms), P_0=65W, and f_s=50 kHz and the inductance L_1 is evaluated as L_1=49uH.

To evaluate the storage capacitor C_1, for low-frequency peak-to-peak capacitor voltage ripple (ΔV_{C1}) can be attained as-

$$\Delta V_{C1} = 2(i_{D1})_{ac_p} X_{C1} = \frac{2(i_{D1})_{ac_p}}{4\pi . f_L C_1} \quad (23)$$

Where $(i_{D1})_{ac_p}$ is peak value of diode current and f_L is line frequency. From figure (3) the line frequency of diode average current i_{D1} is given by

$$(i_{D1}) = \frac{i_{D1p}}{2T_2} d_2 T_s = \frac{d_1 d_2 V_s}{2L_1 f_s} (\sin \omega_L t) \quad (24)$$

Using equation (14) in equation (24), current (i_{D1}) is obtained as

$$(i_{D1}) = \frac{d_1^2 V_s^2}{2L_1 f_s V_{C1}} (sin^2 \omega_L t) = \frac{d_1^2 V_s^2}{2L_1 f_s V_{C1}} \left(\frac{1 - \cos \omega_L t}{2}\right) \quad (25)$$

From equation (25) the low-frequency circulating current through the storage capacitor C_1 and diode D_1 is

$$(i_{D1})_{ac\ content} = \frac{d_1^2 V_s^2 \cos 2\omega_L t}{4L_1 f_s V_{C1}} = (i_{D1})_{ac\,p} . \cos 2\omega_L t \quad (26)$$

Capacitor voltage ripple (ΔV_{C1}) can be attained by using equation (26) from equation (23) is given by

$$\Delta V_{C1} = \frac{d_1^2 V_s^2}{8\pi L_1 f_s f_L V_{C1}} \frac{1}{C_1} \quad (27)$$

The voltage ripple (ΔV_{C1}) of storage capacitance C_1 is given by

$$C_1 = \frac{d_1^2 V_s^2}{8\pi L_1 f_s f_L V_{C1} \Delta V_{C1}} \quad (28)$$

For d_1=0.30, V_s=60(rms), P_0=65W, f_s=50kHz, f_L=50Hz, L_1=49uH, ΔV_{C1}=5.1V, R=5.56Ω the C_1 value is evaluated as C_1=350uF.

Similarly, the output inductance L_2 for a tolerable ripple Δi_{L2} is given by

$$L_2 = \frac{(V_{C1} - V_0) d_1}{f_s \Delta i_{L2}} \quad (29)$$

For d_1=0.30, V_s=60(rms), V_{C1}=100, and f_s=50 kHz, L_2 value is evaluated as L_2=32uH.

Table 2: Circuit parameters

COMPONENT	VALUES
Input voltage (V_s)	60V(rms)
Line frequency(f_L)	50Hz
Switching frequency(f_s)	50KHz
L_1	49uH
L_2	32uH
C_1	350uF
C_0	3000uF
L_f	3mH
C_f	0.4uF
Resistive load(R)	5.56Ω
Duty ratio	0.3

5. RESULTS AND DISCUSSION

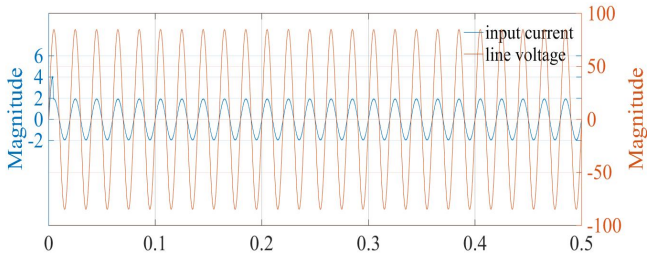

Figure 10(a): Line voltage and input current waveform at $60V_{rms}$

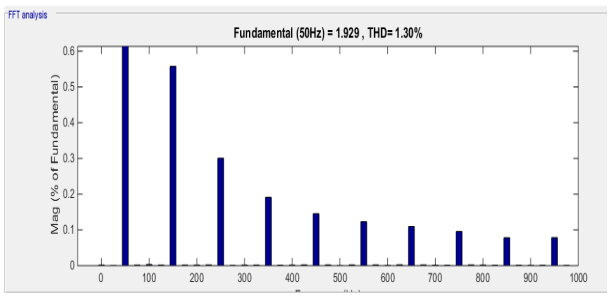

Figure 10(b): Input current harmonic content

The proposed model as shown in Fig. 2 and is simulated using MATLAB/SIMULINK software. The designed parameters of the proposed buck-boost buck converter are tabulated in table-II and components are premeditated based on converter analysis made in prior sections. Input voltage V_s of the converter is assumed to be ideal. The inductor L_1 is operated in DCM and inductor L_2 is operated in CCM. The line voltage and current for different levels of voltages and harmonic content of different currents are shown in Figs. 10-12 and the conduction angle is same for various levels of voltages. The power factor of input current is measured and is shown in Fig. 12 and it is equivalent to 0.999 for three different voltages levels. According to IEC-61000-3-2 limits defined only for a line voltage of 230 V_{rms} but it shows for different voltage levels also. Fig. 13 shows the power factor (d_1=0.3) of input current.

Fig. 10(a) shows line voltage and input current at 60V (rms). It shows that both line voltage and input current are in phase and input current of the converter is pure sinusoidal so that the harmonic content of input current is nearly unity and thus results in less losses and thereby efficiency of the converter increases. Figure 10(b) shows the harmonic content of input current and the %THD value of input current reaches the IEC standards. The %THD value at fundamental frequency is 1.30%.

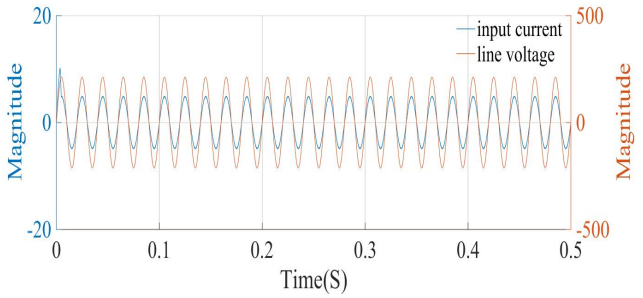

Figure 11(a): Line voltage and input current waveform at 150Vrms

Figure 11(a) shows line voltage and input current at 150V(rms). It shows that both line voltage and input current are in phase and input current of the converter is pure sinusoidal so that the harmonic content of input current is nearly unity and thereby increase in efficiency.

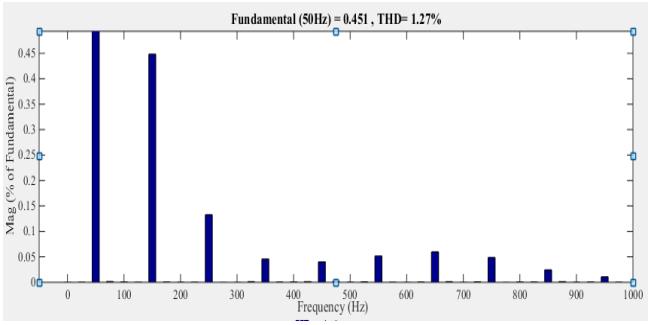

Figure 11(b): Harmonic content of line current

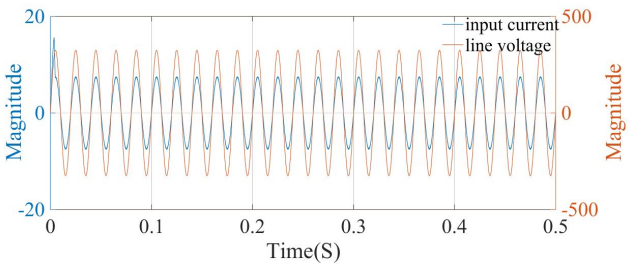

Figure 12(a): Line voltage and input current waveform at 230Vrms

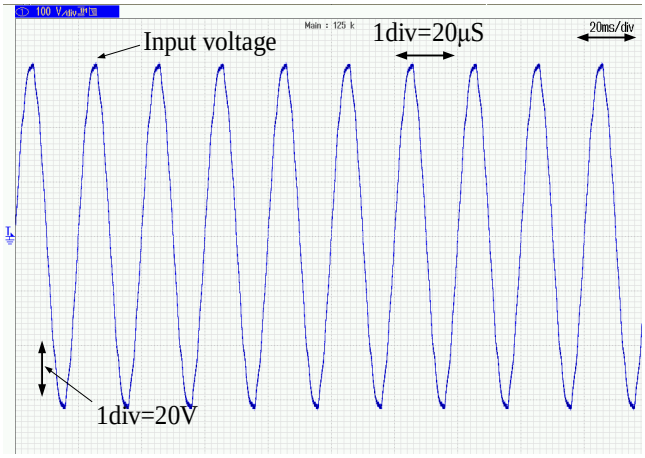

Figure 12(b): Experimental results for line voltage at 230Vrms

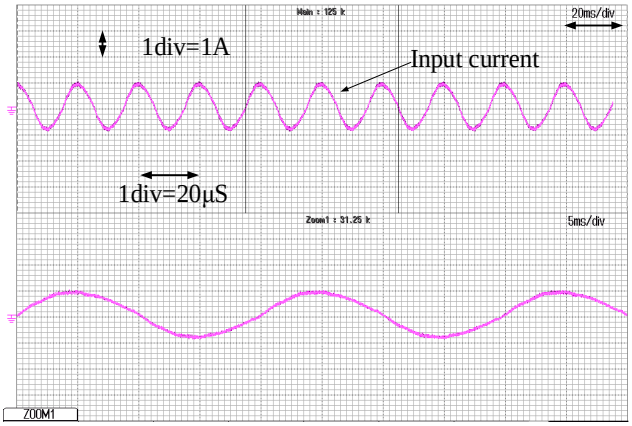

Figure 12(c): Experimental results for input current at 230Vrms

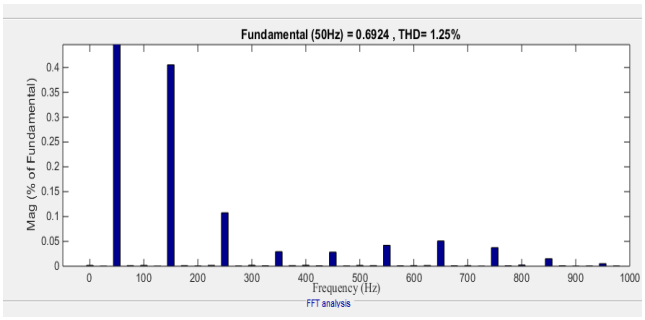

Figure 12(d): Harmonic content of line current

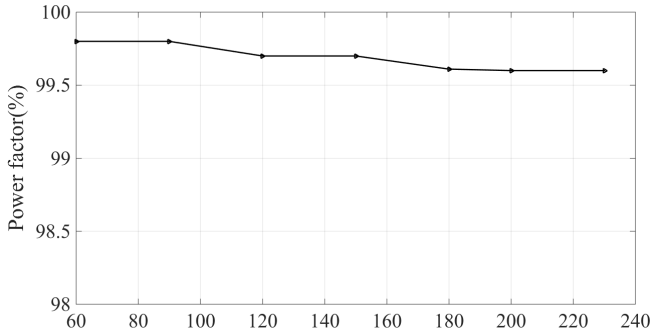

Figure13: Input power factor for universal operating voltage range

Fig. 13 shows the input power factor at different voltage levels and it shows the unity power factor thereby device capacity and size of the equipment can be reduced. The inductors L_1 and L_2 are operated in DCM so the operation of inductors is discontinuous and are represented in Fig. 14(a). The simulation results of inductor current (i_{L1}), output inductor current (i_{L2}) and switch current (i_s) of proposed converter is shown in Fig. 14 (a).

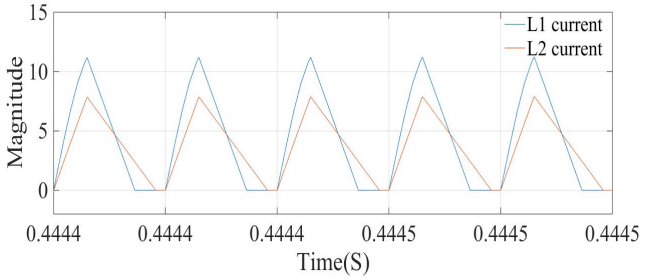

Figure 14(a): Simulation results for i_{L1} and i_{L2}.

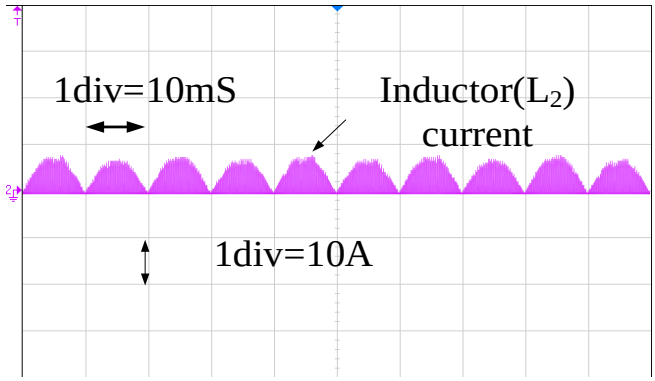

Figure 14(b): Experimental results for output inductor L_2 current

This converter is operated in DCM so that the current in L_1 discharges fast compared to inductor L_2. When converter is operated in DCM current in L_2 starts from zero and ON time is more. Fig. 14(c) shows the switch current when the converter is operated at duty ratio of 0.3(d=0.3). When converter is operated in DCM the switch current is discontinuous.

Fig. 15(a) illustrated the simulation results of switch voltage (V_{sw}) and capacitor voltage (V_{C1}) at 30% duty ratio when the converter is operated in DCM.

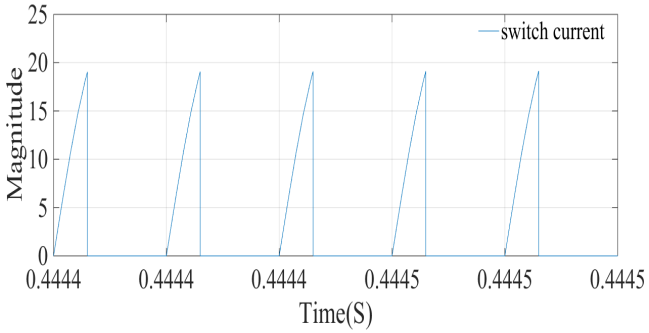

Figure 14(c): Simulation results for switch current (i_s).

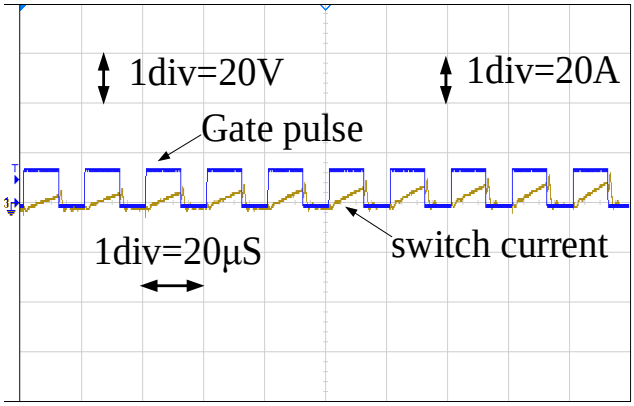

Figure 14(d): Experimental results for switch current and gate pulses

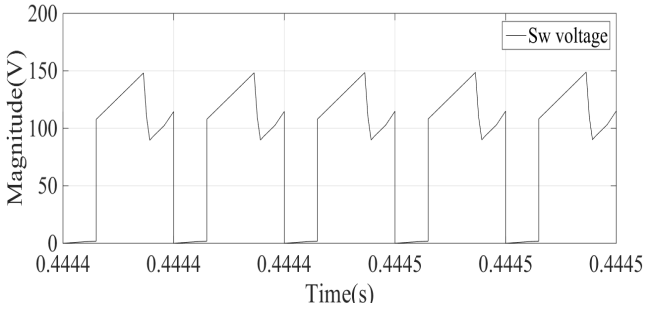

Figure 15(a): Simulation results for switch voltage (V_s).

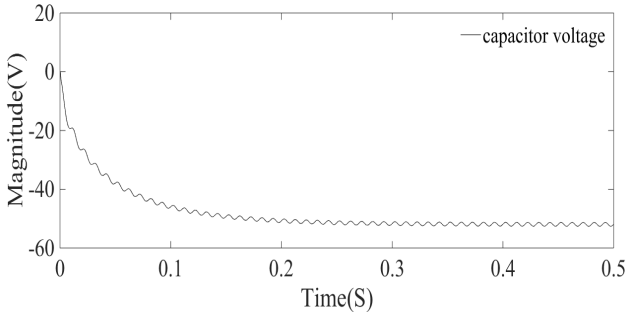

Figure 15(b): Simulation results for capacitor voltage (V_{C1}).

The circuit is operated in DCM then the diode currents in the circuit as illustrated in figure 16. When converter is operated in DCM then the current flow in the diodes is discontinuous.

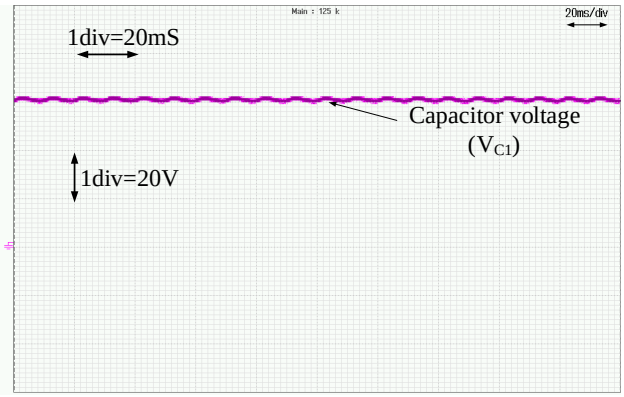

Figure 15(c): Experimental results for capacitor voltage (V_{C1}).

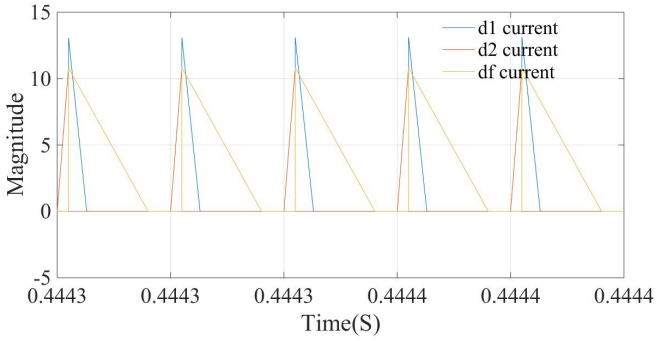

Figure 16: Simulation results for diode-1 current, diode-2 current, free-wheeling diode current.

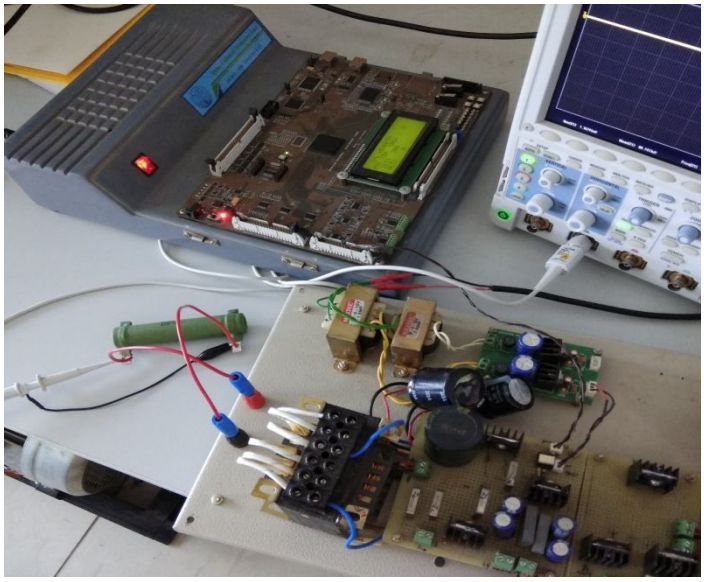

Figure 17: Experimental setup for isolated buck-boost buck converter

From Fig. 18(a) shows the plots for power factor (%), THD (%), capacitor voltage, output voltage with respect to different duty ratio's with constant voltage 60V(rms). From figure it is seen that the power factor for different duty ratios is maintained unity. The %THD of input current is low at 0.3. The capacitor voltage increases with respect to different duty ratios and similarly output voltage gradually increases with respect to duty ratios.

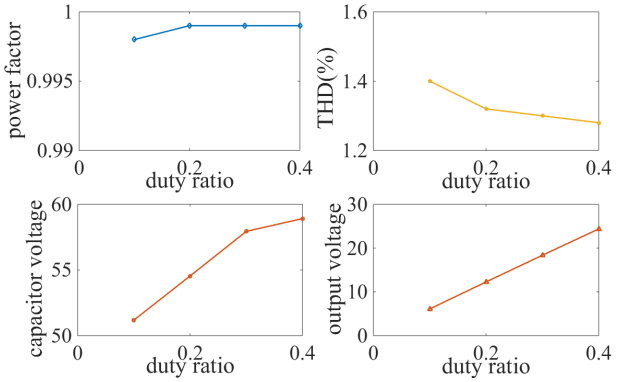

Figure 18(a): Plots for different duty ratio's with power factor, THD (%), capacitor voltage, output voltage.

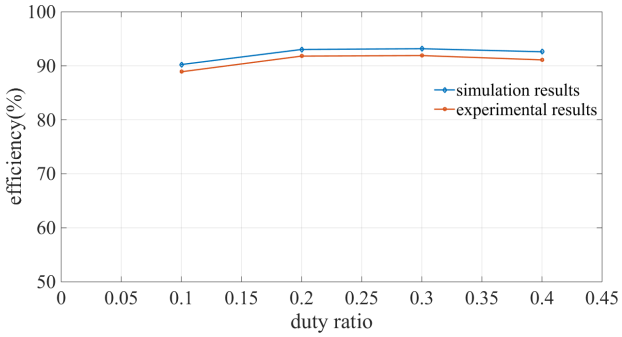

Figure 18(b): Simulation and Experimental results with different duty ratios for efficiency (%).

Fig. 18(b) shows the graph between duty ratios's with efficiency. From this it is seen that at different duty ratio's the efficiency of the converter increases and maintained constant at some particular instants i.e., between 0.2 to 0.3. From this plot it is concluded that above 0.3 duty ratio the converter achieves good efficiency.

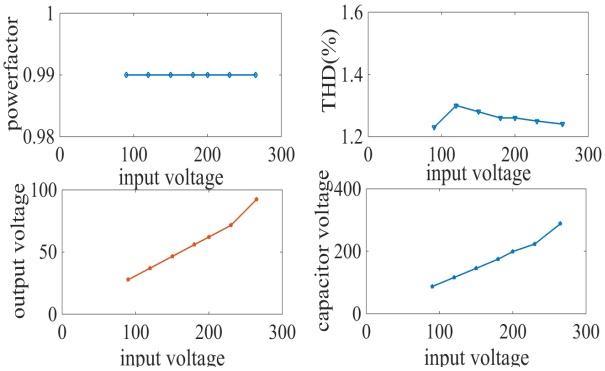

Figure 19(a): Plots for universal operating voltage range with power factor, THD (%), output voltage, capacitor voltage

Fig. 19(a) shows the plots for universal operating voltage range with power factor, THD (%), output voltage, capacitor voltage. Power factor is maintained unity in all cases when duty ratio is 0.3(d=0.3). The THD (%) is very less and reaches the limits of IEEE standards. By this it can be concluded when

this converter is operated at 0.3 duty ratio the input current %THD is very low.

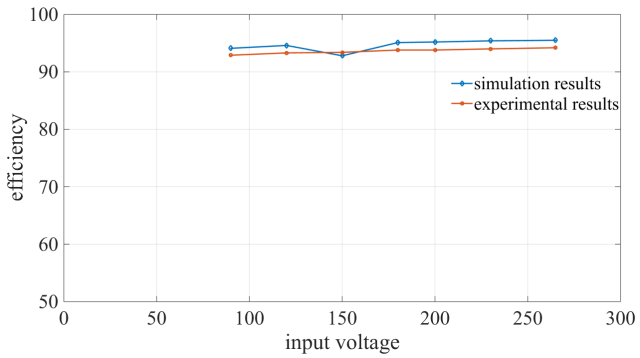

Figure 19(b): Simulation and Experimental results for efficiency at universal operating voltage ranges.

Fig. 19(b) illustrates the simulation and experimental results for efficiencies with respect to input voltage. Compared to simulation results, experimental results show less efficiency due to losses in the converter. The efficiency of the proposed converter is more in simulation results because it is considered in ideal case. In ideal case the switching losses are less compared to hardware.

5. CONCLUSION

A single-stage single switch buck-boost buck isolated converter is proposed for to attain unity power factor and to reduce input current %THD. In this converter buck and buck-boost converters are integrated with an isolated transformer and operated by single switch. The detailed analysis and operation of isolated buck-boost buck converter in DCM is explained with necessary equations and modes. The effectiveness of proposed converter is verified by modeling, 65W, 60V 50Hz converter using MATLAB/SIMULINK software. The input current %THD is measured and it satisfies the IEEE standards and it achieved unity input power factor at fundamental frequency. The proposed converter is tested for universal voltage levels (90V-265V) and from this it is concluded that this converter operates with fast and well-regulated output voltages for lower duty ratio i.e., at d=0.3 in DCM. From these results, the proposed converter achieved unity input power factor, less input current %THD, and high efficiencies for different voltage ranges and different duty ratios.

REFERENCES

1. M. Brkovic and S. Cuk, "**Novel single stage ac-to-dc converters with magnetic amplifiers and high power factor**," in Proc. IEEE Appl. Power Electron. Conf., 1995, pp. 447-453.
2. Nagi Reddy. B, O. Chandra Sekhar, M. Ramamoorty, "**Analysis and implementation of single-stage buck-boost buck converter for battery charging applications**"; Journal of Advanced Research in Dynamical and Control Systems (JARDCS), Vol. 10, No. 4, April 2018, pp 462-475.
3. M. T. Madigan, R.W. Erickson, and E. H. Ismail, "**Integrated high quality rectifier-regulators**," IEEE Trans. Ind. Electron., vol. 46, no. 4, pp. 749–758, Aug. 1999. https://doi.org/10.1109/41.778229
4. Nagi Reddy. B, A. Pandian, O. Chandra Sekhar, M. Ramamoorty, "**Performance and Dynamic Analysis of Single Switch AC-DC Buck-Boost Buck Converter**". International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol. 8, No. 4, Feb 2019, pp 68-72.
5. Nagi Reddy. B, O. Chandra Sekhar, M. Ramamoorty, "**Implementation of zero-current switch turn-ON based buck-boost buck type rectifier for low power applications**". International journal of electronics, https://www.tandfonline.com/doi/full/10.1080/00207217.2019.1582711. Vol.106, No.8.
6. R. Redl, L. Balogh, and N. O. Sokal, "**A new family of single stage isolated power factor correctors with fast regulation of the output voltage**," in Proc. IEEE Power Electron. Spec. Conf., 1994, pp. 1137–1144.
7. M. M. Jovanovic, D. M. Tsang, and F. C. Lee, "**Reduction of voltage stress in integrated high quality rectifier regulators by variable frequency control**," in Proc. IEEE Appl. Power Electron. Conf., 1994, pp. 569–575.
8. M. J. Willers, M. G. Egan, J. M. D. Murphy, and S. Daly, "**A BIFRED converter with a wide load range**," in Proc. IEEE Int. Conf. IECON, 1994, pp. 226–231.
9. Nagi Reddy. B, A. Pandian, O. Chandra Sekhar, M. Rammoorty, "**Design of Non-isolated integrated type AC-DC converter with extended voltage gain and high power factor for Class-C&D applications**". International Journal of Recent Technology and Engineering (IJRTE), Vol. 7, No. 5, Jan 2019, pp 230-236.
10. L. Sri Sivani, Nagi Reddy B, K. Subba Rao, A. Pandian, "**A New Single Switch AC/DC Converter with Extended Voltage Conversion Ratio for SMPS Applications**". International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol. 8, No. 3, Jan 2019, pp 68-72.
11. Rekha R., Srikanth Goud B., Rami Reddy C., Nagi Reddy B. (2020) **PV-Wind-Integrated Hybrid Grid with P&O Optimization Technique**. Innovations in Electrical and Electronics Engineering. Lecture Notes in Electrical Engineering, vol 626. Springer, Singapore. https://doi.org/10.1007/978-981-15-2256-7_53
12. B.S. Goud, B.L. Rao, B.N. Devi, K.S. Kumar, N. Keerthi, "**Review On Optimization Techniques Employed In Distribution Generation**", Journal of Critical Reviews, Vol. 7, No. 2, pp. 639-645, 2020.
13. M. Kiran Kumar, Nagi Reddy. B, N. Rajesh. "**Harmonic Mitigation And Power Quality Enhancement Using PV Fed Series Active Filter For Grid Systems**". International Journal of Scientific & Technology Research, **Volume 9 - Issue 1, January 2020 Edition.**