Realization with Fabrication of Parallel-Gate MOSFET Based Differential Amplifier

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ABSTRACT

Differential amplifiers are widely used for their ability to reject common-mode noise. The differential amplifier may be implemented using BJTs and MOSFETs. It is a commonly used building block in analog IC design.In this research work, the differential amplifier has been designed with Parallel-Gate (PG) MOSFET. To explain this model, first, the basic differential amplifier has been discussed, and after that, it has been structured with PG MOSFET.To analyze this differential amplifier a signal conditioning unit has been used and set at $V_{i1} = V_{i2} = 3.05$ V, 4.05 V, and 5.0 V dc and current mirror circuit atcurrent2 mA to measure the ac differential voltage gain $(V_{o1} − V_{o2})/ (V_{i1} − V_{i2})$. Due to two transistor the hamming / noise canceled each other, and a clear output signal can be achieved.

Key words: Double-gate MOSFET, differential amplifier, Low power device, Transistor, Microelectronics, VLSI.

1. INTRODUCTION

The primary function of a differential amplifier is to produce a linearly amplified output signal (of the small difference between two input signals) while rejecting the common part of the two input signals[1]-[6]. The differential amplifier is widespread and it is used in a variety of analog circuits. It is a fundamental building in operational amplifiers [7]-[10].

Deferm and Reynaert[11] have proposed a differential design technique for W-band CMOS applications. In this work, the transformers are used as passive matching circuits, which provide various advantages compared to the traditional circuits.Wilson *et al.* [12] have designed a fully differential, low-power current-starving inverter-based amplifier topology designed at 0.18-μm process. This design achieves 46 dB dc gain and 464 kHz unity gain frequency with a power consumption of 145.32nW at 700mV power supply voltage for ultra-low power, low bandwidth applications. Vural *et al.* [13]have presented an efficient constrained optimization method for the sizing of differential amplifier with current mirror load. Thienen and Reynaert [14] have designed a 160-GHz fully-differential power amplifier in 40-nm CMOS. A tapered gate connection network was optimized which results in the reduction of gate resistance and allows to achieve a maximum gain of 11.6 dB with 3-dB bandwidth of24 GHz from the three-stage amplifier. The achieved saturated output power was 4.1 dBm, and 1-dB compression power was 1.5 dBm.

Saso *et al.* [15] have designed a class-AB one-stage fully differential amplifier, which includes adaptive biasing techniques to the conventional class-A differential amplifier. It improves the linearity, gain-bandwidth product, and slew rate, while maintaining the same DC bias currents and supply voltage requirements. Khateb *et al.* [16] have presented a low-voltage low-power CMOS structure for the fully differential difference transconductance amplifier. This circuit employs the QFG technique to achieve a simple CMOS topology and class-AB output stages. Maundy *et al.* [17] have revisited the common-base differential amplifier. Thereafter, derived a new differential input-output filters for the common-base differential amplifier as well as a low impedance Norton amplifier. The simulations in 90-nm UMC CMOS process of several filters, as well as experiments conducted using discrete transistors, confirm the theoretical results. Srivastava *et al.* [18], [19] have designed the double-gate MOSFET based differential amplifier and class-AB amplifier, respectively. This present research work is in continuation of these works.

In the thicker fully-depleted MOSFETs, a current undershoot is normally observed when the front gate is biased inversion. An advantage of extremely thin devices is that they do not suffer from such transients, simply because the back interface cannot be driven in accumulation[20]-[23]. In the scaled devices, the total number of channel dopants decreases, resulting in a larger variation of dopant numbers and hence significantly impacting the threshold voltage [24], [25].

In this present research work,authors have designed a novel differential amplifier with parallel-gate MOSFET. Thereafter, its various parameters have been analyzed, including the fabrication of the device and testing. The work presented in the paper has been organized as follows: Section 2 describes the basics of differential amplifier theories. On the basis of small-signal model of the parallel-gate MOSFET

a differential amplifier has been proposed in the Section 3. The Section 4 has the fabricated model of this amplifier in terms of printed circuit and its result analysis. Finally, Section 5concludes the work and recommends the future aspects.
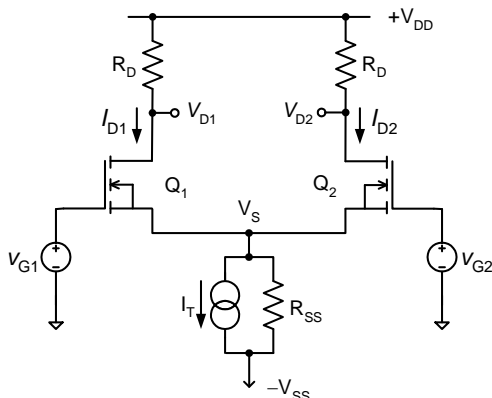

Figure 1: Basic MOSFET based differential amplifier.

2. BASIC OF AMPLIFIERS AND ITS COMPONENTS

The differential amplifier responds to the difference between the two applied input signals and ideally rejects signals that are common to both inputs. The basic MOSFET differential pair is shown in Fig. 1. These MOSFETs are assumed identical (matched), and the dc biasing is controlled by a constant current source [24], [25]. The differential amplifier amplifies only the differential input signal and rejects the common-mode input signal completely. This section deals and revisited the basic theories of differential amplifiers and its parameters.

2.1 Differential & Common-Mode Signals and CMRR

It is convenient to represent the input signals to different amplifiers by their differential and common mode components. Two input voltages V_1 and V_2 applied to the terminals of the differential amplifier. The differential input signal v_{id} is the difference between the two input signals V_2 and V_1 i.e., $v_{id} = V_2 - V_1$. The common-mode input signal $v_{i, cm}$ is the average of the two input signals i.e. $v_{i,cm} = (v_1+v_2)/2$. The efficiency of a difference amplifier is measured by the degree to which it amplifies the necessary differential component and rejects the unwanted common-mode component. This measure is usually expressed by a quantity called the Common-Mode Rejection Ratio (CMRR) defined as [20], [25]-[27]:

$$CMRR = \frac{|A_{vd}|}{|A_{vcm}|} \quad (1)$$

where $A_{vd} = \left.\frac{v_o}{v_{id}}\right|_{v_{icm}=0}$ is the differential voltage gain, and $A_{vcm} = \left.\frac{v_o}{v_{icm}}\right|_{v_{id}=0}$ is the common-mode voltage gain.

A. DC Analysis

The dc analysis can be simplified by making the assumptions that the current source's output resistance is infinite: $R_{SS} = \infty$ (means the current source is ideal, i.e. the current source provides the specific required current to derive the circuits) [20], [25], [26].Initially, for testing (calibration)$V_{G1} = V_{G2} = 0$ was assumed. From the circuit's symmetry, it is obvious that the bias tail current (I_T, also known as currents, coming from source) will be divided equally between the two MOSFETs, so$I_{D1} = I_{D2} = I_T/2$. Assuming the MOSFETs are biased into the saturation region, the voltage at each drain will be $V_{D1} = V_{D2} = V_{DD}-I_D.R_D$.In this circuit, V_{GS}can be determined using the usual single-gateMOSFET saturation mode [20]-[22], [25], [26] as:

$$I_D = \frac{1}{2}k'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 \quad (2)$$

Since $V_S = -V_{GS}$ hence$V_{DS} = V_D-V_S = V_{DD}-I_D.R_D+V_{GS}$ and for saturation $V_{DS} \geq V_{GS} - V_T$.

B. Small-Signal Operation

For MOSFETs, the small-signal operation is easiest analysed by considering the circuit response to the differential and common-mode components of the signals separately and working with the relevant half-circuit model for each case. In the following analysis, external load resistance R_L has been omitted as this will depend on the specific application, hence where necessary, $R_D$is replaced by $R'_L = R_D // R_L$ as appropriate [20], [25], [26].The differential pair's output may be taken differentially between the two drains (known as differential output)$v_{od} = v_{D1}- v_{D2}$. If the output is taken from one drain w.r.t. source (single-ended output) is$v_{os} = v_{D1}$or $v_{os} = v_{D2}$[20], [27]-[29].

a) Pure differential signals:

Considering the basic (single-gate) MOSFET differential pair with differential signals applied as in Fig.2. For pure differential signals, points on the symmetry line are virtual ground. The dc supply rails are signal grounds, and at points x in Fig. 2(a), (by symmetry), the increase in signal current in one MOSFET is exactly matched by the decrease in signal current in the other MOSFET hence the signal voltage at x will be zero [4], [25]-[29].
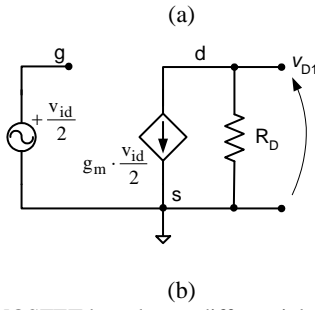
(a)

(b)
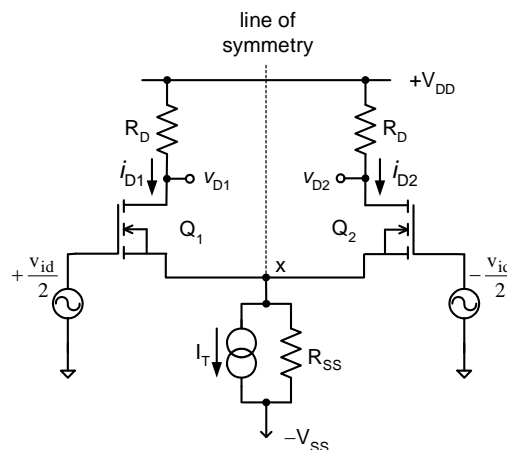
Figure 2: (a) MOSFET based pure differential amplifier, and (b) its equivalent half-circuit.
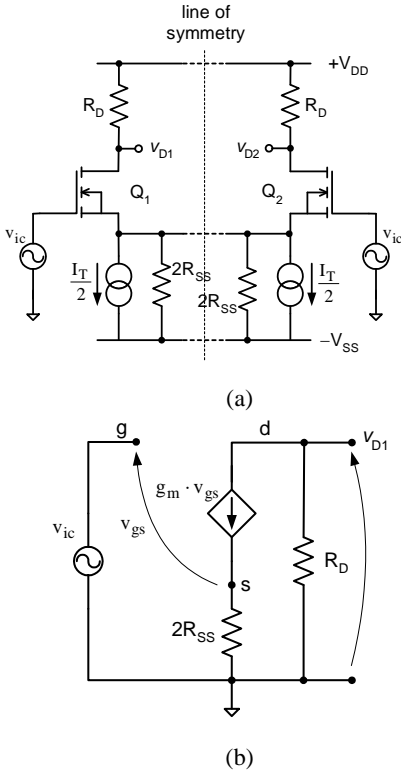

(a)

(b)

Figure 3: (a) MOSFET based pure common-mode amplifier and (b) its equivalent half-circuit.

Hence for differential signals, the circuit is effectively two identical half-circuits, each comprising a common-source MOSFET with opposite polarity differential signal. An equivalent half-circuit is drawn as in Fig.2(b) and MOSFET has been replaced by an appropriate π-model. From this equivalent half-circuit [20], [25]-[27], [29]:

$$A_{Vd} = \frac{v_{od}}{v_{id}} = \frac{v_{D1} - v_{D2}}{v_{id}} = \frac{-g_m \frac{v_{id}}{2} R_D}{\frac{v_{id}}{2}} = -g_m R_D \text{(3a)}$$

$$A_{Vds} = \frac{v_{os}}{v_{id}} = \frac{v_{D1}}{v_{id}} = \frac{-g_m \frac{v_{id}}{2} R_D}{2\frac{v_{id}}{2}} = -\frac{1}{2}(g_m R_D) \text{(3b)}$$

b) *Pure common-mode signals:*

The differential pair (symmetric) with common-mode signals is shown in Fig.3. For pure common-mode signals points on the line of symmetry are open circuits since there are no

current flows in these links [17], [25], [29]-[32].Hence for common-mode signals, the circuit is effectively two identical half-circuits, each comprising a MOSFET (common-source connection with R_S). An equivalent half-circuit has been drawn in Fig.3(b) using π-model.If the output is taken single-ended, then from the equivalent half-circuit of Fig.3(a):

$$A_{Vcs} \frac{v_{D1}}{v_{ic}} = \frac{-g_m v_{GS} R_D}{v_{GS} + g_m v_{GS} 2R_{SS}} = -\frac{R_D}{2R_{SS}} \quad (\text{if } g_m 2R_{SS} >> 1) \text{ (4)}$$

$$\text{CMRR} = \left| \frac{A_{Vds}}{A_{Vcs}} \right| = \frac{g_m R_D}{2} \cdot \frac{2R_{SS}}{R_D} = g_m R_{SS} \text{(5)}$$

To improve these existing circuits, authors have replaced the single-gate MOSFET with the parallel-gate MOSFET, which is the novelty of this work.

2.2 Introduction of Parallel-Gate (PG) MOSFET

A large number of gates provide improved electrostatic control of the channel, so that the Si body thickness and width can be larger than the double-gate MOSFET structures. They are tied together electrically and are self-aligned with each other and the source/drain regions [33], [34]. The DG MOSFET significantly suppressed the Short Channel Effects (SCE), reduced Drain Induced Barrier Lowering (DIBL), excellent scalability with the device scaling. It uses the volume inversion phenomenon, where the carriers flow inside the Silicon layer and improving the carrier mobility [35], [36].

The behavior of switches, with multiple gates, depends on the number of gates, which controls the device's operational process. Therefore, various logic functions can be implemented into a single device. The independent double-gate transistors can be used to implement the universal logic functionality within a single transistor [25], [35]. So, this design is suitable and useful to analyze further for these types of specific applications. However, the differential amplifier with DG MOSFET experiences the minimal distortion and negligible voltage fluctuation [18], [19].

Better conformity between the simulations and analysis of the proposed model has been achieved using the parallel-gate MOSFET.Since the logic density of a transistor can be increased with independently controlled MOSFET [25]. The independent gate option can be useful for low power and mixed-signal applications [37], [38], and such developments at the device level provide opportunities to design various novel circuit for the low-power high-performance devices. The parallel-gate technique gives rise to many performance enhancements e.g. increased transconductance, lowered threshold voltage, etc. [39].

As the channel length of MOSFET is reduced, the drain potential begins to influence the channel potential. This short channel effect is mitigated by thin gate oxide and thin depletion width below the channel to the substrate to shield the channel from the drain. Therefore, as MOSFET scaling becomes limited by leakage currents, parallel-gate offers the

opportunity to proceed beyond the performance of single-gate bulk-Silicon MOSFET [40].

In DG MOSFET, two channels are separated by sufficient distance to be independent of each other, which creates two independent transistors on the same piece of Silicon. Therefore, in this proposed design, two transistors as an alternative to the DG MOSFET have been used. Each gate can control one-half of the device, and its operation is independent of each other, which is obvious in this design. The equivalent current through the device is the sum of currents in the separate channels and it uses traditional current equations [41]-[48]. When a proper model and a set of parameters are used, its accurate model can be design. A model is normally represented by an equivalent circuit consisting of elements e.g. resistances, capacitances, inductances, voltage sources, current sources, and heat sink. However, some of them may result from empirical experiences to enhance the model accuracy.

3. PROPOSED DIFFERENTIAL AMPLIFIER AND ITS MATHMATICAL MODELING

To design the circuit, authors have replaced the single-gate MOSFET (Fig.1) with the parallel-gate MOSFET. The basic PG MOSFET differential pair is shown in Fig.4, where both PG MOSFETs are assumed identical (matched), and the dc biasing is controlled by a constant current source.This differential amplifier is designed to provide the amplified difference between two input signals. In Fig.4, there are two inputs (V_{G1} and V_{G2}) applied on the gate terminal of the transistor and two outputs (V_{D1} and V_{D2}) taken from the transistors' drain terminals. The source of both transistors Q_1 and Q_2 are connected to a common source resistor (R_{ss}). The V_{DD} and V_{SS} are the two supply voltages for the circuit. The opposite points of both the positive and negative voltage supplies are connected to the ground. This circuit has been analyzed with various aspect as follows:
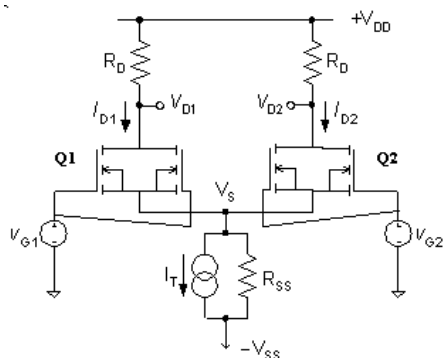

Figure 4: Proposed model of the differential amplifier based on parallel MOSFET.

A. The DC Analysis

The dc analysis can be simplified by making the assumptions that the output resistance of the current source is infinite: $R_{SS} \rightarrow$ infinite (means the current source is ideal, i.e. the current source is providing the specific required current to derive the circuits).Initially, for testing (calibration),

$V_{G1a} = V_{G1b} = V_{G2a} = V_{G2b} = 0$, where V_{G1a} and $V_{G1b}$are the gate voltages of transistor *a* and transistor *b* (left-hand section) and V_{G2a} and $V_{G2b}$are the gate voltage of transistor *a* and transistor *b* (right-hand section). From the symmetry of the circuit it is obvious that the bias tail current (I_T) will be divided equally between the four MOSFETs so $I_{D1a} = I_{D1b} = I_{D2a} = I_{D2b} = I_T/4$,where I_{D1a} and $I_{D1b}$are the drain current of transistor *a* and transistor *b* (left-hand section) and I_{D2a} and $I_{D2b}$are the drain current of transistor *a* and transistor *b* (right-hand section). Assuming the MOSFETs are biased into the saturation region, then the voltage at each drain will be $V_{D1a} = V_{D1b} = V_{D2a} = V_{D2b} = V_{DD} - I_D/4 \cdot R_D$. Here, V_{GS} may be determined using the usual MOSFET saturation mode as in Eq. (2) [20], [25], [26] and hence:

$$V_{GS} = V_t + \sqrt{\frac{2 \cdot I_D}{k'\left(\frac{W}{L}\right)}} = V_t + \sqrt{\frac{I_T}{k'\left(\frac{W}{L}\right)}} \qquad (6)$$

$V_s = -V_{GS}$ hence $V_{DS} = V_{DD} - I_D.R_D + V_{GS}$ and for saturation $V_{DS} \geq V_{GS} - V_t$.

B. Small-Signal Analysis

The small-signal model is analyzed by considering the circuit response to the differential and common-mode components of the signals separately and working with the relevant half-circuit model for each case.

a) Pure differential signals

The parallel-gate MOSFET differential pair with differential signals applied is shown in Fig.5(a). For pure differential signals, points on the line of symmetry are virtual grounds. Hence for differential signals, the circuit is effectively two identical half-circuits, each comprising of two parallel MOSFET with opposite polarity differential signal components applied. Its equivalent half-circuit π-model) is shown in Fig.5(b).
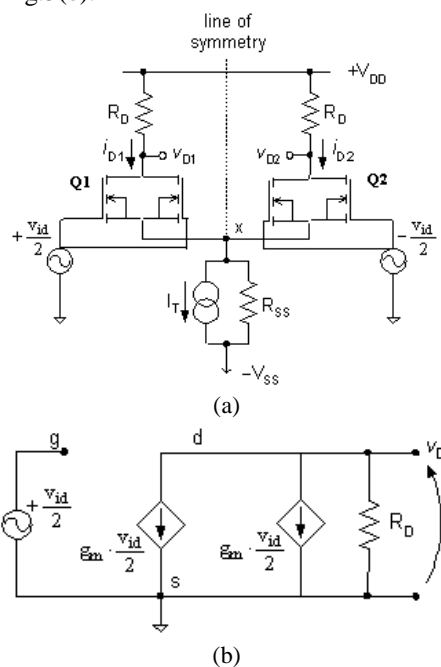

(a)

(b)

Figure 5: (a) Parallel-gate MOSFET based pure differential amplifier and (b) its equivalent half-circuit.

The small-signal equivalent circuit has been simplified to effectively two half-circuits each of the parallel-gate MOSFET circuit. From the equivalent half-circuit:

$$A_{Vd} = \frac{v_{od}}{v_{id}} = \frac{v_{D1} - v_{D2}}{v_{id}} = -\frac{g_m v_{id} R_D}{\frac{v_{id}}{2}} = -2g_m R_D \quad (7a)$$

$$A_{Vds} = \frac{v_{os}}{\frac{v_{id}}{2}} = \frac{2v_{D1}}{v_{id}} = -\frac{2g_m v_{id} R_D}{v_{id}} = -2g_m R_D \quad (7b)$$

b) Pure common-mode signals

The parallel-gate MOSFET differential pair in the fully-symmetric form with identical common-mode signals applied is shown in Fig.6(a).Hence, for common-mode signals, the circuit is effectively two identical half-circuits, each comprising a parallel-gate MOSFET with equal common-mode signal components applied. Its equivalent half-circuit π-model is shown in Fig. 6(b). If the output is taken single-ended, then from the equivalent half-circuit:

$$A_{Vcs} = \frac{v_{D1}}{v_{ic}} = \frac{-2g_m v_{GS} R_D}{v_{GS} + 2g_m v_{GS} 2R_{SS}} = -\frac{R_D}{R_{SS}}, \text{ if } 2g_m 2R_{SS} >> 1 \quad (8)$$

Hence,

$$\text{CMRR} = \left| \frac{A_{Vds}}{A_{Vcs}} \right| = 2g_m R_D \frac{R_{SS}}{R_D} = 2g_m R_{SS} \quad (9)$$
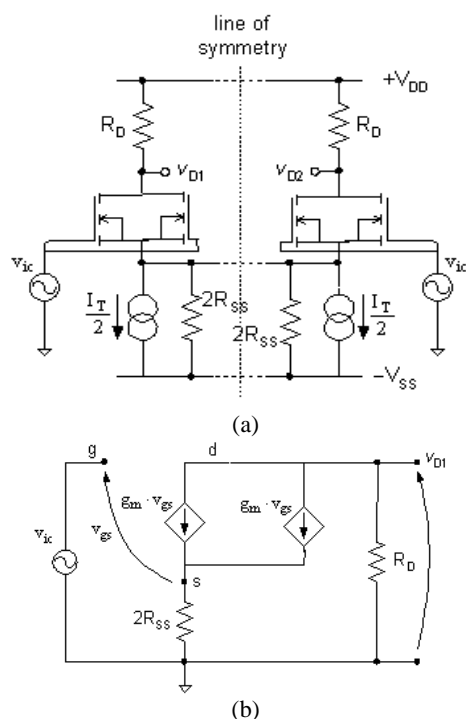

(a)

(b)

Figure 1:(a) Parallel-gate MOSFET based pure common-mode amplifier, (b) Its Equivalent half-circuit.

ComparingEq. (5) and Eq. (9), it is shown that the CMRR is twice for the parallel-gate MOSFET differential amplifier as compared to the basic MOSFET based differential amplifier.

4. CIRCUIT DESIGNING OF PROPOSED DIFFERENTIAL AMPLIFIER AND ITS RESULT ANALYSIS

The implementation of the full system has been designed as prototype. A differential amplifier has been designed to allow for isolated testing of the differential amplifier and the system's individual stages. The bread-board circuit has been designed in compliance with highlighted requirements with regards to drilling sizes, track sizes, and the overall circuit size [32], [33], [41], [49]-[52].

Connections has been done for the differential amplifier module and its associated component and equipment, according to Fig.4 in the Fig. 7 at various stages. Signal conditioning unit (current source) has been used to provide current of 3.06 mA, 4.06 mA, and 5.0 mA in R_{ss}. This can be done with a rotator switch of the signal conditioning unit. After that, all dc voltages have been measured (currents can also be measured) in the circuit with $V_{i1} = V_{i2}$= 3.06 V, 4.06 V, 5.0 V, and with potentiometer adjusted so that $V_{o1} = V_{o2}$.For the parallel-gate MOSFET section all four voltages ($V_{i1a} = V_{i1b} = V_{i2a} = V_{i2b}$) has been set to 3.06 V, 4.06 V, 5.0 V.

Thereafter, the ac differential voltages of the amplifier have been measured at *1kHz*(this frequency can be varied according to the specific application) at an output level of $1V_{p-p}$ at each output. When the mode switch is in the normal position, then signal conditioning unit provides two signals *180°* out of phase, with a common dc bias control voltage which may be varied between about *3.0 V* to *6.0 V*. This variation also depends on the type and internal construction of signal conditioning circuit.These readings have been taken by the oscilloscope to measure all the ac voltages.

The differential input resistance of the amplifier can be varied by the potentiometer. This may be implemented by measuring the ac voltage drop. The ac voltages on both sides of the sensing resistor have been measured and subtracted them to determine the voltage drop (if any), but in this design, it has been set such that this voltage drop is zero. Determining the voltage range of the dc common-mode signal that can be applied to the amplifier's input terminals without affecting the differential voltage gain. The ac differential signal conditions have been set at fix, as it is calibrated in starting.

A. For DC Analysis

In this section, dc analysis for the differential amplifier based on the (i) single-gate MOSFET and the (ii) proposed parallel-gate MOSFET have been performed. For this purpose, the setup has been established in the laboratory, and the devices and instruments used have been shown in Fig. 7 and Fig. 8. Thereafter, reading and calculation have been done. The details of each working process have been written as the name of the figure for easy understanding.
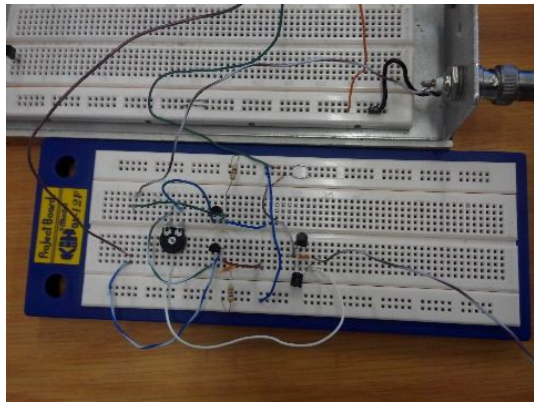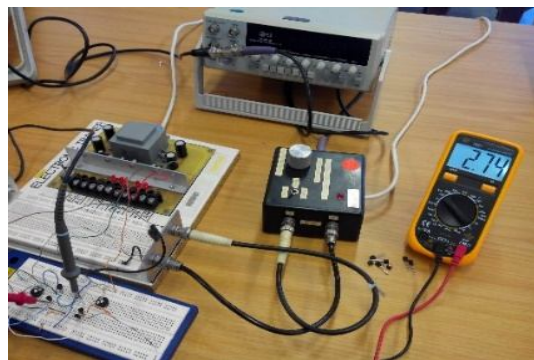
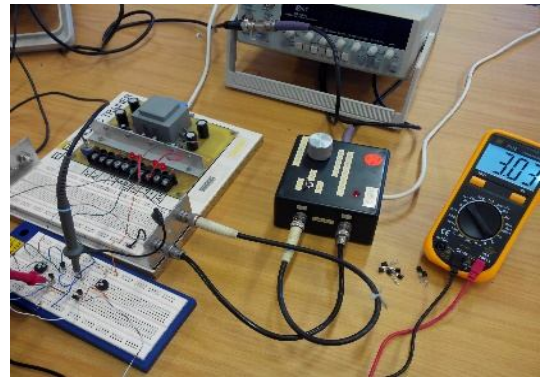(a) Basic circuit of a differential amplifier with MOSFET.
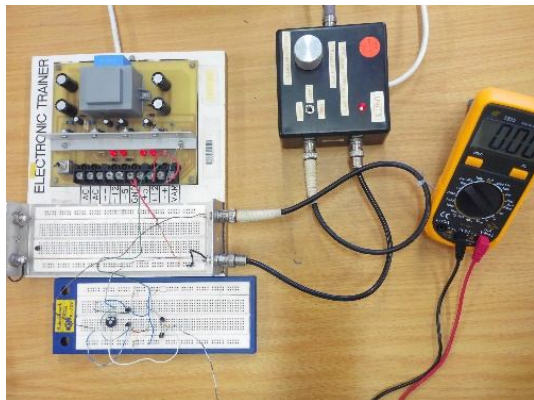
(b)Starting point (calibration of the circuits and testing devices).
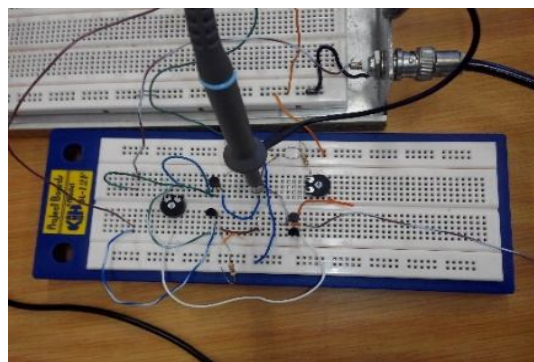
(c)Testing probe procedure.

(d) Observation of the drain voltage of the differential amplifier with MOSFET.

(e) Observation for the input differential amplifier with MOSFET.

Figure 7: Design and measurements steps / process of the single-gate MOSFET based differential-amplifier.
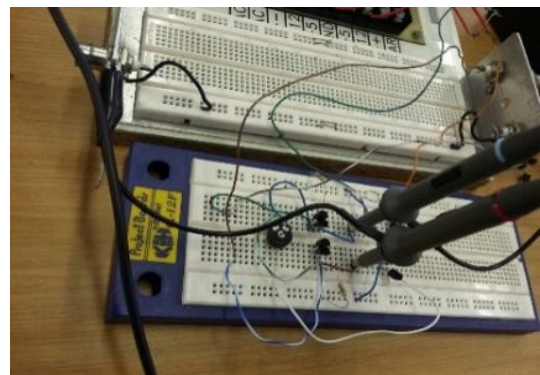

Figure 8: Probe connection for the observation of output for a differential amplifier with parallel-gate MOSFET.

Now a circuit has been designed with the parallel-gate MOSFET, and testing procedure has been followed as above. This Fig. 8 has the probe connection for the observation of output for a differential amplifier with parallel-gate MOSFET. The reading has been recorded for both the cases (i) with single-gate MOSFET in Table 1 and (ii) with parallel-gate MOSFET in Table 2.

Differences between the outputs are doubled (0.35 V at the input of 3.06 V) for the designed parallel-gate MOSFET based amplifier as compared to the single-gate MOSFET (0.14 V at the input of 3.06 V) based amplifier. For the higher input voltage, these MOSFETs reach on the saturation stage, so there is not much difference at the higher voltages (at 4.05 V and 5.00 V).

Table 1:DC analysis for Single-Gate MOSFET (units are in Volts)

V_{i1} (Applied)	V_{S1} (Measured)	$V_{o1} = V_{D1}$ (Measured)	V_{i2} (Applied)	V_{S2} (Measured)	$V_{o2} = V_{D2}$ (Measured)	Difference between V_{o1} and V_{o2}
3.06	2.74	3.03	3.06	2.64	2.89	0.14
4.06	3.30	3.37	4.06	3.28	3.33	0.04
5.00	4.14	4.26	5.00	4.09	4.23	0.03

Table 2:DC analysis for Parallel-Gate MOSFET (units are in Volts)

| V_{i1} (Applied)	V_{S1} (Measured)	$V_{o1} = V_{D1}$ (Measured)	V_{i2} (Applied)	V_{S2} (Measured)	$V_{o2} = V_{D2}$ (Measured)	Difference between V_{o1} and V_{o2}
3.06	2.88	3.01	3.06	2.51	2.64	0.35
4.06	3.33	3.38	4.06	3.31	3.34	0.04
5.00	4.25	4.28	5.00	4.23	4.25	0.03

This high difference voltage is expected due to the parallel-gate MOSFETs as they have two channels to flow the current twice as compared to the single-gate MOSFET. Therefore, this design is suitable for the application where higher voltage difference is required with size constraint. As there are two MOSFETs are used, so CMRR is better as both transistors reject the common noises.

B. For AC Analysis

In this section, ac analysis for the differential amplifier based on the (i) single-gate MOSFET in Fig. 9 and the (ii) proposedparallel-gate MOSFET in Fig, 10 have been performed. For this purpose, the setup has been established in the laboratory, and the devices and instruments used have been shown in following figures. Thereafter, reading and calculation have been done. These results have been presented in Table 3 and Table 4, respectively.
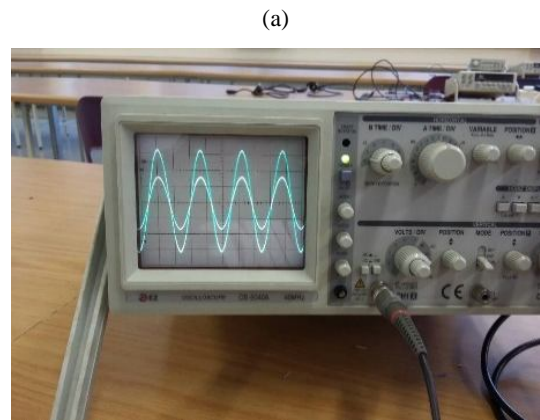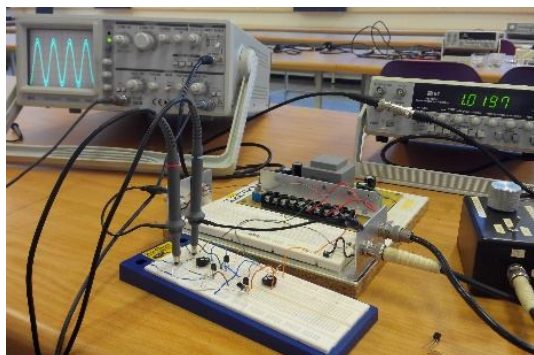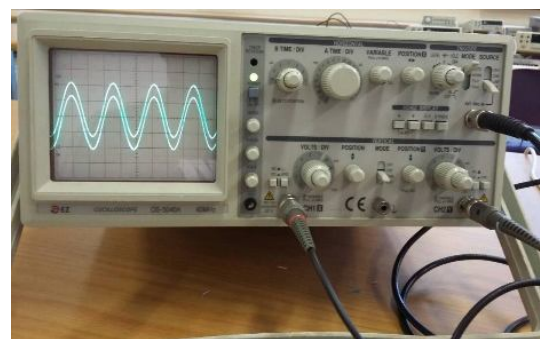

(a)
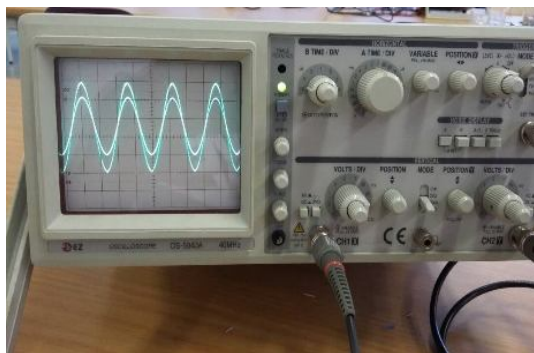
(b)

Figure 9: (a) Circuit setup, and (b) Observation for the output of the differential amplifier with MOSFET.

(a)

(b)

(c)

Figure 10:(a) Observation, (b) amplifier output, and (c) common-mode output of the differential amplifier with parallel-gate MOSFET.

Table 3:AC analysis for Single-Gate MOSFET (units are in Volts)

V_{i1} (Applied)	V_{i2} (Applied)	V_{01} (Measured)	V_{02} (Measured)	Difference between V_{o1} and V_{o2}
0.12	0.14	0.060	0.104	0.44

Table 4:AC analysis for Parallel-Gate MOSFET (units are in Volts)

V_{i1} (Applied)	V_{i2} (Applied)	V_{01} (Measured)	V_{02} (Measured)	Difference between V_{o1} and V_{o2}
0.12	0.14	0.068	0.132	0.64

Differences between the outputs are increased (0.64 V at different inputs of 0.12 V and 0.14 V) for the parallel-gate MOSFET based amplifier compared to the single gate MOSFET (0.44 V at different inputs of 0.12 V and 0.14 V) based amplifier.

This high difference output voltage is expected due to the parallel-gate MOSFETs as they have two channels to flow the current twice as compared to the single-gate MOSFET. Therefore, this proposed design is suitable for the application where higher voltage difference is required with size constraint. As here are two MOSFETs used, CMRR is better as both transistors are rejecting the common noises.

5. CONCLUSIONS AND FUTURE RECOMMENDATIONS

The design of the parallel-gate MOSFET differential amplifier has better and wider output as compared to the single-gate MOSFET differential amplifier. Finally, on the basis of the theoretical analysis and after that practical approach, it can be concluded that the designed differential amplifier has a better solution to improve the CMRR and an extensive output.

In the existing differential amplifier (with single transistor), hamming / noise exists due to the power supplies in a single transistor. Due to *two* transistors the hamming / noise canceled each other, and a clear output signal can be achieved. Since the *two* transistors model of amplifier takes a large space/area in the full circuits, so MOSFET (a replacement of BJT) has been used.

In future, this differential amplifier can be designed with multi-gate transistor and also with various high-k dielectric materials.

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