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The narrowband tunable Radio Frequency (RF) power amplifier with High-Efficiency at 2.4 GHz Frequency

Idrees S. Al-Kofahi[1], Zaid Albataineh[2], Mamoun Tantawi [3] and Ahmad Dagamseh[3]
[1]Hijjawi Faculty for Engineering Technology, Al Yarmouk University, Jordan, ikofahi@yu.edu.jo
[2]Hijjawi Faculty for Engineering Technology, Al Yarmouk University, Jordan, zaid.bataineh@yu.edu.jo
[3] Hijjawi Faculty for Engineering Technology, Al Yarmouk University, Jordan.

ABSTRACT

This paper proposes a new high efficiency design that uses a source inductive degeneration with feedback for 2.4 GHz. Based on 0.18 µm CMOS technology, the proposed power amplifier (PA) uses Cascode and feedback. Cascode results in a high level of gain while the feedback improves the linearity and reliability of the design. The circuit benefits from added power efficiency at 32.5 % along with an output of 1 dB compression point (P_1dB) is 8.8 dBm via a 2.5 V voltage supply, noise figure (NF) equal 2 dB and gain is 12.74 dB.

Key words: Low Noise Amplifier, CMOS, Cascode, feedback, Compression Point, radio frequency (RF).

1. INTRODUCTION

The CMOS RF power amplifier has been experiencing notable growth over the past few years [1]. In terms of technological use, it has begun to meet the demands of the market for cheaper and smaller mobile communication devices [2]. This realization of RF power amplifiers abilities in the mainstream of CMOS technology has become essential in recent times [3]. CMOS PA is expected to be operated in a simple and effective manner that increases output power and offers improved efficiency of the PA [4]. The noise figure (NF) has showed an improvement in efficiency and power gain due to the decreased noise of the CMOS PA.

Tremendous research pertaining to the Internet of Thing (IoT) with a concentration on the internet of things (IoT) RF transceiver design. The power amplifier is acknowledged as the critical building block of the transceiver that has the highest power consumption. There is now a quest for a high efficiency PA in terms of powering portable devices [5 - 12]. There are two main groups of amplifiers that can be developed in this instance. Amplifier classes are mainly lumped into two basic groups. The first are the classically controlled conduction angle amplifiers forming the more common amplifier classes of A, B, AB and C, which are defined by the length of their conduction state over some portion of the output waveform, such that the output stage transistor operation lies somewhere between being “fully-ON” and “fully-OFF”.

The second set of amplifiers is the newer so-called “switching” amplifier classes of D, E, F, G, S, T etc., which use digital circuits and pulse width modulation (PWM) to constantly switch the signal between “fully-ON” and “fully-OFF” driving the output hard into the transistors saturation and cut-off regions. The first group is a Class A and Class - C type (switch) that comprises Class -D and Class – E. The second group is based on the Class F PA that is classified between the linear and switch amplifier. This first group is composed of conventional Class A, B, AB, and C operating modes representing the transistor’s current source [10]. The linearity of this type is acceptable but not efficient.

However, the linearity of Type PA is worse, although, type PA has a better efficiency in comparison with the first PA group. With the introduction of the Class – E power amplifier [11] by Sokal in 1975, the simplicity of the structure makes it a suitable choice for a high frequency transmitter [3-13]. Techniques such as mode locking was used to achieve high frequency PA [14] but the bandwidth was hampered by its limiting locking range of mode lock base power amplifier.

The conventional configuration of the CEPA RF choke uses a drain of switch transistor known as infinite DC feed or shunts capacitor structure. This cannot be used for integrated designs because of its low quality inductor and high power consumption [15]. Under a modified topology called the second order finite DC feed [16], the small inductor used manages to remove the choke without shunt capacitance [17-19, 23].

PA transistors are required to be large because they need to deliver ample power to the load. That is why the capacitance of gate drain is large and the gain seems to be decreased by these transistors.

The trans-conductance of transistor finds its power consumption decreased when using cross coupling topology [20]. This technique has been found to provide high gain and better reverse isolation [21]. PAs that work well in watt level are reported [22, 23]. While robust power against voltage stress was achieved [22], power dissipation was also high. To make PA work at high levels of efficiency, injection lock oscillators were used in conventional Class – E PA [23]. While this method has its limitations due to frequency bandwidth structures and efficiency, the method cannot deliver RF power for deep submicron PAs and thus, have posed a challenge to its developers [14]. [23-25] millimeter transistors were required in order to create proper current for

watt level output power. The existing constraints of the state of the art PAs [26,27], have allowed for the development of a fully differential Class – E PA comprised of some of these methods.

In [20-21], they used the cascode class – E amplifier as a driver amplifier. Both used an interstage LC matching circuit running through the driver and main amplifier, which performs the injection locking through gate to drain capacitance of the main amplifier. This in turn reduces the required input power. Based on [26], it is possible to use a cascode driver amplifier with double resonance circuit and negative capacitance cascode as a main amplifier to reduce voltage stress on CMOS transistors, thus enhancing efficiency. This can be used for the implementation of watt-level RF transmitters with a note that it cannot be used for low power transmitters because it requires high input power (≈+6.5 dBm). However, since both use a large number of inductors, these require a larger silicon area with additional parasitic capacitance (i.e. due to on-chip inductors and wider transistors in terms of 4000-μm and 7000-μm width used in the cascode main amplifier). It also requires an additional control circuitry because of unwanted oscillation that occurs when the RF input signal is not linked into the power amplifier. Therefore, this is not suitable for on-chip fully integrated RF transmitters.

In [22], they indicated that the capacitive feedback and pimatching cascode amplifier (CFPM-CA) may be used for narrow band Low Noise Amplifier (LNA) in order to boost power and reduce the silicon area. This removes the for source degeneration inductor (Ls) by providing full power and noise matching at the input level so it requires low input power (i.e. ≤0 dBm) This can be adopted for use as a driver amplifier for both proposals in this paper.

According to literature from [28] the common source amplifier suffers from voltage stress so it cannot deliver a low output power of about less than 6 dBm so it cannot be used for the PA implementation based on high output power i.e. ≥+15 dBm).

On the other hand, the cascode class – E amplifier that uses a DC block LC passive tuning circuit is used by [25] as a main circuit amplifier. This suffers from a higher silicone area requirement and large quality factor inductors (Q).

In [18] they use a common source amplifier with finite DC feed inductor and harmonic termination circuits. This is affected by voltage stress handling capabilities so it cannot be used either for on-chip integration or low power applications.

However, in [19], they used negative capacitance cascode class-E amplifiers with injection locking gate inductors. The result, high efficiency at low power when used as a main amplifier. However, it too suffers from the need for a larger silicon area.

Using a LC tank oscillator, the idea was to reach high frequency operation mode [14]. Specific work was dedicated to the development of the IOT frequency range which we used at 2.4 GHz for the proposed PA. Cross couple neutralization was used to improve the stability and PAE of the system. Using small size transistors for the differential structure plus complementary structure of our PA resulted in a low threshold value (THD).

For this study, the narrowband tunable radio frequency (RF) power amplifier was created using an amplifier circuitry configured to receive, generate and amplifies RF output signal. This provides a narrow band gain response set at a 2.4 GHz frequency.

This can be used to amplify weak input signals in wireless devices (WCDs) such as cordless telephones.

There are several communications systems that operate at several frequency bands. Third generation (3G) mobile communication systems use bands above 1GHz such as 1920-1980 MHz for wide band code division multiple accesses (WCDMA) [3].

A filter can be created out of a tunable narrow band to constrict the noise outside the preset frequency band. The response gained within the narrow band should be linear in representation of the desired frequency band.

In this paper, we propose that a modified negative capacitance cascode class-E amplifier. One or more amplifier stages that comprise the PA circuitry along with a tunable resonant design can be connected to an amplifier stage or stages. Each tunable resonant structure can use the tuning control signal to find a narrow band gain response for the amplifier circuit. Our main aims are to design power amplifier that consists of one stage amplifier and one tunable resonant circuit in 0.18 μm CMOS technology. Due to the low trans-conductance of CMOS technology, CMOS needs to have a cascode-stage circuit that will allow it to achieve a sufficiently high gain. For this design, the cascode process was used with the result of a high gain in terms of feedback stage linearity and reduced noise figure design. a parallel LC-tuning circuit is used at the output of the amplifier to obtain higher efficiency and higher output power. A suggestion that has already been proposed by [21] for use in a single stage common source amplifier. While this suffers from a voltage stress handling capability problem, the suggested cascode class-E power amplifiers do not exhibit this error.

The rest of this paper is organized as follows. A Power Amplifier circuit design is presented in section 2. In section 3, the simulation and experimental results are shown. Finally, in section 4, conclusions are given.

2. POWER AMPLIFIER DESIGN

Power amplification has a number of criteria to be consider. These including the balancing of parameters like maximum gain, high output power gain, power added efficiency, linearity, minimum noise figure, and power dissipation. As expected, these criteria often conflict with each other.

Figure 1 shows a schematic diagram of the proposed power amplifier. This design was created using feedback stage and cascode topology. At this stage, feedback linearity is responsible for control and high power output.

The power stage of the designed PA consists of M1and M2 in a cascode topology. The size of the power transistors is chosen to obtain the highest power. The channel width of

M_1 and M_2 are 136 µm and 73 µm, respectively. In order to ensure the unconditional stability of the circuit, the feedback composed of two transistors in cascode topology. A cascode topology is adopted in order to avoid excessive voltage on the CMOS devices, which are prone to oxide breakdown under high stresses [4, 5]. With a dc supply of 2.5 V and an output power of 9.9 dBm, the power consumption is 9 mW.

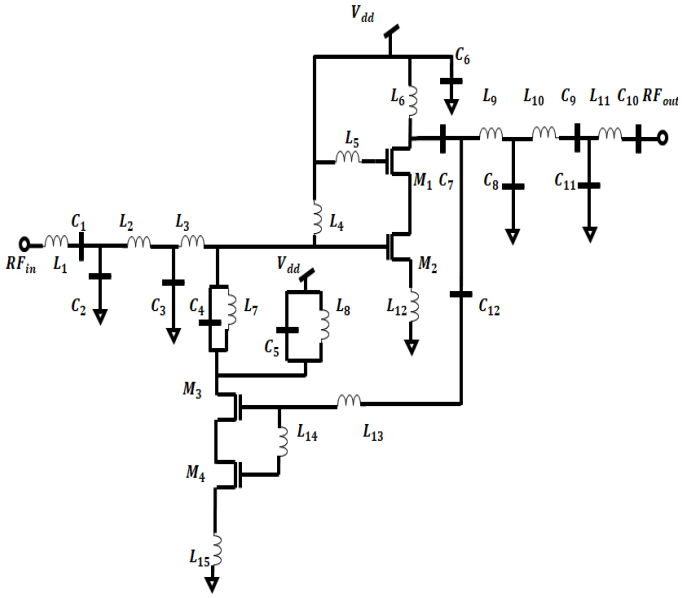

Figure 1: Schematic of the proposed PA

3. EXPERMENTAL RESULTS

The proposed design is simulated and optimized with Agilent Technologies' Advanced Design System (ADS) software.

Fig (2) shows the small-signal gain S21 of the PA. The maximum gain of 12.74 dB is achieved at 2.4 GHz . An excellent input matching at 2.4 GHz can be observed in Fig (3), indicated by S11 parameter close to -62 dB and an output matching close to -23 dB can be observed in the same figure.

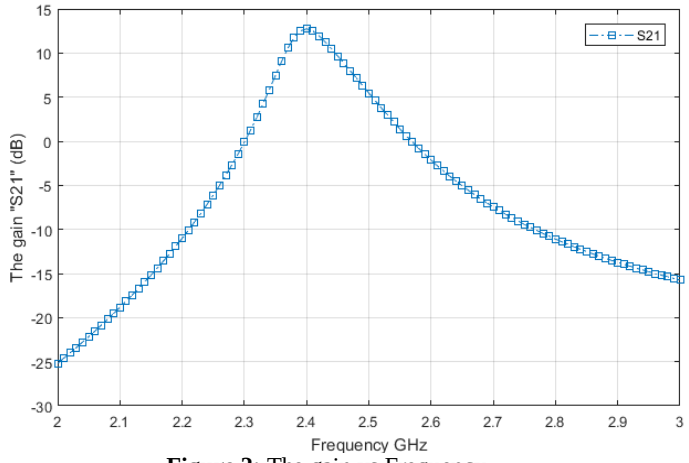

Figure 2: The gain vs Frequency

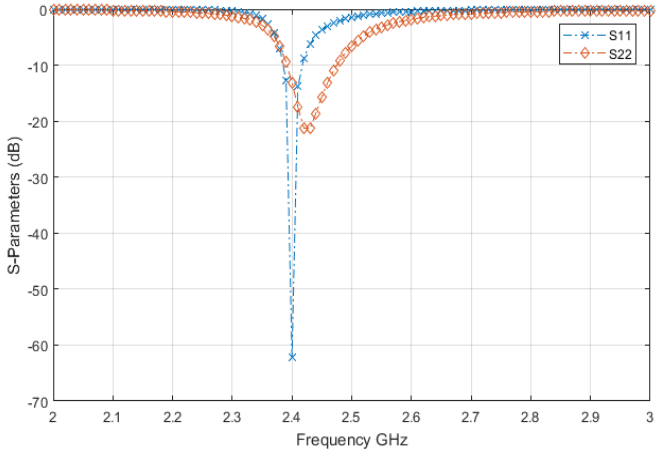

Figure 3: Input matching and Output matching

Fig (3) shows the i/p and o/p matching. It is clear that an excellent i/p match of -62 dB at 2.4 GHz is achieved, while an o/p matching of around -23 dB is obtained. The reverse isolation is shown in fig (4). It is clear that reverse isolation of -19dB at 2.4 GHz is obtained.

Whereas Fig (4) present good reverse isolation S12 of -19 dB at 2.4 GHz. Also, transient analysis is useful for drain voltage and current waveforms, as shown in Fig (5).

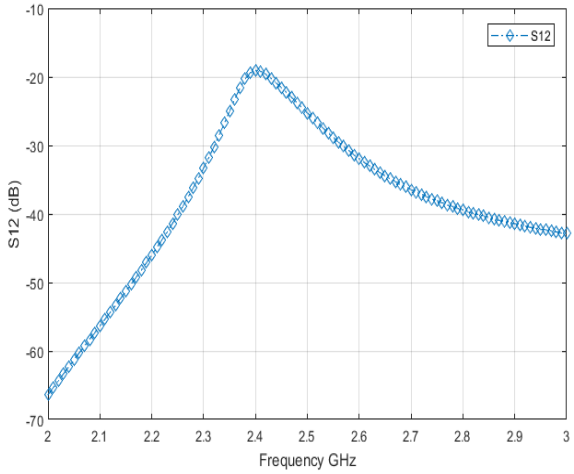

Figure 4: The reverse isolation

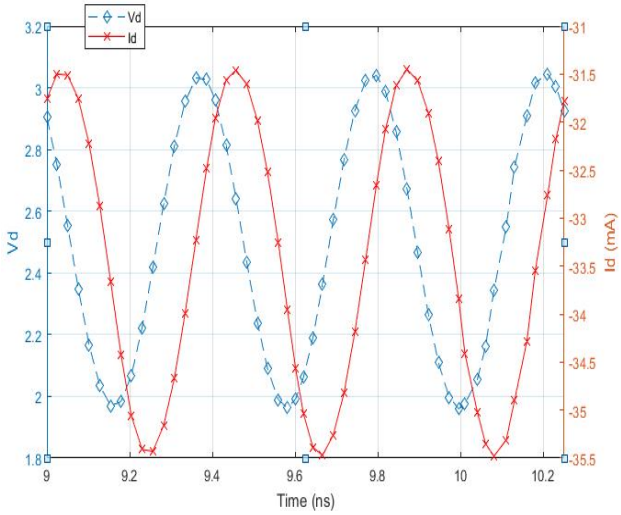

Figure 5: Transient voltage and current waveforms of the drain

Fig (6) presents good simulated stability μ-factor for the proposed PA. It can be observed that, due to the careful design of feedback stage. The simulated noise figure is shown in Fig (7).

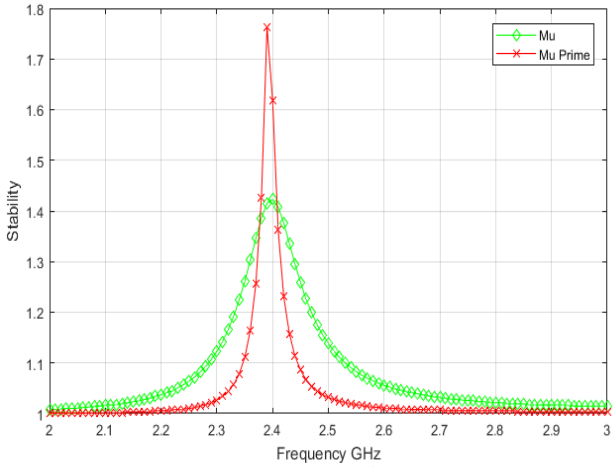

Figure 6: Stability factor (Mu)

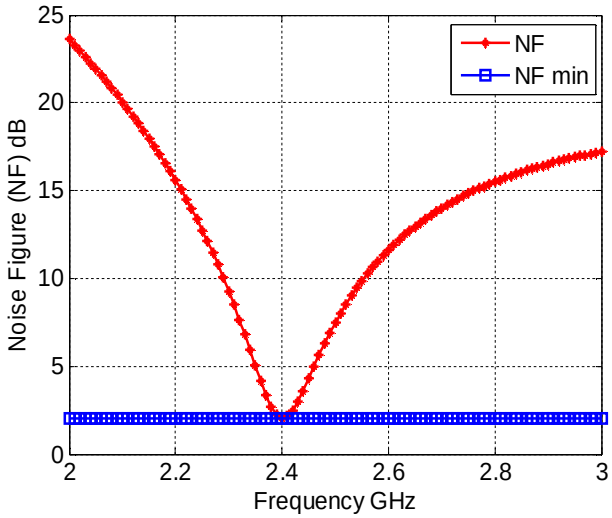

Figure 7: Noise Figure

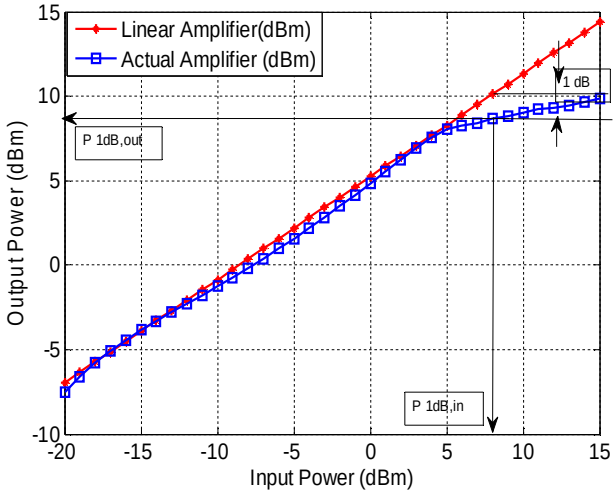

Figure 8: Pout vs Pin curves for linearity comparison (1 dB compression point)

The figure shows that at 2.4GHz minimum noise figure of 2 dB is obtained. While linear PA has a specific gain per frequency range and the input power increases, there is a point when the gain turn into losses and the quality begins to decrease. This is when the PA has a compression though there is no output increase or input increase. This flattened gain indicates high signal levels, resulting in a saturated amplifier. A non-linear response results along with signal distortion, harmonics, and intermodulation products. One must know when the point compression begins in order to prevent distortion at specific input levels. So, in this proposed PA the P_1dB is presented in Fig (8).

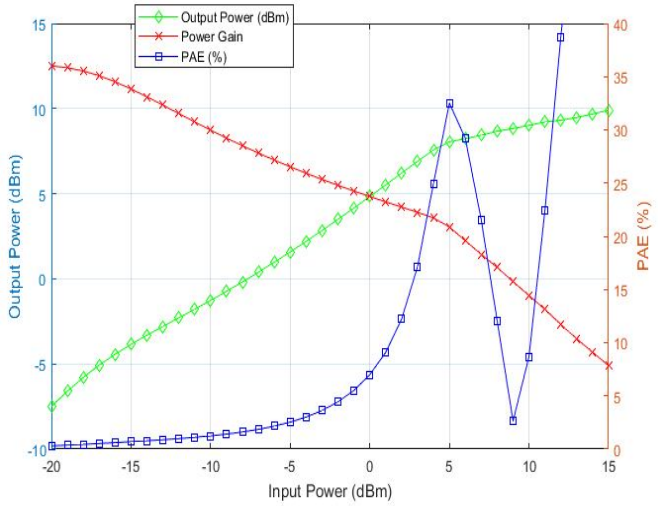

Figure 9: Output power vs Input power

The PA achieved good power amplifier efficiency (PAE) of 32.5% and an output power of 9.9 dBm in 50 Ω load, whereas the power gain is 12.5 dB as shown in Fig (9).

Table 1: Comparison Results

REF.	TECH. NODE (NM)	FREQUENCY (GHZ)	VDD (V)	GAIN (DB)	PAE %
[6]	180	2.4	3.3	15	6.3
[7]	130	2.5	1.8	27	38.3
[8]	180	2.4	3.3	NA	27
[9]	65	2.5	3	17	4.9
[10]	180	2.4	1.8	13	6.3
[11]	180	2.6	3.3	12	30.3
THIS WORK	180	2.4	2.5	12.7	32.5

*NA: not available

4. CONCLUSION

This paper summarized the simulation results of the PA activities using the advanced design system based on 0.18 μm topology. Small signal gains are obtained using S-parameter analysis. It is found that design gain of 12.74 dB at 2.4 GHz, reverse isolation of -19 dB and input and output matching of -62 dB and -13 dB respectively can be achieved. There is a PAE of 32.5% with a power gain of 12.5 dB using 2.5 V dc power supply with a consumption of 9 mW. Due to the

efficient linear clarity, an excellent starting point for future military and commercial amplification power was created using narrow band power matching networks.

REFERENCES

1. Thomas H. Lee, the design of CMOS Radio-Frequency Integrated Circuits, 2003.
2. M. Acar,Nauta, Bram ,Annema, Anne J.,"Power Amplifiers in CMOS Technology: A contribution to power amplifier theory and techniques",Published - 2 Feb 2011,978-90-365-3138-2
3. Ali M. Niknejad,Debopriyo Chowdhury,Jiashu Chen," IEEE Transactions on Microwave Theory and Techniques (Volume: 60, Issue: 6, June 2012)" https://doi.org/10.1109/TMTT.2012.2193898
4. Morgan, Patrick N. (Austin, TX, US) Dupuis, Timothy J. (West Lake Hills, TX, US) Bockelman, David E. (Dripping Springs, TX, US), "Narrow-band tunable radio frequency (RF) power amplifiers and related methods", United States Patent Application 20120009889
5. T. Sowlati and D. Leenaerts, “A 2.4GHz 0.18?m CMOS Self-Biased Cascode Power Amplifier with 23dBm Output Power,” IEEE Int. SolidState Circuits Conf. Sept., 2002.
6. V. Knopik, B. Martineau, and D. Belot, “20dBm CMOS Class AB Power Amplifier Design for Low Cost 2GHz-2.45GHz Consumer Applications in a 0.13?m Technology,” IEEE, pp. 2675–2678, 2005.
7. Yoon, Y., Kim, J., Kim, H., An, K. H., Lee, O., Lee, C. H., et al. (2012). A dual-mode CMOS RF power amplifier with integrated tunable matching network. IEEE Transactions on Microwave Theory and Techniques, 60(1), 77–88. https://doi.org/10.1109/TMTT.2011.2175235
8. Santos, E. L., Leite, B., & Mariano, A. (2015). Multimode 2.4 GHz CMOS power amplifier with gain control for efficiency enhancement at power backoff. In 2015 IEEE 6th Latin American Symposium on Circuits & Systems (LASCAS), 2015, pp. 1–4.
9. An, K. H., Lee, D. H., Lee, O., Kim, H., Han, J., Kim, W., et al. (2009). A 2.4 GHz fully integrated linear CMOS power amplifier with discrete power control. IEEE Microwave and Wireless Components Letters, 19(7), 479–481.
10. Tuffery, A., Deltimple, N., Kerherve ´, E., Knopik, V., & Cathelin, P. (2015). CMOS fully integrated reconfigurable power amplifier with efficiency enhancement for LTE applications. Electronics Letters, 51(2), 181–183.
11. Santos, F., Mariano, A., & Leite, B. (2016).2.4 GHz CMOS digitally programmable power amplifier for power back-off operation. In 2016 IEEE 7th Latin American Symposium on Circuits & Systems (LASCAS), 2016, pp. 159–162.
12. Mohsen Haghighat1 • Abdolreza Nabavi1. Fully integrated CMOS power amplifier with linearity and efficiency enhancement using 2nd harmonic injection technique. 1 June 2016/Revised: 21 July 2016/Accepted: 26 October 2016 Springer Science+Business Media New York 2016. RF Power Amplifiers, MARIAN K. KAZIMIERCZUK.
13. A. Taibi, M. Trabelsi, A. Slimane, A. A. Saadi and M. T. Belaroussi, "Efficient UWB low noise amplifier with high out of band interference cancellation," in IET Microwaves, Antennas & Propagation, vol. 11, no. 1, pp. 98-105, 8 1 2017. https://doi.org/10.1049/iet-map.2016.0187
14. L. Albasha et al., "An Ultra-Wideband Digitally Programmable Power Amplifier With Efficiency Enhancement for Cellular and Emerging Wireless Communication Standards," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 10, pp. 1579-1591, Oct. 2016.
15. M. Akbarpour, F. M. Ghannouchi and M. Helaoui, "Current-Biasing of Power-Amplifier Transistors and Its Application for Ultra-Wideband High Efficiency at Power Back-Off," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 4, pp. 1257-1271, April 2017.
16. M Mabrok,, et al., “Design of Wide-band Power Amplifier Based on Power Combiner Technique with Low Intermodulation Distortion”, International Journal of Electrical and Computer Engineering (IJECE), Vol. 8, No. 5, pp. 3504~3511, October 2018.
17. Bataineh, Z., & Salem, F. An Energy-Efficient and High Gain Low Noise Amplifier for Receiver Front-Ends. International Journal of Research in Wireless Systems, 2012.
18. Z Albataineh, Robust blind channel estimation algorithm for linear STBC systems using fourth order cumulant matrices, Telecommunication Systems, Volume 68, Issue 3, pp 573–582. July 2018. https://doi.org/10.1007/s11235-017-0410-4
19. Zaid Albataineh, Yazan Hamadeh, Jafar Moheidat, Ahmad Dagamseh, Idrees Al-Kofahi, Mohammed Alsumady, A High-Gain Low Noise Amplifier for RFID Front-Ends Reader, Jordan Journal of Electrical Engineering (JJEE), Volume 3, Pages 65-74, Number 1, 2017.
20. Z. Albataineh, J. Moheidat and Y. Hamada, "Design of high gain 2.4GHz CMOS LNA amplifier for wireless sensor network applications," 10th Jordanian International Electrical and Electronics Engineering Conference (JIEEEC), Amman, 2017, pp. 1-5.
21. Z Albataineh, Blind Decoding of Massive MIMO Uplink Systems Based on the Higher Order Cumulants, Wireless Personal Communications (2018).
22. A. Taibi, M. Trabelsi, A. Slimane, A. A. Saadi and M. T. Belaroussi, "Efficient UWB low noise amplifier with high out of band interference cancellation," in IET Microwaves, Antennas & Propagation, vol. 11, no. 1, pp. 98-105, 8 1 2017.
23. L. Albasha et al., "An Ultra-Wideband Digitally Programmable Power Amplifier With Efficiency Enhancement for Cellular and Emerging Wireless Communication Standards," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 10, pp. 1579-1591, Oct. 2016. https://doi.org/10.1109/TCSI.2016.2586599

24. Bataineh, Z., Jehad I Ababneh and Salem, F. Linear Phase FIR Low Pass Filter Design Using Hybrid-Differential Evolution. International Journal of Research in Wireless Systems, 2012.
25. Bataineh, Z. and Salem, F. New blind multiuser detection in DS-CDMA using H-DE and ICA. 4th International Conference on Intelligent Systems, Modelling and Simulation, 2013.
26. Bataineh, Z. and Salem, F. New blind multiuser detection in DS-CDMA based on extension of efficient fast independent component analysis (EF-ICA). 4th International Conference on Intelligent Systems, Modelling and Simulation, 2013.
27. T.V.RamaKrishna, G.V.Ganesh, B.S.D.Saikumar, K.Chandana, D.Lokesh and N.Siddaiah. Electromechanical and RF performance analysis of MEMS shunt configuration switch. 4th rishna et al., International Journal of Emerging Trends in Engineering Research, 7(11), November 2, Volume 7, No. 11 November 2019. https://doi.org/10.30534/ijeter/2019/267112019
28. N.Siddaiah,V.V.Praveen,P.KavyaSri,Y.GaneshBabu and G.Venkata Ganesh. A Low Power Cantilever-Based Metal Oxide Semiconductor Gas Sensor for Green House Applications. 4th rishna et al., International Journal of Emerging Trends in Engineering Research, 7(11), November 2, Volume 7, No. 11 November 2019. https://doi.org/10.30534/ijeter/2019/307112019
29. A.Bendali, S. Bri , M. Habibi , M.N. Srifi and A. El fellahin. Study and Design a Novel Adaptive Array Antenna for a RFID Applications. 4th rishna et al., International Journal of Emerging Trends in Engineering Research, 7(11), Volume 7, No. 12 December 2019.