

Design and Simulation of Seven Level Cascaded H Bridge Inverter for Medium Power Applications

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ABSTRACT

In the recent years, multilevel inverters (MLI) are highly being used for medium power and high-power applications because of several merits such as low voltage stress on the power switches, low electromagnetic interferences, low dv/dt ratio to supply lower harmonic contents in the output voltage and current. Multilevel inverters have become more popular in electric high-power application with the promise of very low disturbances and the possibility to function at lower switching frequencies than ordinary two-level inverters. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. So that there is no need for all switches to work in high frequency it leads to simpler and more reliable control of the inverter. The seven-level inverter with reduced number of switches with PWM (Pulse Width Modulation) switching is simulated. It is observed that the pulse generation using PWM switching leads to further reduction of THD. Simulations of the proposed system have been carried out in MATLAB/SIMULINK environment to show its effectiveness of Seven Level Inverter Topology for power quality issues.

Key words: Cascaded H bridge inverter, sinusoidal Pulse width modulation, IRP controller, THD.

1.INTRODUCTION

Power electronic device that converts dc power into ac power at desired output voltage and frequency is known as inverter.

The inverter producing an output voltage or current with two different levels of +V and -V is known as 2 level inverters. This two-level conventional inverter operates at high switching frequency, with high change losses and rating constraints for high power and voltage applications. It also faces harmonic distortion, EMI and high stress. High level of total harmonic distortion is another problem. Because of these problems, it is difficult to interface power electronic switches directly to high and medium voltage grid.

Here comes the need for a different topology of multi-level inverter. The multilevel inverter topology concept has been introduced in the year 1975 with three level converters. It is possible to increase the power rating with number of voltage levels in the inverter. This decreases the device rating in the inverter. A multilevel inverter generates a smooth sinusoidal waveform from several d c voltage levels as its input.

Multi-level inverters have taken part in industrial applications for high power and voltage ranges. It can be easily communicated with renewable energy sources for various high-power applications. The input side dc voltage sources are obtained from batteries, capacitor, renewable energy system, etc.

2. CONCEPT OF MULTILEVEL INVERTER

In Conventional two-level inverters normally generate an output AC voltage from an input DC voltage. Pulse Width Modulation switching scheme is used to generated the AC output voltage (as shown in fig).

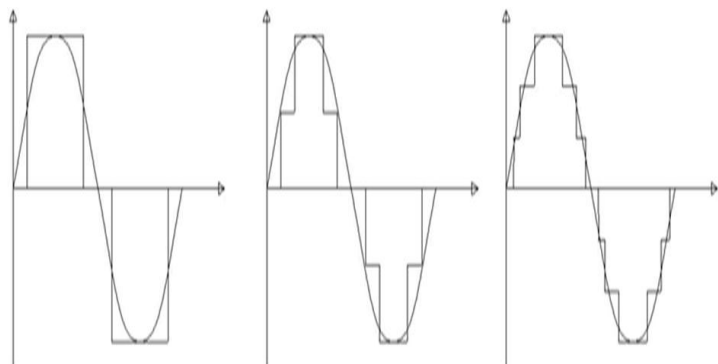


Figure 1: Shows 3 level, 5 level, 7 level inverter waveforms

Figure 1 output AC voltage waveform of Multilevel inverters.

In the concept of Multilevel Inverter topology (MLI), several DC voltage levels are added together to create a smoother output waveform (as shown in figure 3). The obtained output waveform has lower dv/dt and harmonic distortions. The circuit design is more complex with the increase in voltage levels. It needs a complicated switching controller circuit also.

As in figure 1, Conventional two-level inverters normally generate an output AC voltage from an input DC voltage. Pulse Width Modulation switching scheme is used to generate the AC output voltage (as shown in figure 2). In the concept of Multilevel Inverter topology (MLI), several DC voltage levels are added together to create a smoother output waveform (as shown in figure 3). The obtained output waveform has lower dv/dt and harmonic distortions. The circuit design is more complex with the increase in voltage levels. It needs a complicated switching controller circuit also.

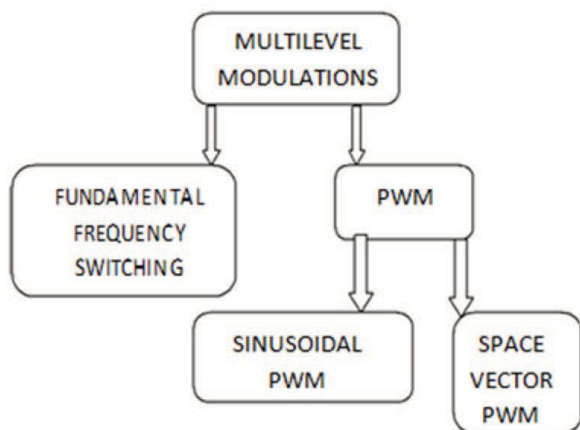


Figure 2: Shows Modulation Techniques of Multi Level Inverter

3. CASCADED VOLTAGE H BRIDGE MULTILEVEL INVERTER TOPOLOGY

The cascaded H-bridge inverter uses separate DC sources or capacitors (as shown in figure 8). It requires only less number of components in each level. There is a series connection of power conversion cells. The H-bridge consists of capacitors

and switches pair combination. For each H-Bridge, separate input DC voltage is obtained. It generates a sinusoidal output voltage. The inverter uses series connected H-bridge cells, each providing three different levels of DC voltages (zero, positive DC and negative DC voltages). The output voltage is the sum of all the generated voltages from each H Bridge cell. If m cells are present, the numbers of output voltage levels will be $(2m+1)$.

4. SEVEN LEVEL CASCADED VOLTAGE H BRIDGE MULTILEVEL INVERTER

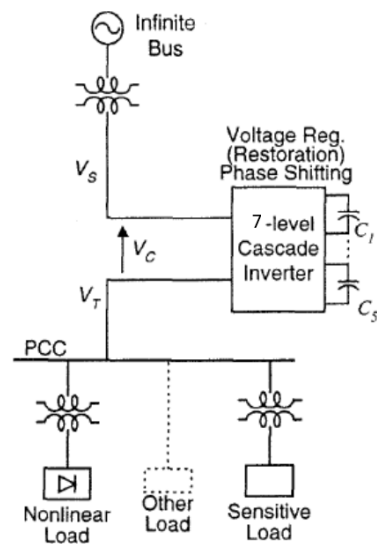


Figure 3 : Shows System configuration for voltage regulation (restoration), phase shifting, and harmonic isolation.

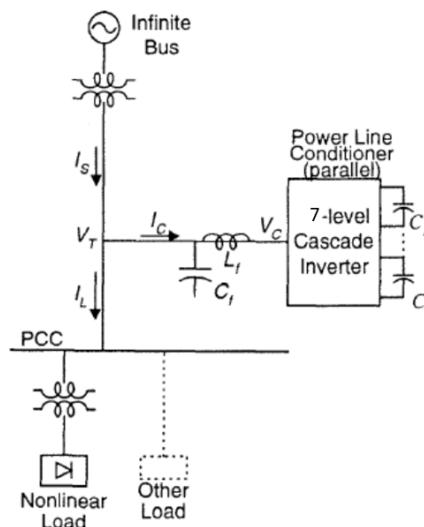


Figure 4 : Shows System configuration for var and harmonic compensation

A DC - DC converter takes the voltage from a DC source and converts the voltage of supply into another DC voltage level. They are used to increase or decrease the voltage level. This is commonly used in automobiles, portable chargers and

portable DVD players. Some devices need a certain amount of voltage to run the device. Too much of power can destroy the device or less power may not be able to run the device. The converter takes the power from the battery and cuts down the voltage level, similarly a converter step-up the voltage level. For example, it might be necessary to step down the power of a large battery of 24V to 12V to run a radio.

A multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input. The term multilevel starts with the three-level inverter introduced in 1981.

Multilevel inverters have an arrangement of power switching devices, capacitor, voltage sources. Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low Electro Magnetic Interference (EMI).

Now-a-days, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The most attractive features of a multilevel inverter are, they can generate output voltages with lower dv/dt, draw input current with very low distortion, generate smaller common-mode (CM) voltage and they can operate with a lower switching frequency. Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with limited maximum device rating.

As a result of high technology development, the demand and the quality of electric power is higher than before. Because of the advancement of semiconductor, the specification of power device and power conversion technique is promoted. One of the power converters which can transform DC to AC is called inverter. Inverter is the intermedium which transmit power to other electrical equipment such as uninterruptible power supply, servo motor, air-conditioning system, and smart grid compose of renewable energy shown in Fig. 1. To satisfy different demands and characteristic of loads, the output frequency and voltage have to change with different loads;

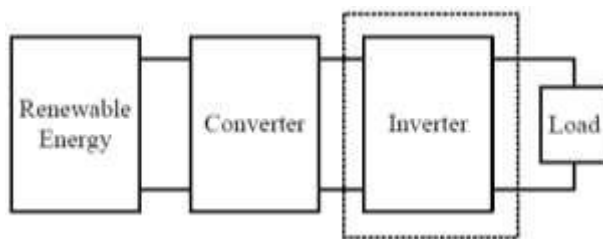


Figure 5: Shows Block diagram of renewable system

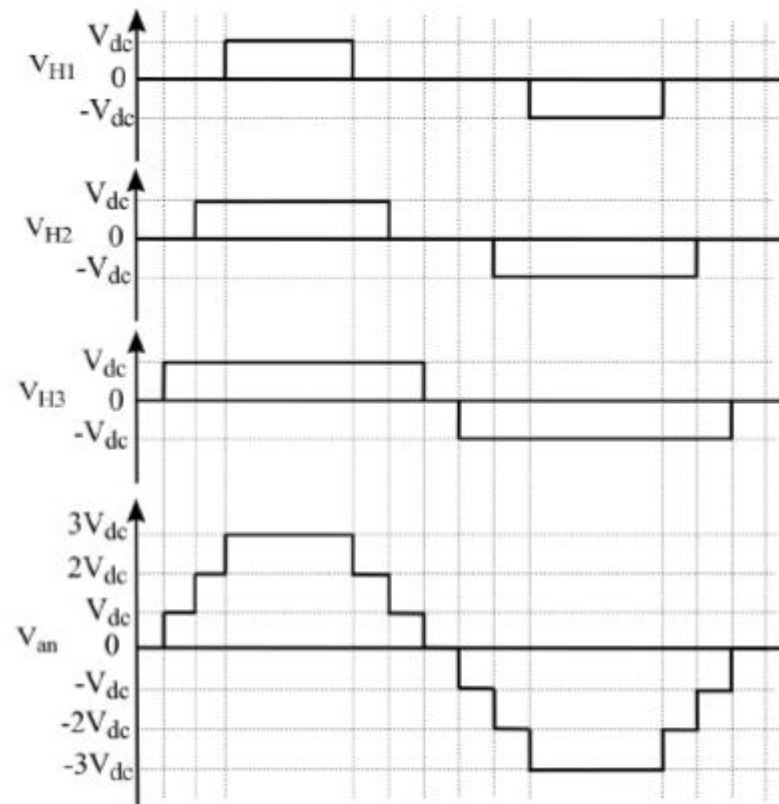


Figure 6: Shows output waveforms of seven level inverter

5.IRP THEORY

IRP theory was initially proposed by Akagi et al. IRP theory is based on the time domain. It is valid both for steady-state and transient operation. The basic block diagram of IRP theory.

Where I_{Comp} is the compensation current, I_{Source} is the source current and I_{Load} is the load current. The instantaneous power theory implements a transformation from a stationary reference system in a-b-c coordinates, to a system with coordinates α - β -0 by making use of an algebraic transformation, known as Clarke transformation.

$$\begin{bmatrix} V_0 \\ V_\alpha \\ V_\beta \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} P_0 \\ P \\ q \end{bmatrix} = \begin{bmatrix} V_0 & 0 & 0 \\ 0 & V_\alpha & V_\beta \\ 0 & -V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \quad (3)$$

Eq. (2) is valid for current transformation also. For phase three wire system $i_0=0$, so zero sequence power $P_0=0$ and consequently power equation would be

$$\begin{bmatrix} P \\ q \end{bmatrix} = \begin{bmatrix} V_{\alpha} & V_{\beta} \\ -V_{\beta} & V_{\alpha} \end{bmatrix} \begin{bmatrix} i_{l\alpha} \\ i_{l\beta} \end{bmatrix} \quad (4)$$

Using (4) the instantaneous active and reactive load powers could be obtained by following

$$\begin{bmatrix} P_l \\ q_l \end{bmatrix} = \begin{bmatrix} V_{\alpha} & V_{\beta} \\ -V_{\beta} & V_{\alpha} \end{bmatrix} \begin{bmatrix} i_{l\alpha} \\ i_{l\beta} \end{bmatrix} \quad (5)$$

Which could be decomposed into oscillatory and average component. Under balanced and sinusoidal mains voltage conditions the average power components are related to the first harmonic current of positive sequence and the oscillatory components represent all higher order current harmonics including the first harmonic current of negative sequence. Thus, the DSTATCOM should compensate the oscillatory power components so that the average power components remain in the mains.

$$\begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} = \frac{1}{v_{\alpha}^2 + v_{\beta}^2} \begin{bmatrix} V_{\alpha} & -V_{\beta} \\ V_{\beta} & V_{\alpha} \end{bmatrix} \begin{bmatrix} \bar{p} \\ 0 \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i_{sa} \\ i_{sb} \\ i_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{s\alpha} \\ i_{s\beta} \end{bmatrix} \quad (7)$$

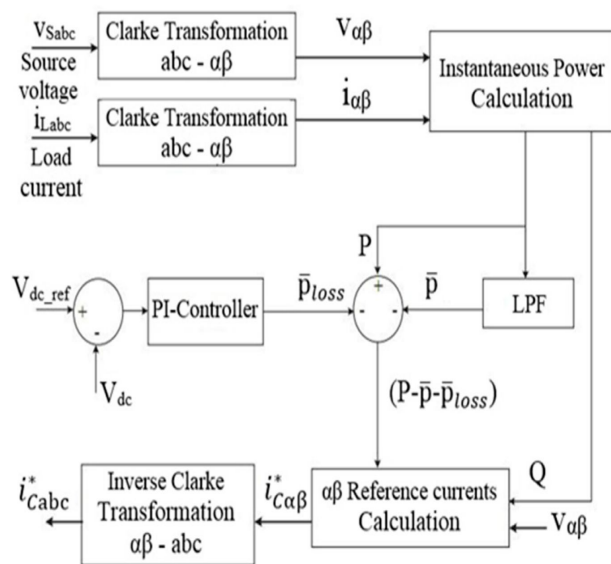


Figure 7: Shows IRP controller

6.SINUSOIDAL PWM

In a simple source voltage inverter, the switches can be turned ON and OFF as needed. During each cycle, the switch is turned on or off once. This results in a square waveform. However, if the switch is turned on for a number of times, a harmonic profile that is improved waveform is obtained. The sinusoidal PWM waveform is obtained by comparing the desired modulated waveform with a triangular waveform of high frequency. Regardless of whether the voltage of the signal is smaller or larger than that of the carrier waveform,

the resulting output voltage of the DC bus is either negative or positive. The sinusoidal amplitude is given as A_m and that of the carrier triangle is given as A_c . For sinusoidal PWM, the modulating index m is given by A_m/A_c .

7.SIMULINK BLOCK DIAGRAM

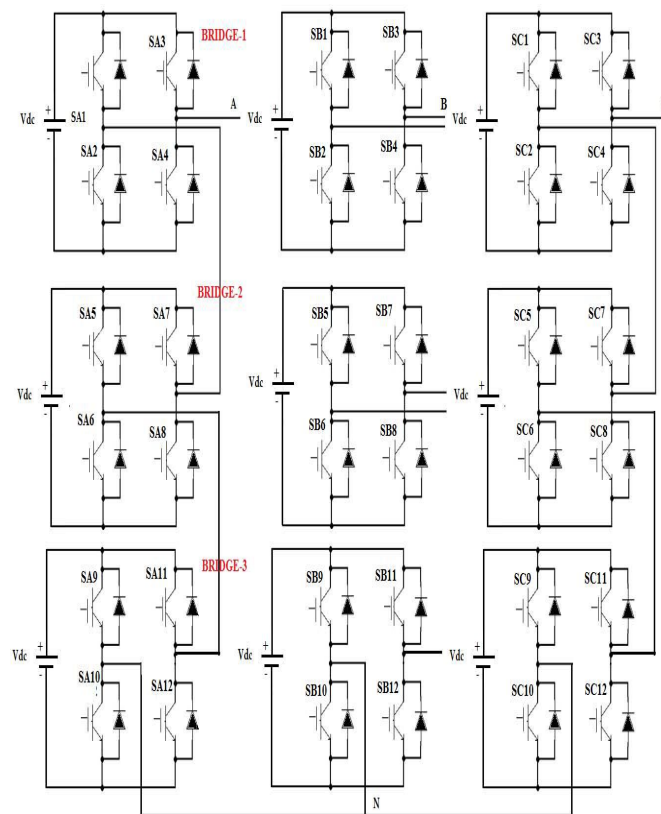


Figure 8: Shows simulink block diagram

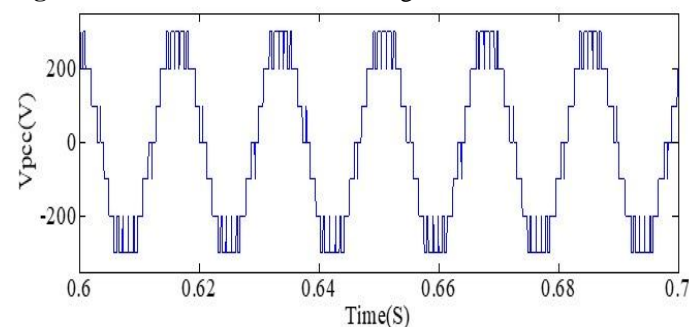


Figure 9 :Shows Output voltage waveform of seven level inverter

8.MATLAB RESULTS

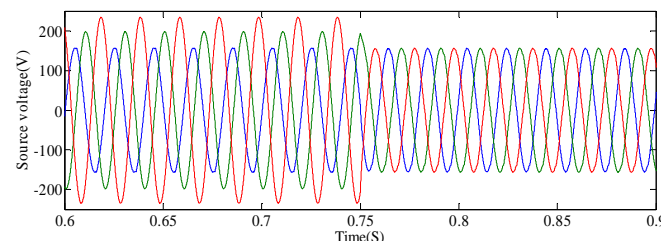


Figure 10: Shows waveform of source voltage

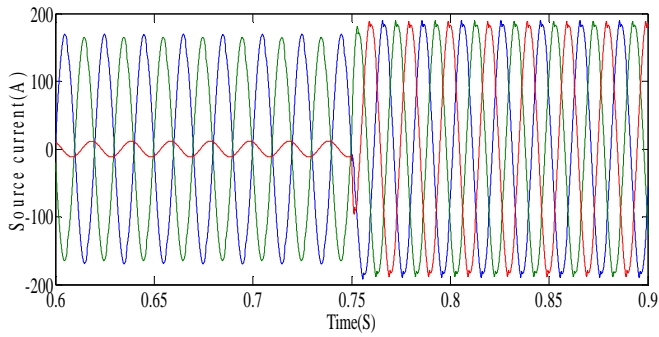


Figure 11: Shows waveform of source current

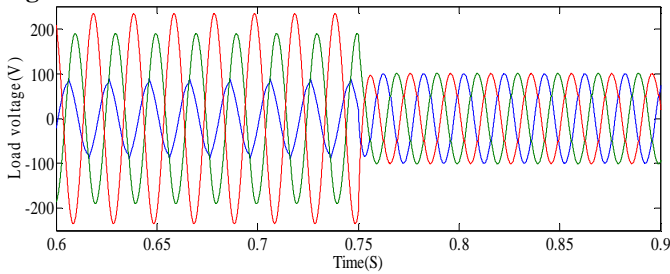


Figure 12: Shows waveform of Load voltage

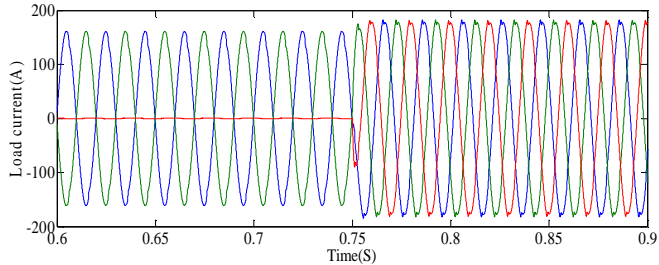
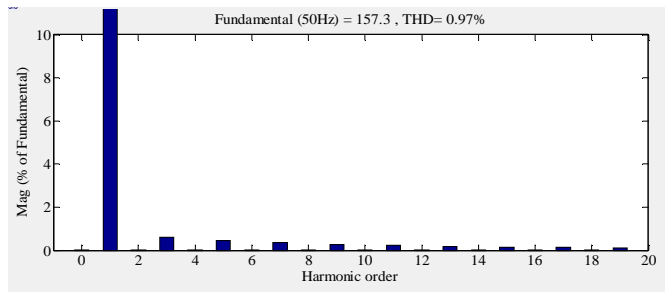
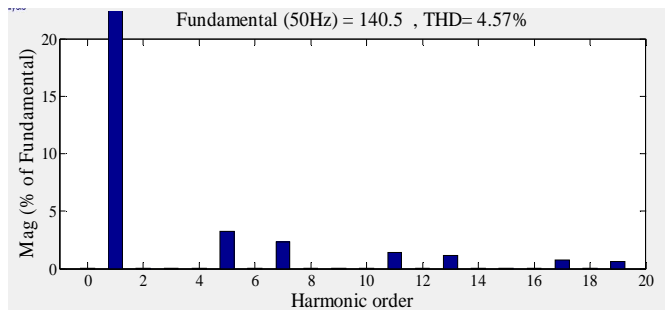


Figure 13: Shows waveform of load current

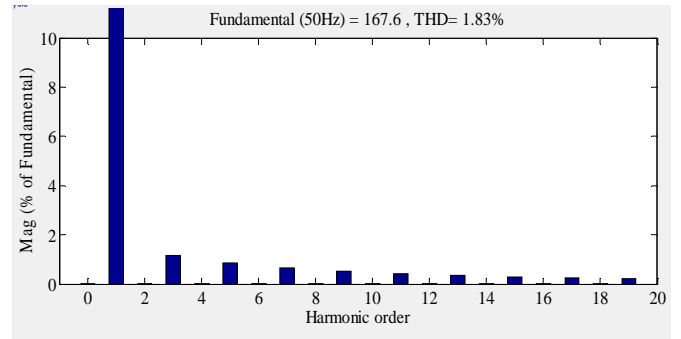
Figure 14: Shows FFT Analysis for under balanced condition:



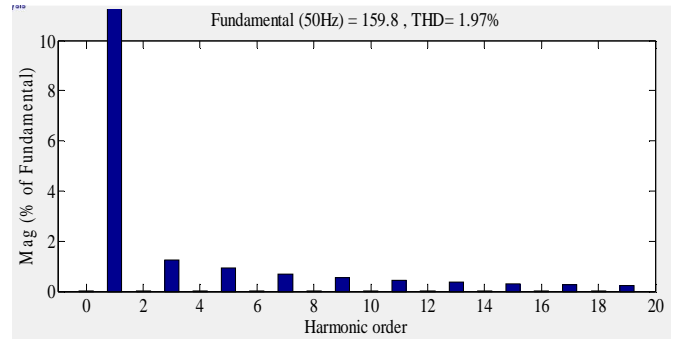
(i) THD of source voltage



(ii)THD of load voltage

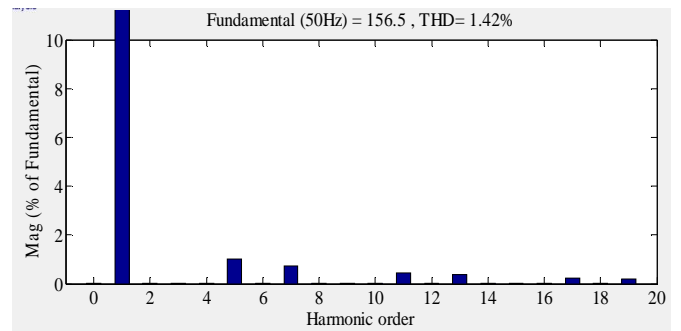


(iii) THD of source current

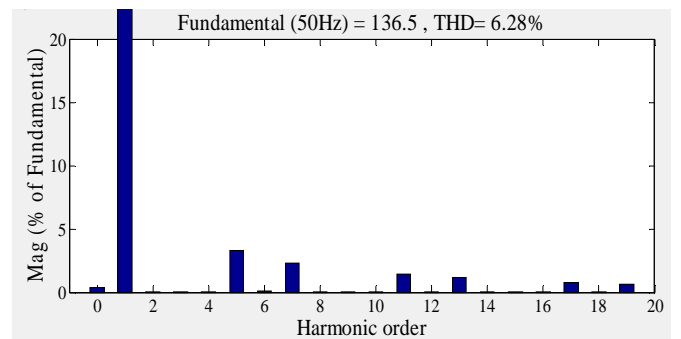


(iv)THD of load current

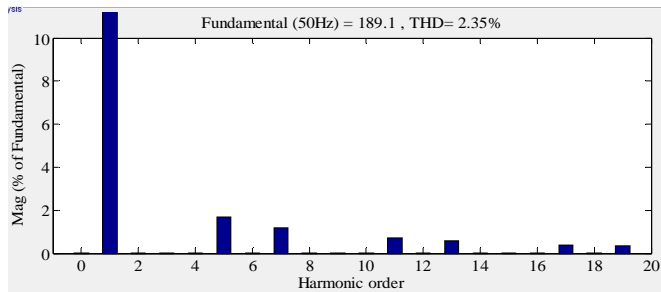
Figure 15: Shows FFT Analysis under un-balanced condition



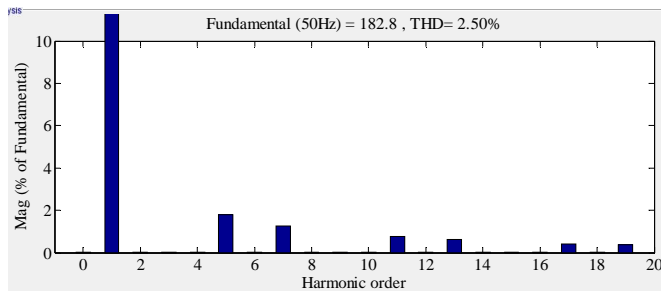
(v)THD of source voltage



(vi)THD of load voltage



(vii) THD of source current



(viii) THD of load current

9. CONCLUSION

From the above all discussions, it is concluded that in cascaded multilevel it is possible to eliminate considerable amount of harmonics and reduction of THD is also done by adding harmonic filter of proper frequency THD can be reduced at further more amount at least in software based simulation. There by ensuring the minimum switching losses, reducing size and installation cost. The new topology is well suited for drives and renewable energy applications. By this 7level cascaded H bridge inverter the total harmonic distortion is reduced and the performance of the system increased compare to the normal conventional inverters.

10. RESULT TABLE

Tables 1: Shows THD parameters of the system

Cases	With7-level inverter (Balanced)	With7-level inverter (unbalanced)
Source Voltage (Mag, %THD)	157.3, 0.97	156.5, 1.42
Load Voltage (Mag, %THD)	140.5, 4.57	136.5, 6.28
Source Current (Mag, %THD)	167.6, 1.83	189.1, 2.35
Load Current (Mag, %THD)	159.8, 1.97	182.8, 2.5

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