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# An Improved Bandwidth, Resistance Compensated Cascode Current Mirror

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## ABSTRACT

With increase in popularity of efficient low-power compact hardware and medical devices with better efficiency and battery backup has increased the need to utilize reliable methods for designing analog and mixed-signal circuits. The desired circuit performance with least power consumption can be achieved by relative scaling of device geometry and its parameters [1-5]. The conventional gate-driven technique is not much effective in this respect so the research has been done on the usage of non-conventional techniques. An alternate to conventional techniques can be a bulk-driven technique. Here, the input is connected at the bulk terminal of the MOSFET instead of biasing it with either the source terminal or the supply voltages thus removing the threshold voltage. The self-biased technique is used to attain high output impedance and high voltage swing with low power consumption [6-7]. The super-cascode technique is utilized at the output to improve the swing of waveform. Bandwidth of circuit is also enhanced using the compensating resistance technique. The simulations of the proposed current mirror are carried out at 180 nm CMOS technology [8-10].

**Key words:** Current mirror, Self-biased, Gate-driven, Bulk-driven.

## 1. INTRODUCTION

A Current mirror (CM) is a circuit that generates the replica of current at input end onto the output end irrespective of the loading conditions [11]. CMs are the basic component of various analog and mixed-signal design such as level shifters, amplifiers, filters, etc. It also finds applications in biomedical engineering for designing various equipment [12-15]. An efficiently designed CM can improve the overall performance of such systems. Theoretically, the cascade configuration of transistors boots the accuracy of a CM and increase the output resistance though with an increase in supply voltage requirement there is a reduction in the input/output compliance range thus making it incompatible with current technology trend. The current mirror proposed here utilizes the bulk-driven concept to boost the performance of low voltage analog circuit without any modification in existing MOS structure also it utilizes the wide-swing characteristic of the self-biased technique [16]. It also makes use of compensating resistance technique to enhance the bandwidth of the circuit and the super-cascode technique is applied at the output end to obtain higher output impedance.

## 2. BASIC CURRENT MIRROR

The core of any CM is the basic CM shown in Figure 1. It is composed of two n-MOS transistors namely M1 and M2, a reference current source $I_{Ref}$ connected to the drain of transistor M1. The transistor M1 is in the diode configuration with its gate connected to the drain. The gate of transistors M1 and M2 are coupled together while the output is taken at the drain of transistor M2. As the transistor M1 is in diode configuration it always functions in saturation mode and since the gate-source potential of both the transistors is equal, M2 also operates in saturation. Therefore, the drain current $I_D$ of the transistors [while overlooking the Channel Length Modulation (CLM) effect] is given as:

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_t\right)^2 \quad (1)$$

Thus, reference current $I_{Ref}$ can be written as:

$$I_{Ref} = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left(V_{GS1} - V_t\right)^2 \quad (2)$$

and, the output current

$$I_{Out} = \mu_n C_{ox}\left(\frac{W}{L}\right)_2\left(V_{GS2} - V_t\right)^2 \quad (3)$$

where, $\mu_n$ is the carrier mobility, $C_{ox}$ is the oxide capacitance, $\frac{W}{L}$ is the transistor's aspect ratio, $V_{GS}$ is the gate-to-source potential and $V_t$ is the threshold voltage of the transistor. Since $V_{GS1} = V_{GS2} = V_{GS}$. On equating equation (2) and (3), we get

$$\frac{I_{Out}}{I_{Ref}} = \frac{(W/L)_2}{(W/L)_1} \tag{4}$$

From equation (4), it can be concluded that the replica of current at input end can be generated at the output end when the aspect ratio of both the MOSFETs M1 and M2 are equal i.e. when transistors M1 and M2 are matched. Miller Effect comes into shape for the above expression when CLM is considered. To overcome this effect cascade current mirror was introduced.

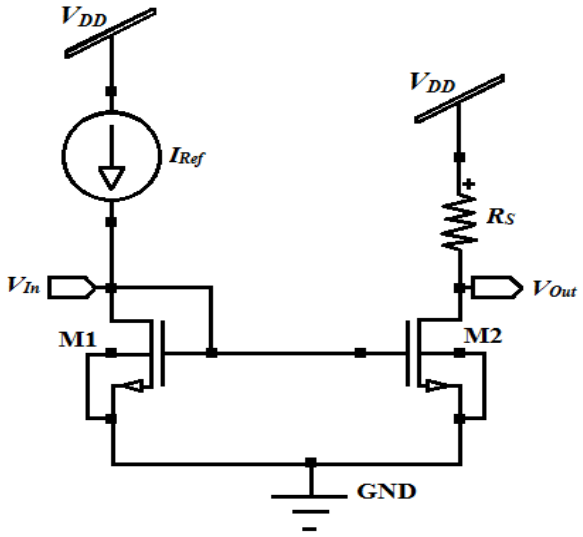


**Figure 1:** Basic Current Mirror

## 3. CASCODE CURRENT MIRROR

A pair of transistors connected in common gate configuration one over the other, to provide current buffering for the output of a common source amplifying transistor is referred as cascading. It increases the output impedance of a current source and serves as a high-gain amplifier. Due to high current transfer error and low output resistance CM performance is inadequate for high-performance applications, which can be improved by reducing CLM effect using cascode technique [17].

CCM (Cascode Current Mirror) technique is utilized to attain superior current matching characteristics at both output and input node and to improve the circuit gain, but with a shortcoming of reduced voltage swing. The basic CCM circuit is illustrated in Figure 2. It can be understood as two basic current mirror stages cacoded one over the other (M1, M2, M3 and M4), one reference current source $I_{Ref}$ and an output $I_{Out}$. Transistors M1 and M3 are in the diode configuration. The transistors M1 and M3 are gate coupled with transistor M2 and M4 respectively [18-19].

In basic CM circuit analysis, we have neglected the CLM effect but practically, a significant error is introduced during current copying due to the CLM effect, especially if narrow channel transistors are used. Considering CLM effect for basic current mirror, we can write

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_t)^2 (1 + \lambda V_{DS1}) \tag{5}$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_t)^2 (1 + \lambda V_{DS2}) \tag{6}$$

where, $\lambda$ = channel length modulation parameter.
and hence,

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2 (1 + \lambda V_{DS2})}{(W/L)_1 (1 + \lambda V_{DS1})} \tag{7}$$

Drain-source voltage of M1 is equal to its gate-source voltage since the MOSFET M1 is diode connected and as M1 and M2 are gate coupled the gate-source voltage of both the transistors is equal i.e. $V_{DS1} = V_{GS1} = V_{GS2}$ while $V_{DS2}$ may or may not be equal to $V_{GS2}$ since the circuitry is fed by transistor M2.

In order to overpower the CLM effect, a cascode current source is used because cascode devices are capable to shield the transistor variations from lower stages i.e.

$$\frac{I_{D2}}{I_{D3}} = \frac{I_{D1}}{I_{D4}} \tag{8}$$

or,

$$\frac{(W/L)_2 (1 + \lambda V_{DS2})}{(W/L)_3 (1 + \lambda V_{DS3})} = \frac{(W/L)_1 (1 + \lambda V_{DS1})}{(W/L)_4 (1 + \lambda V_{DS4})} \tag{9}$$

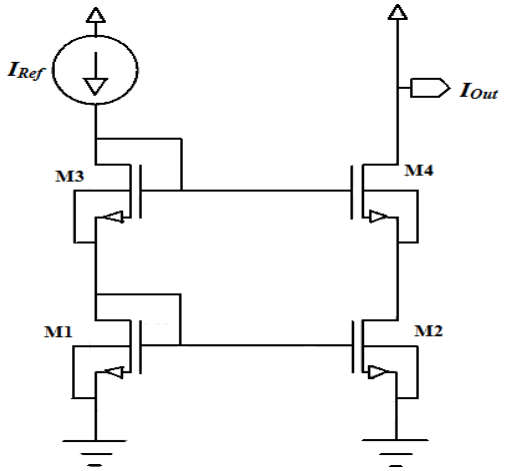


**Figure 2:** Cascode Current Mirror

If, CLM effect is neglected $\frac{(W/L)_2}{(W/L)_3} = \frac{(W/L)_1}{(W/L)_4}$, then $V_{GS2} = V_{GS3}$ and $V_{DS1} = V_{DS4}$. The main advantage of using cascade current mirror is it shoots up the required supply voltage while the input and output compliances decrease.

## 4. SELF-BIASED HIGH SWING CASCODE CURRENT MIRROR

After exploring a lot of literatures on CM it was concluded that the CMs operating in saturation mode has higher trans-conductance compared to those operating in linear or sub-threshold mode leading to higher bandwidth and enhanced input and output impedances. Figure 3 shows the self-biased cascode current mirror (SBCCM) [20]. As compared to cascode CM this technique shows an improvement by a factor of $V_T$ leading to the low supply voltage. It also provides the benefit of reduced power consumption and enhanced output resistance and high voltage swing. The input impedances of SBCCM is given as:

$$r_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{g_{m3}} + R \qquad (10)$$

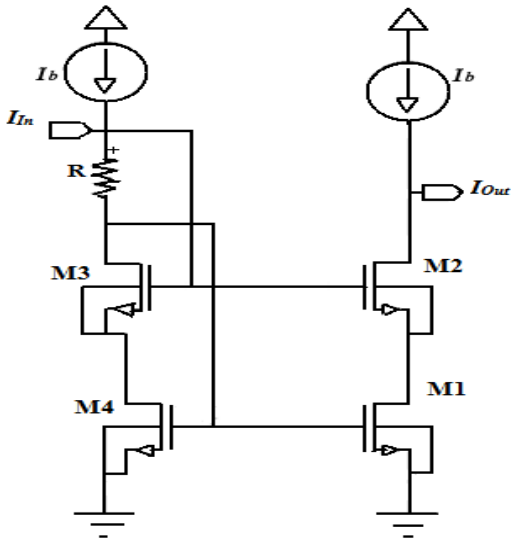


**Figure 3:** Self-Biased Cascade Current Mirror

and output impedances of SBCCM is given as:

$$r_{out} \approx r_{01} r_{02} (g_{m2} + g_{mb2}) \qquad (11)$$

for $g_m r_0 >> 1$ & $r_0 > R$

while the bandwidth is given as

$$\omega_0 = \sqrt{\frac{g_{m2} g_{m3}}{C_{gs2}(C_{gs1} + C_{gs3})}} \qquad (12)$$

## 5. BULK-DRIVEN CURRENT MIRROR

The bulk-driven SBCCM is illustrated in Figure 4 [21], as is evident, the input signal is applied at the bulk-drain connection of the transistor whereas the gate terminals are biased by a constant voltage $V_{DD}$, thus enabling the channel formation. At the input and output terminal of the device, a lower voltage drop is required as the threshold voltage ($V_T$) requirement is removed from the signal path, enabling the circuit to function at lower supply voltages as compared to its gate-driven complements. The reliance of the MOSFET current on bulk-drain voltage is validated by the fixed potential given at the gate terminal. It is given by equation

$$I_D(\text{sat}) = \frac{\beta}{2}\left(V_{GS} - V_{T0} - \gamma\sqrt{2\varphi_f - V_{BS}} + \gamma\sqrt{2\varphi_f}\right)^2, \qquad (13)$$
$$V_{DS} > V_{GS} - V_T$$

where, $\beta = \mu_n C_{ox} W/L$, $\mu_n$ is the carriers' mobility, $C_{ox}$ is the capacitance at the gate-oxide interface (per unit area), $\frac{W}{L}$ is MOSFET's aspect ratio, $\varphi_f$ is absolute fermi-potential, $V_T$ is the threshold voltage of MOSFET at zero bias and $\gamma$ is the body- effect coefficient of MOSFET.

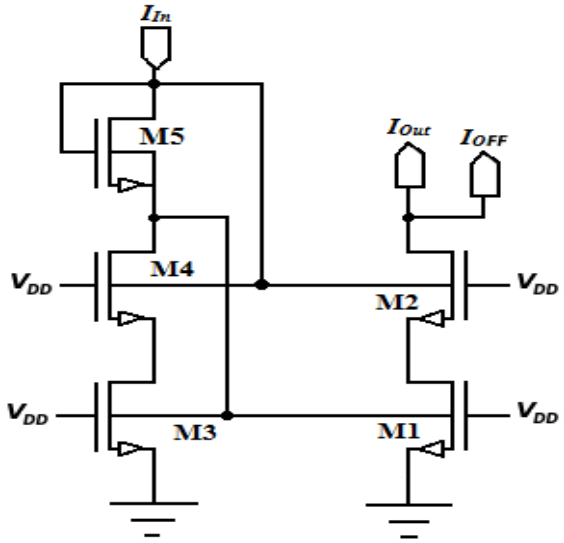


**Figure 4:** Self-Biased Bulk-Driven Cascode Current Mirror.

The current through MOSFETs can be determined by Eq. (13), for variation in potential VBS.

For bulk-driven SBCCM, the input resistance is given as:

$$r_{In} = \frac{v_{in}}{i_{in}} \approx R + \frac{1}{g_{mb3}} \quad (14)$$

For bulk-driven SBCCM the output resistance is given as:

$$r_{out} \approx r_{01} r_{02} \left( g_{m2} + g_{mb2} \right) \quad (15)$$

And the bandwidth is obtained as

$$\omega_0 = \sqrt{\frac{g_{m2} g_{mb1}}{2 C_{gs2} C_{sb1}}} \quad (16)$$

where, $\omega_o$ is the cutoff frequency, $g_m$ denotes the trans-conductance of transistors and C denotes the parasitic capacitance of transistors.

## 6.SELF-BIASED BULK-DRIVEN CASCODE CURRENT MIRROR

The existing circuit is illustrated in Figure 5 is a gate-driven CM which utilizes a compensating resistance M7 amid the gates of transistor M1 and M4 while the transistor M5 forms a super-cascode configuration with transistor M6 at the output terminal [22-25].

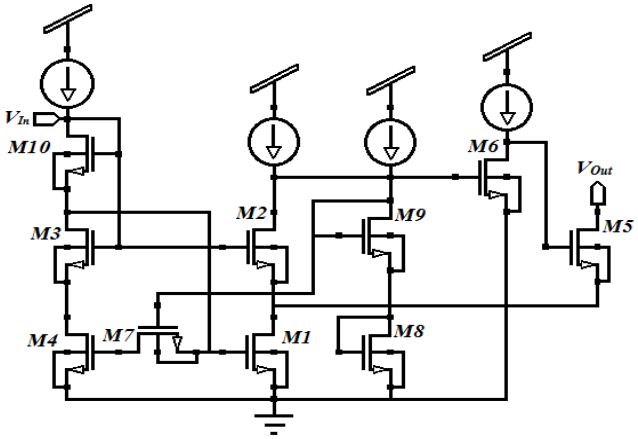


**Figure 5:** Existing Self-Biased Cascode Current Mirror

For accurate replication of current, current mirrors with high impedance is required. To increase the accuracy of analog circuitry for increased voltage signal amplitude and for accurate performance with low supply voltages high voltage swing of CM is desired. Figure 4 shows the proposed CM. Here, the transistors M1, M2, M3 and M4 forms a self-biased cascade CM. The self-biased configuration is used to obtain high output resistance, high voltage swing and to lower the power consumption.

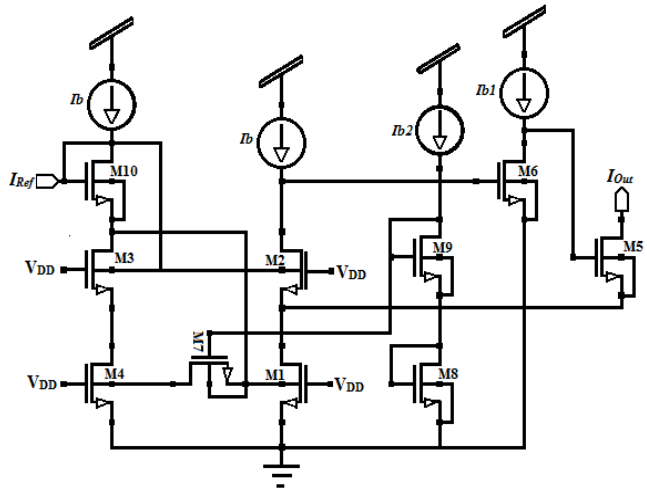


**Figure 6:** Proposed bulk-driven self-biased cascode current mirror

To allow the CM to operate at lower supply voltage the input is fed at the bulk terminals while the gate terminal of the CM is connected to a constant positive supply. It also lowers the power dissipation due to offset current which come into existence because of non-linear behavior of MOSFETs at lower voltage. A compensating resistance (M7) is introduced between the inputs of M1 and M4 to enhance the bandwidth of CM. The transistors M5 and M6 at the output forms the super-cascode configuration to enhance the output resistance of the circuit for better performance.

The small signal model of proposed CM is illustrated in Figure7.

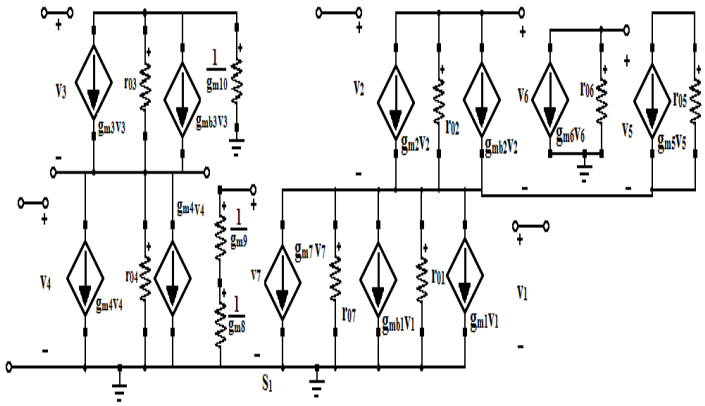


**Figure 7:** Small signal model of proposed circuit

## 7. SIMULATION RESULTS

The performance of a current mirror is measured in respect of accuracy, input/output resistance, input/output voltage compliance, bandwidth etc. The proposed circuit is designed to operate at lower voltages with higher bandwidth and better performance. Various parameters of proposed bulk-driven CM are compared with the existing gate-driven CM and is summarized in Table-1. Through analysis it was found that the bulk-driven CM circuit has better performance compared to the gate-driven CM circuit.

**Table 1:** COMPARATIVE ANALYSIS AT THE 3V SUPPLY VOLTAGE.

| Parameters | Gate-driven circuit | Bulk-driven Circuit |
|---|---|---|
| **Input resistance (GΩ)** | 1.77 | 0.59 |
| **Output resistance (KΩ)** | 1.00 | 1.55 |

**Table 2:** PARAMETER ANALYSIS AT DIFFERENT SUPPLY VOLTAGE.

| Voltage | 3V | 2V | 1V |
|---|---|---|---|
| **Power consumption (mW)** | 0.91 | 0.42 | 0.11 |
| **Input resistance (GΩ)** | 0.59 | 0.59 | 0.59 |
| **Output resistance (KΩ)** | 1.55 | 1.58 | 1.68 |

## 7. CONCLUSION

After analyzing various techniques for designing a high-performance CM the bulk-driven CM is designed. The circuit is designed to operate at lower voltage with increased bandwidth and high output resistance of the circuit. On comparing various parameters of existing and proposed current mirror it was found that the bulk-driven configuration has better input/output resistance compared to the gate-driven circuit while both the circuits utilizes equal number of transistors.

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