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Validation of the FPGA-Based Image Processing Techniques using the efficient tool like Xilinx Device Generators

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ABSTRACT

Foremost Image Enhancement's intent is to analyze an image in a direction that the output becomes more appropriate for a particular application, rather than the original picture. Image enhancement methods include a multitude of options for enhancing the image accuracy of photographs. The appropriate choice of such strategies is strongly determined by the imaging modality. FPGA has several main features that can be used as a tool for the processing of authentic time algorithms. It gives significantly higher efficiency over the programmable processor. This paper presents information regarding FPGA implementation of Image Processing Algorithms using Xilinx System Generator (XSG). Xilinx Application Generator is a Xilinx existing application process that makes FPGA hardware design relatively easy. For synthesis and simulation, the Xilinx device generator is initiated with MATLAB. To reintroduce a wide range of image processing algorithms, a model-based analysis approach will be used. Various classification algorithms for RGB to grayscale, image negativity, image retrieval, contrast stretching, threshold, boundaries extraction, as well as various image fusion methods are explored, and therefore how they are implemented using available Device Generator components.

Key words: Xilinx System Generator (XSG), Field Programmable Gate Array (FPGA), Image enhancement, Simulink, MATLAB.

1. INTRODUCTION

Image processing is a technique for applying operations to an image in order to improve it or extract useful information from it. Computer vision, remote sensing, features retrieval, facial identification, predicting and other branches of science and technology use image processing. Filtering or enhancing an image with different types of functions, As well as some other methods for removing detail from source image, is characteristic of image processing. Image processing algorithms significantly improve image quality, which is useful in Goal detection and monitoring technologies focused on medical imaging, surveillance, and robotics. Image fusion is a process of merging multiple images from the same scene to produce a new image. The goal of image fusion is to represent relevant data from multiple images in a single image. The resulting fused image would be more informative than any of the original images. Image fusion reduces confusion and improves Precision. Since the rendering of it takes a long time to create a picture in real time, the only solution is to apply the algorithm on a hardware basis. FPGAs are used to implement the logic required for an application, with different hardware designed for each purpose. To create an FPGA design using HDL such as VHDL/Verilog, it is relatively difficult to write code. The Xilinx Device Generator is a MATLAB/Simulink-based design platform that delivers high performance while reducing development time. The Xilinx System Generator is used to implement image processing algorithms. The algorithms are implemented in hardware on FPGAs using a model-based architecture approach. To create an FPGA programming file, various tasks, such as synthesis place and path, are carried out automatically. The Xilinx-based FPGAs are debugged, implemented, and tested using Device Generator, which automates the design process [3].

2. IMAGE DESIGN FLOW FOR PROCESSING WITH XILINX GENERATOR SYSTEM

DSP Device Generator is a programming tool in the Vivado® Design Suite. Device Generator allows you to use the Simulink® model-based design environment for FPGA design. In the Simulink modeling environment, designs are captured using a Xilinx-specific block array. Adders, multipliers, and registers are only a few of the basic building blocks used in many of these blocks. It also includes forward error correction blocks, FFTs, filters, and memory blocks, among other DSP building blocks. Many of these difficult blocks help the Xilinx IP core generators provide consistent results to the chosen computer. RTL synthesis and implementation (where even the gate level architecture is organized and routed within the FPGA) were systematically performed to generate the FPGA programming bit stream in the following FPGA steps. Device

Generator claims to have a black box block that lets you import RTL into Simulink and co-simulate it with ModelSim or Xilinx ISE Simulator. Hardware implementation tends to help to co-simulate the FPGA module with the pixel vector generated via MATLAB Simulink Blocks [2].

The goal of image processing is to validate a given image in such a way that perhaps the outcome is more suitable than the original picture for the intended reason. Image processing techniques can be divided into two main categories: Spatial field techniques and frequency domain techniques. Techniques in the spatial domain that work with individual pixels in an image. Approaches to processing are largely based on the strength of single pixels. Mathematical transformations such as the Fourier transforms validate frequency domain approaches.

The algorithm models are constructed using the Xilinx block collection. The image pixels given to the Xilinx models are multidimensional image signals and otherwise Color signals are separated into RGB vectors. By providing the necessary time, these models are simulated in the MATLAB/simulation environment. Device generator parameters are set and generated. When the net list is compiled, a model and programming file in verilog HDL is generated, which can be accessed using Xilinx ISE. The results are displayed in the Video Viewer, as soon as the expected results appear, they will be optimized for an acceptable FPGA implementation. The device generator itself has the ability to create user constrains files (.ucf), test vectors and test windows for the testing architecture.

3. ENHANCEMENT ALGORITHM FOR IMAGE

Improvement of image is the method of enhancing the quality and information characteristics of the original data prior to processing. Common features usually involve contrast enhancement, spatial filtering, density cutting, and many more.

The next task is to implement the Algorithm for Grayscale Image Enhancement using XSG blocks which shown in figure 1. The entire process consists of the following steps.

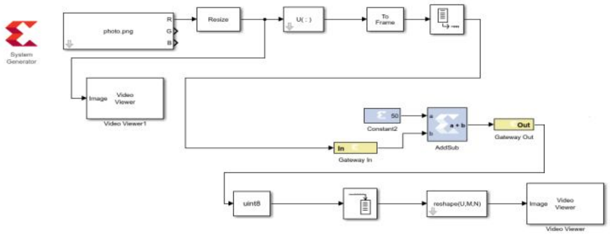

Figure 1: Enhancement algorithm using XSG

4. ALGORITHM FOR LINEARITY CONTRAST ENHANCEMENT

Linear image contrast is also known as linear contrast stretching. Continues to expand the remotely sensed data's initial digital values into a different distribution. The overall spectrum sensitivity of the display system can be used by extending the initial image input values.

In contrast stretching, we essentially increase the dynamic spectrum of grey values in the picture being processed. The Grayscale picture is extended based on the formula. New pixel = [{3*(old pixel-127)} +112] There, the product of the transformation is a new pixel. Figure 2 shows the implementation of contrast algorithm using XSG blocks.

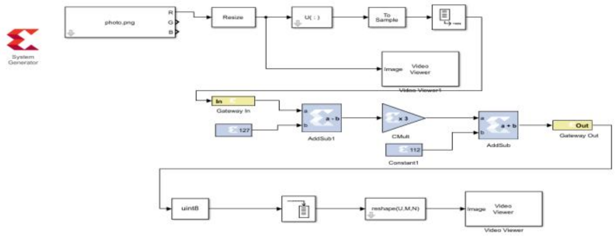

Figure 2: contrast algorithm using XSG

5. IMAGE THRESHOLDING ALGORITHM

Methods of rendering pixels above a certain threshold are white in this algorithm, while others are black. During this step, each pixel in the image is changed to a dark pixel in the image's resolution if it is less than a fixed constant value, or a white pixel if the image's intensity is greater than that constant. A Mux can also be used if the threshold values need to be replaced with white values. Figure 3 shows the implementation of threshold algorithm using XSG blocks

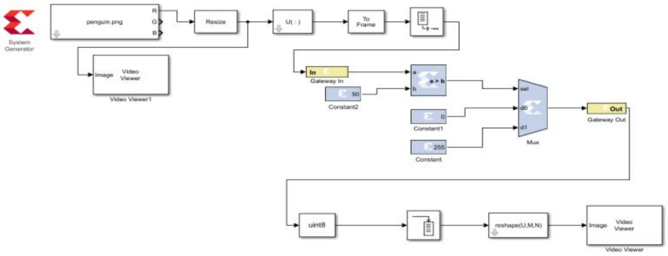

Figure 3: Threshold algorithm using XSG

6. IMAGE BACKGROUND SUBTRACTION ALGORITHM

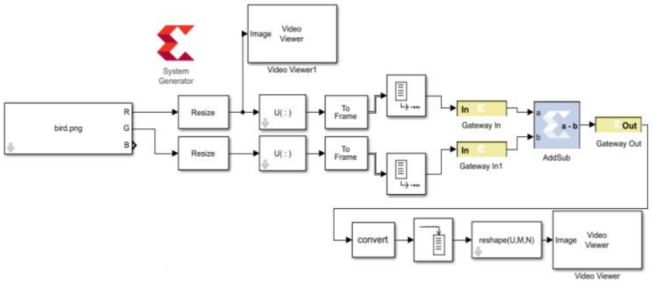

Figure 4: Background substraction using XSG

Background subtraction is a conventional algorithm for applications involving tracking to video surveillance devices. It separates moving objects using the contrast between the backdrop and the input images. The trick to the history subtraction is the establishment of a stable initial context. Figure 4 shows implementation of background subtraction using XSG blocks

7. OUTCOMES IN EXPERIMENTAL VALIDATION

The contrast stretching was implemented using (MATLAB R2020, version) and tested different types of contrast Enhancement, Linear Contrast on the image as seen in the following diagram.

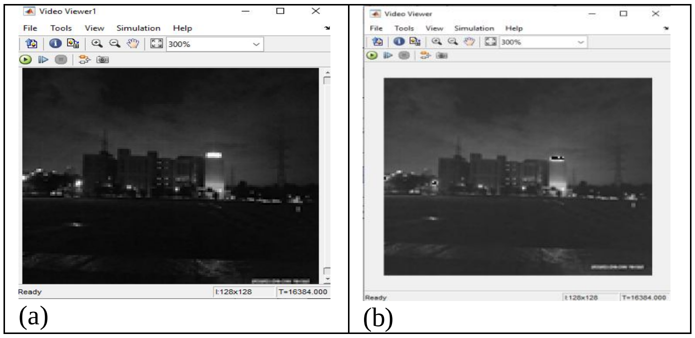

Figure 5: Grayscale Image Enhancement Result (a) original source image (b) image enhancement

Figure 5 shows a comparison of grayscale image enhancement input and output.

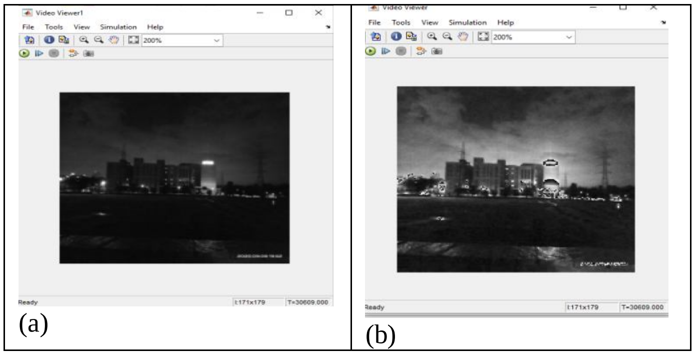

Figure 6: Result from Grayscale Contrast Stretching (a) original source image (b) image with linear contrast enhancement

Figure 6 shows a comparison of grayscale image Contrast stretching input and output.

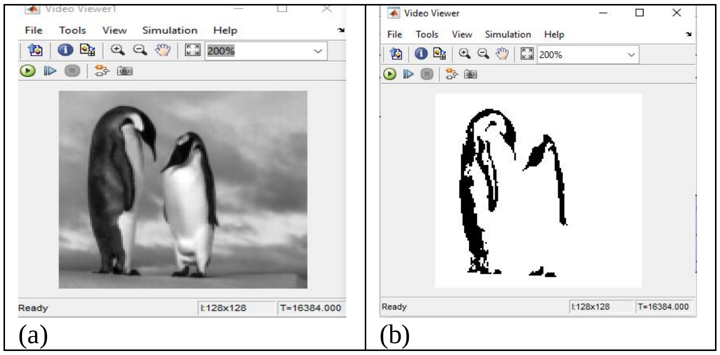

Figure 7: Result of the Grayscale Image threshold (a) original source image (b) image thresholding

Figure 7 shows a comparison of grayscale image threshold input and output.

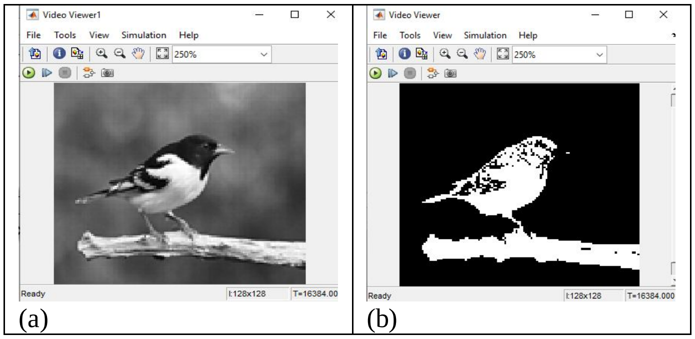

Figure 8: Result from the subtraction of background (a) original source image (b) image with background subtraction

Figure 8 shows a comparison of subtraction of background image input and output.

8. CONCLUSION

The Xilinx System Generator model offers software simulation, but most importantly, it can synthesis parallelism and speed in FPGA hardware. These features are important for image processing. The system generation tool for image processing creates a comfortable environment for design processing. All of that is easily accomplished since the processing units are constructed by block sets. Various real-time image processing algorithms are formulated and solved using XSG block set. FPGA technology has progressed as a result of the implementation of advanced FPGA technologies, and powerful methods for modeling, simulation, and synthesis have rendered FPGA a very useful tool.

9. CONCLUDING REMARKS

Image enhancing algorithms provide a wide range of image editing techniques to produce visually suitable images. The selection of these approaches is determined by the task at hand, the image quality, the viewer's characteristics, and the viewing conditions. Although the computation time of enhancement algorithms is not addressed in this article, it may be an important factor when choosing an algorithm for real-time applications. Regardless of how efficient each of these algorithms is on their own, in order to boost the picture more efficiently, a mixture of these methods will need to be devised in practise

10. FUTURE SCOPE

Image analysis is not narrowed down only to the algorithms applied above, but also to other algorithms that are operated on the area of interest, such that a detailed understanding has always been achieved. Image enhancement is taken as an application for Validation of image processing in this article, but can be applied to all Application areas. Similar analysis is conducted for many other evaluation parameters.

Target hardware is assessed in terms of development of advanced and requirements.

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REFERENCES

1. Rafael C. Gonzalez, Richard E. Woods, "**Digital Image Processing**", 4th edition, 330 Hudson Street; Prentice-Hall.
2. V. Chaitanya Deepthi, P. Surya Pradad,"**Medical Image Fusion using Xilinx System Generator in FPGA,**"*International Journal of VLSI System Design and Communication Systems* Volume.04, IssueNo.10, October-2016, Pages: 0990-0993
3. Neha. P. Raut, Prof.A.V.Gokhale, "**FPGA Implementation for Image Processing Algorithms Using Xilinx System Generator**", *IOSR Journal of VLSI and Signal Processing*, vol.2(4),pp.26-36
4. Praveen vanaparthy, Sahitya.G, Krishna Sree and Dr.C.D.Naidu, "**FPGA Implementation of Image Enhancement Algorithms for Biomedical Image Processing**," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering* , vol. 2, no. 11, pp. 5747 - 5753, November 2013
5. "DSP System Generator User Guide,"www.xilinx.com.Neha. P. Raut, Prof.A.V.Gokhale, "**FPGA Implementation for Image Processing Algorithms Using Xilinx System Generator**", *IOSR Journal of VLSI and Signal Processing*, vol.2(4),pp.26-36.
6. Ravi.s, Abdul Rahim.B, Fahimuddin shaik, "**FPGA Based Design and Implementation of Image Edge Detection Using Xilinx System Generator**," *International Journal of Engineering Trends and Technology (IJETT*), vol. 4, no. 10, pp. 4657-4660, Oct 2013.
7. Gore Tai M, Prof. S Nipanikar, "**FPGA Implementation of Image Fusion using DWT for remote sensing application**," ISSN (print): 2393-8374, (online): 2394-0697, volume-2, Issue-8, 2015..