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Profound Understanding of Various Annealing Scheme Effects on the Electrical Characteristics of Silicon Carbide based Devices

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ABSTRACT

One of the semiconductor device fabrication processes include annealing, a process by which silicon wafer is heated at higher temperature for a certain duration and then cooled down slowly. The main purpose of annealing is to mend the damage caused by ion implantation and to increase the electrical activation of dopant atoms. Traditionally, annealing has been used to enhance the material properties and electrical characteristics of conventional semiconductors devices made from silicon and gallium arsenide which found applications in normal human environment. Being a wideband gap semiconductor with noble physio thermoelectric properties, silicon carbide has been a choice of material for higher temperature and higher-power applications. Due to inertness to chemical reaction at nominal temperature, ion implantation is reported to be a preferred method for doping silicon carbide. As the ion implantation causes material destruction a suitable annealing scheme is required for recovering crystal damages and dopant activation. In this paper, effect of different annealing scheme viz. post implantation annealing, post deposition and post metallization annealing on the electrical and structural characteristics of silicon carbide-based devices reported till date are reviewed comprehensively.

Key words: Annealing, Interface, Oxide charges, Post Implantation, Silicon-Carbide.

1. INTRODUCTION

Physical limitations of material properties of silicon results in moving to wide band gap (WBG) semiconductors for higher temperature and high-power applications. Features like known device process technology, thermal oxidation comparable to that of silicon and high thermal conductivity make silicon carbide (SiC) a choice of material than other WBG semiconductors. High breakdown electric field (approx. 10 x higher than silicon), high thermal conductivity even higher than copper, twice the saturation velocity than silicon makes SiC based devices more advantageous for higher power and higher temperature applications and this semiconductor material has been under development for nearly two decades. High breakdown electric field of SiC allows thinner drift region and more doping concentration for the given breakdown voltage which results in lower ON resistance and smaller forward voltage drop of SiC power devices. Low ON resistance of SiC results in less energy loss during operation. Twice the saturation velocity of SiC than silicon provides significant reduction in switching losses and allows higher switching frequencies than Silicon (Si) based power devices [1], [2]. Wide band gap and resulting lower generation of electron-hole pairs at a given temperature results in reduction of losses due to leakage current when the switch is idle compared to silicon. In addition, higher thermal conductivity of SiC permits effective transportation of heat from the device which avoids or reduces the additional cooling requirement of high-power devices [3]-[6]. To improve the device performance especially at higher switching frequency, blocking voltage and temperature, SiC are found to be appropriate to replace the traditional silicon [7], [8]. However, factors such as rudimentary stages of many processes and challenges associated with fabrication of SiC devices prevent the use of this material to its full potential [9]-[11].

With the rapid development in the microelectronics industry, a broader research is required on the limitations and reliability of electronic devices, particularly when they have been exposed to external interferences. Electronic devices, when exposed to radiation, undergo degradation in their electrical characteristics. This can be recovered from thermal annealing treatment [12]. Annealing process which improved the electrical characteristics of silicon devices is essential for SiC devices as well. Being the most commonly used technology for doping of SiC, ion implantation causes

destruction of the material structure being bombarded [13]. Post implantation annealing is required to repair crystal defects and to increase the activation of dopants. Comprehensive survey on various annealing scheme employed in SiC devices would be helpful to determine the suitable annealing method for improving the performance of higher power and higher temperature SiC devices. In this paper, we present the effect of various annealing scheme on the electrical characteristics of SiC devices. Figure 1 present the effect of annealing on different aspects of semiconductor devices viz. dopant activation, leakage current reduction, crystal damage recovery and channel mobility improvement.

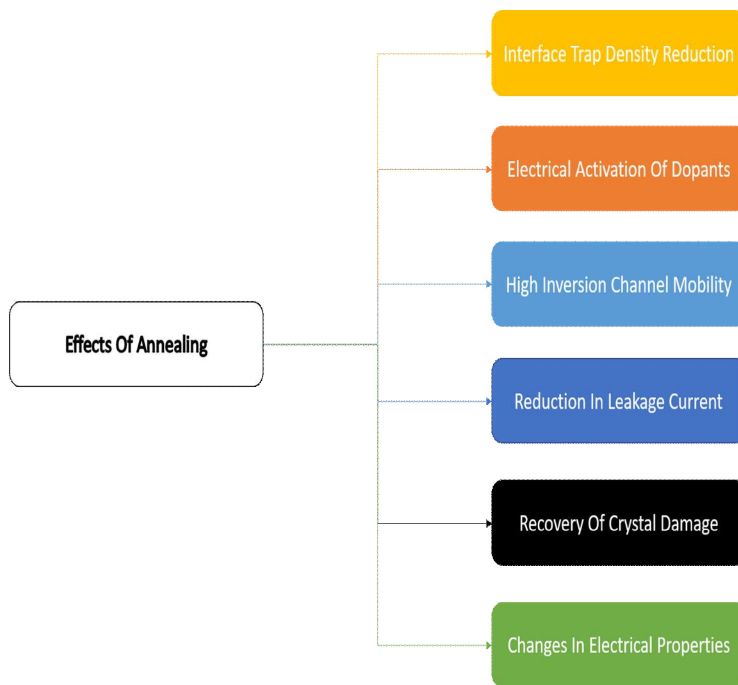

Figure 1: Various effects of Annealing

2. RELATED WORKS

2.1. Reduced Interface charge Density

Effect of annealing on Pd/SiC and Pd/SiO_2/SiC Schottky diode sensors interfacial and electronic properties for the detection of hydrogen and hydrocarbon gases at elevated temperature is investigated in [14]. Earlier experiments on Pd/SiC structure detects presence of hydrogen from its forward current, even after extended annealing at 425˚C. However, drift in the sensor properties recommended that the stabilization of the diode structure was essential. To meet this requirement, a thin layer of silicon dioxide is placed in between Pd and SiC, thus forming Pd/SiO_2/SiC. Both Pd/SiC and Pd/SiO_2/SiC diodes were annealed at 425˚C for nearly 140 hours and their electronic and interfacial properties were compared. Because of the annealing, electronic properties and the sensitivity to hydrogen for both diodes differs significantly. The Pd/SiC diode, has a broad interface region with palladium silicides (Pd_xSi) spread throughout the Pd while Pd/SiO_2/SiC diode has a sharp interface with considerably less Pd_xSi. Formation of SiO_x layer in the near surface region of the Pd likely be the reason for the relative insensitivity of the Pd/SiO_2/SiC diode to hydrogen.

The effects of Nitric oxide (NO) annealing conditions on the interfacial properties of SiO_2/SiC interface have been investigated in [15]. The interface trap density and the oxide charges get significantly reduced with increase in NO annealing temperature and annealing duration. Increasing annealing temperature to 1130˚C from 930˚C and extending annealing duration to 180 minutes from 30 minutes reduces the interface trap density. The NO annealing temperature has more effect on SiO_2/SiC interface than annealing duration. There is a linear decrease in effective oxide charges as NO annealing temperature increases, but oxide charges decays exponentially with NO annealing duration.

P.T. Lai et al. have investigated the effect of dry and wet O_2 annealing on the interfacial properties of nitrided oxides of n-type 6H-SiC MOS system [16]. Interface quality which got deteriorated by nitridation is improved after O_2 annealing as reoxidation reduces the nitridation induced interface damage. Further, lower interface state density is observed in nitrided sample annealed in wet or dry O_2 than those sample annealed in N_2. All nitrided sample exhibit better oxide reliability with significantly less shift of flat band voltage as nitridation replaces stronger Si-N bonds in the place of strained Si-O bonds. However, O_2 annealing of nitrided oxide slightly reduces the reliability as content of N_2 decreases during annealing.

S. Dhar et al. have investigated the effect of POA in NO on the interface trap density that is near the 4H–SiC conduction band edge at the oxide/(11$\bar{2}$0) 4H–SiC interface [17]. Generally, 4H-SiC MOSFETs are prone to have larger interface state density near the conduction band edge. POA of dry oxides in NO effects in considerable reduction of interface state density near the conduction band edge at the SiO_2/(11$\bar{2}$0) 4H–SiC interface and the value comparable to that on (0001) face. The above result implies that physical natures of defects that contribute to the interface states density on both the crystal faces are alike.

The effect of nitrogen annealing on the interface of SiC/SiO_2 properties of SiC MOS capacitors was investigated in [18]. Nitridation is performed by annealing the oxide in NO_x ambient. The interface properties have been characterized by interface state density, dielectric strength and normalized parallel conductance. Parallel conductance characteristics reveals that both slow state and fast state were present in samples annealed in N_2. Analysis of nitridation mechanism

shows that, the nitridation process started from near conduction band and extended till mid bandgap, resulting in partial nitridation of SiC/SiO_2 interface. Further, many slow states are started converting into fast states for those samples underwent nitrogen annealing at higher temperature. The result shows that more effective nitridation occurs at higher annealing temperature resulting in reduction of interface state densities. Different annealing scheme used for reducing the interface state density were summarized in Table 1.

Table 1: Related works discussing the interface state density reduction by Annealing

Biblical Work	Published Year	Limitations in previous work	Proposed Methodology	Results obtained
Liang-Yu Chen et al [14]	1997	Earlier experiments on Pd/SiC structure detects presence of hydrogen from its forward current, even after extended annealing at 425˚C. However, drift in the sensor properties recommended that the stabilization of the diode structure is necessary	A thin layer of silicon dioxide is placed in between SiC and Pd, thus resulting in the formation of $Pd/SiO_2/SiC$. Both Pd/SiC diodes and $Pd/SiO_2/SiC$ diodes were annealed at 425˚C for nearly 140 hours	Lesser interface state density. The Pd/SiC diode, has a broad interface region with palladium silicides (Pd_xSi) spread throughout the Pd while $Pd/SiO_2/SiC$ diode has a sharp interface with considerably less Pd_xSi
H. F. Li et al [15]	2000	Higher interface state density and oxide charges	Nitric oxide annealing is done on the interfacial properties of thermal SiO_2/SiC interface	The interface trap density and the oxide charges get significantly reduced with increase in NO annealing temperature and annealing duration. Increasing annealing temperature to 1130˚C from 930˚C and extending annealing duration to 180 minutes from 30 minutes reduces the interface trap density
P. T. Lai et al [16]	2000	Interface quality gets deteriorated by nitridation	Dry and wet O_2 annealing on the interfacial properties of nitrided oxides of n-type 6H-SiC MOS device	Lower interface state density is observed in nitrided sample annealed in wet or dry O_2 than those sample annealed in N_2
S. Dhar et al [17]	2004	Near the conduction band, edge 4H-SiC MOSFETs have larger interface state density.	POA is done in NO condition on the interface trap density near the 4H–SiC conduction band edge at the oxide/$(11\bar{2}0)$ 4H–SiC interface	POA of dry oxides in NO ambient effects in considerable decrease in interface state density that is near the conduction band edge
Z. Peng et al [18]	2016	Higher interface state density and oxide charges	Nitrogen annealing performed on SiC/SiO_2 interfacial properties of SiC MOS capacitors	Analysis of nitridation mechanism shows that, the specified nitridation process that started from near conduction band and extend upto mid bandgap, resulting in partial nitridation of SiC/SiO_2 interface

2.2 Electrical Activation of Dopant atoms

Thorough analysis of the effects of post implantation annealing on SiC electrical characteristics based double-implanted MOSFET has been simulated and the results are presented in [7]. A model to predict donor and acceptor concentrations relevant to factors viz. total doping concentration, annealing time and temperature has been

proposed. Simulation results are in excellent match with the experiments and exhibit accurately the influence of annealing steps on the parameters viz. drain current, channel potential, threshold voltage and ON-state resistance. Threshold voltage exhibit high sensitivity on annealing variables with threshold voltage shift of 1.5 V is observed for increase in the annealing temperature from 1600˚C to 1700˚C.

Post implant laser annealing of p-type Al doped 4H-SiC wafer for electrically activating the doping species and to restore crystal structure have been studied in [19]. Laser annealing induced recrystallization of the implanted 4H–SiC material is attributed to changes in the phonon mode intensity.

P. Fedeli et al. have studied the relevance of post implantation annealing duration on Al implanted 4H-SiC electrical activation [20]. The study reveals that at the annealing temperature of 1950 ᵒ C the electrical activation of Al implanted in 4H-SiC increases with annealing time up to saturation and maximum Al electrical activation is obtained at the minimum annealing duration of about 22 min.

H. Hanafusa and S. Higashi have reported the activation of P dopant atoms in 4H–SiC using high temperature thermal plasma jet (TPJ) annealing [21]. Phosphorus atoms implanted into 4H–SiC at 300 °C were activated using a very high temperature and a very high cooling rate annealing process applied using TPJ irradiation. A high activation ratio of 40 % with the maximum concentration of free electron with the value of 2.0×10^{20} cm^{-3} obtained at the maximum annealing temperature at 1630 °C and at the cooling rate of 531°C/s. Crystal orientation analysis reveals that annealing at 1630°C results in recrystallization of the sample to a 4H–SiC(0001). Samples annealed at high-temperature have fairly good crystalline uniformity as observed from image quality (IQ) values. Further, it has been reported that the carrier concentration increases considerably with cooling rate as rapid cooling may restrain the impurity deactivation. Different annealing scheme used for electrical activation of dopant atoms were given in Table 2.

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Table 2: Related works depicting electrical activation of dopants by Annealing

Biblical Work	Published Year	Limitations in previous work	Proposed Methodology	Results obtained
A. Toifl et al [7]	2019	Electrically inactive p type and n type dopants	An activation model is done to predict the acceptor and donor concentrations. Later thermal annealing is done to activate dopants	Electrically activated dopant atoms
C. Boutopoulos et al [19]	2007	Electrically inactive p type dopants	Pulsed laser (YAG laser) for Post implantation annealing to electrically activate P-type dopants of 4H-SiC	P-type dopants electrically activated
P. Fedeli et al [20]	2016	Electrically inactive of Al species	Post implantation annealing is done at the annealing temperature 1950˚C	Electrically activation of Al species
H. Hanafusa et al [21]	2018	Electrically inactive Phosphorus dopant atoms	After implantation process, phosphorus atoms are activated using thermal plasma jet annealing method	A higher activation ratio of 40% obtained with higher electron concentration

2.3 Higher Channel Mobility and Lower Leakage Current

Effects of hydrogen post-oxidation annealing (POA) on 4H-SiC MOSFET inversion channel mobility is investigated in [22]. POA in H_2 ambient at 800˚C for a duration of 30 minutes reduces the interface trap density by one order compared with un annealed sample. This improvement in interface trap density results in 3.5 times higher inversion channel mobility and the value of 110 cm^2/V.s was achieved using H_2 POA. Further, low threshold voltage of 3.1 V and channel mobility of more than 100 cm^2/V.s for a wide range of gate voltage is also achieved using H_2 POA.

Masato Noborio et al. have compared the performance of P-channel SiC MOSFETs with N_2O grown oxides and deposited SiO_2 followed by N_2O annealing fabricated on different crystal faces [23]. The MOSFET fabricated on

(0001) face with deposited oxide exhibit relatively high channel mobility of $10 cm^2/V$. s than those obtained from N_2O grown oxides value of $7 cm^2/V$. s. For $(03\bar{3}8)$ MOSFETs, the channel mobility got improved to 13 cm^2/V. s in deposited oxide than those obtained from $11 cm^2/V$. s in N_2O grown oxides. Further, the channel mobility of $(11\bar{2}0)$ face MOSFETs exhibited high value of $17 cm^2/V$. s irrespective of the gate oxides.

The effects of nitridation on channel mobility of 4H-SiC MOSFETs fabricated on various crystal faces viz. (0001), $(000\bar{1})$, and $(11\bar{2}0)$ are investigated in [24]. In a typical n-channel SiC MOSFET, the inversion channel mobility is much lower when compared to the bulk mobility in SiC. Low channel mobility is ascribed to large density of states at SiC/SiO_2 interface. Thermal annealing in N_2O and NO is found to be useful in reducing the interface state density and enhancing the channel mobility. For (0001) and $(000\bar{1})$ faces, MOSFETs channel mobility with NO-annealed oxide is higher when compared to N_2O-annealed oxide while MOSFETs on (1120) face exhibited channel mobility of more than 100 $cm^2/V{\cdot}s$ which is higher than those on (0001) and $(000\bar{1})$ faces.
The effect of annealing temperature on n-Si/n-SiC hetero junctions electrical characteristics that are fabricated by surface activated bonding (SAB) is investigated in [25]. Leakage current value of 1.7×10^{-5} mA/cm^2 at - 3 V and significantly less marked hump in the I -V characteristics were observed for low forward bias voltages for the junctions that were annealed at a higher temperature value of 700 °C. I-V characteristics improvement could be attributed to annihilation of the amorphous layer at the interface because of the annealing.

Post deposition annealing (PDA) effects and post metallization annealing (PMA) effects on $Pd/HfO_2/SiC$ metal insulator semiconductor (MIS) capacitors structural and electrical characteristics were investigated in [26]. PDA was carried out in N_2O plasma followed by N_2 while PMA was performed using Forming gas. It has been described that post deposition N_2O plasma annealing improves thermal stability of dielectric film by restraining crystallization during high temperature rapid thermal annealing (RTA) performed in N_2. High temperature RTA in N_2 succeeding the N_2O plasma annealing causes Hf silicate formation at the HfO_2/SiC interface which reduces the magnitude of both leakage current and interface state density by an order. Further, PMA in forming gas at a temperature of 350 °C for a duration of 40 minutes reduces the density of interface states by two orders of magnitude and gate leakage current by thrice than as-deposited HfO_2 film. Both PMA in Forming gas and PDA using N_2O plasma followed by N_2 were reported to improve $Pd/HfO_2/SiC$ MIS capacitors characteristics.

Effect of high temperature post deposition RTA and PMA on the $Pd/Al_2O_3/SiC$ MIS capacitors characteristics were reported in [27]. Post deposition RTA performed in N_2 ambient at the temperature of 900˚C of Al_2O_3 film results in partial crystallization causing higher gate leakage current and formation of aluminium silicide at the interface of Al_2O_3/SiC causing more than three times higher interface state density than as-deposited film. PMA in forming gas for a duration of 40 minutes of post deposition RTA annealed film improves the gate leakage current by an order. It has been reported that the combination of post deposition RTA and PMA in forming gas for 40 minutes is useful in decreasing the gate leakage current of $Pd/Al_2O_3/SiC$ MIS capacitors.
The summary of works related to channel mobility improvement and leakage current reduction by various annealing scheme were presented in Table 3.

2.4 Other Effects of Annealing

N.I. Cho et al. have studied the impact of laser annealing on the amorphous silicon carbide films deposited on to a single crystal silicon substrate [28]. SiC film deposition was carried out by plasma enhanced chemical vapor deposition, commonly known as PECVD. Laser annealing of a-SiC film using simultaneous UV and IR lasers results in formation of SiC polycrystals through the process of structure reordering.
S. Khanna et al. have explored the impact of annealing temperature on Pt/4H-SiC Schottky barrier diodes electrical characteristics [29]. As-deposited diodes exhibited non ideal behaviour with an ideality factor of value 1.71 and a barrier height calculated from the capacitance-voltage and current-voltage measurements were 1.82eV and 1.07eV respectively. Rapid thermal annealing, commonly known as RTA performed in N_2 ambience at different temperature reduces the difference in barrier height obtained by both C-V and I-V measurements and is found be less at 400˚C. Further, the ideality factor is also improved to 1.12 after annealing at 400˚C.

Milantha De Silva et al. have reported creation of low resistance Ti-SiC Ohmic contacts using laser annealing for 4H-SiC power devices [30]. This paper has demonstrated the non-equilibrium laser silicidations of Titanium (Ti) for low resistance that has ohmic contact to 4H-SiC C-face. Use of NiSi electrode on SiC results in carbon lumps at the interface of silicide/SiC causing larger contact resistance. Carbon agglomeration is controlled using nanoseconds laser annealing while contact resistance is reduced by non-equilibrium annealing condition. Pulse laser annealing with 2.5 J/cm^2 laser power in Ar ambient for a duration of 40 nanoseconds followed by rapid thermal annealing of Ti (75 nm)/SiC sample produces low specific contact resistance with the value of 2.4×10^{-4} Ωcm^2.

Takafumi Okuda et al. have investigated the effect on the surface passivation of SiC epitaxial layer deposited with SiO_2 by $POCl_3$ annealing [31]. On an uncovered surface of SiC epitaxial layers, surface recombination velocity is very high and its value varying from 1000 -5000 cm/s which reduces the lifetime of the carriers. As a surface passivation technique, thermally grown SiO_2 was ineffective in reducing the surface recombination on SiC due to large density of interface states at the interface of SiO_2/SiC. Passivation by SiO_2 with $POCl_3$ annealing has been reported to be considerably reduces both the surface recombination at the SiC epilayer and the interface state density at SiC/SiO_2 interface. Surface passivation is carried out in two steps: (i) thermal annealing in $POCl_3$ gas mixture; (ii) following thermal annealing in pure N_2. Both annealing schemes were performed at two different temperatures viz. 900 °C and 1000 °C. It has been reported that $POCl_3$ annealing followed by N_2 annealing at 1000 °C is effective for surface passivation which improves the carrier life time to as high as 3.0 µs when compared with other annealing temperature combinations.

Table 3: Related works on the higher channel mobility and leakage current reduction by Annealing

Biblical Work	**Published Year**	**Limitations in previous work**	**Proposed Methodology**	**Results obtained**
Junji Senzaki et al [22]	2002	Lower inversion channel mobility	POA is done in hydrogen ambient for the improvement of inversion channel mobility	Higher channel mobility of more than 100 cm^2/V.s
Masato Noborio et al [23]	2009	Lower channel mobility of 7 cm^2/V.s from N_2O grown oxides	SiO_2 is deposited which is followed by N_2O annealing that is fabricated on different crystal faces of MOSFET	(0001) face shows higher channel mobility of value 10 cm^2/V.s. (0038) face and (1120) face show very much higher channel mobility of values 13 cm^2/V.s and 17 cm^2/V.s respectively
Yuichiro Nanen et al [24]	2013	Normal n-type SiC MOSFET has lower inversion channel mobility than the bulk mobility in SiC, which leads to high density of states at interface.	Thermal annealing is done in N_2O and NO ambient separately	(0001) and (0001̄) faces that have been annealed with NO show higher channel mobility of 100 cm^2/V.s than the faces fabricated with N_2O annealing
T. Hayashi et al [25]	2014	Before annealing, higher leakage current has been marked	n-Si/n-SiC hetero junctions are fabricated using the process of surface activated bonding (SAB)	Reduced Leakage current value of 1.7×10^{-5} mA/cm^2 at - 3 V and I-V characteristics improvement
P. Esakky et al [26]	2017	poor thermal stability and more leakage current	PDA is carried in N_2O plasma, which is followed by N_2 and Post Metallization annealing is done using forming gas	Thermal stability has been increased by PDA, whereas, gate leakage current and interface trap density were reduced by PMA method
E. Papanasam et al [27]	2018	Post deposition RTA that is performed in N_2 ambient at 900°C of Al_2O_3 film results in partial crystallization causing higher gate leakage current and aluminum silicide formation at the Al_2O_3/SiC interface	PMA in forming gas for a duration of 40 minutes of post deposition RTA annealed film reduces the gate leakage current	The combination of post deposition RTA and PMA in forming gas for 40 minutes is useful in the reduction of the gate leakage current of Pd/Al_2O_3/SiC MIS capacitors.

Cristiano Calabretta et al. have proposed a new technique for the recovery of crystal damages induced by ion implantation using laser annealing with XeCl laser pulses for 30 ns [32]. Laser annealing helps to accomplish complete recovery of crystal in the 0.50 and 0.60 J/cm^2 energy density range, strongly reduces the concentration of carbon vacancy in the implanted area and also avoids formation of intra-bandgap carrier recombination centers. Further, laser treated crystal exhibit nearly stress-free lattice when compared with thermally annealed samples.Radiation and annealing effects of SiC MOSFETs at high voltage gate bias are reported in [33]. Both the oxide trapped charges and interface traps were estimated. At 12V gate bias, the shift of threshold voltage caused by irradiation is found to be more. But in practical application, the driving voltage of SiC MOSFETs varies from -5V to 25V. Hence it is essential to elucidate the radiation

effects of SiC MOSFETs under elevated voltage up to 25V. At 25V gate bias, the shift in threshold voltage caused by irradiation is reduced. Annealing effects of SiC-MOSFETs at positive 35V, 40V and 45V were
also investigated. The oxide trapped charges is more rapidly neutralized by 45V gate bias annealing compared to thermal annealing. The results show that by increasing driving voltage, the threshold voltage degeneration of SiC MOSFET is reduced, thus increasing the service life of devices.

Xiangyu Yang et al. have explored the outcome of forming gas annealing (FGA) on the electrical characteristics of 4H-SiC MOSFET with lanthanum silicate gate dielectric [34]. The application of SiC MOS devices are limited by poor electron mobility originating from high density of interface states (D_{it}) at SiC/SiO_2 interface. Though nitrogen or phosphorous incorporation into the gate oxide improves the mobility, the mobility obtained remains notably lower than the bulk mobility of 4H-SiC. Further, nitrogen or phosphorous incorporation may lead to unwanted negative threshold voltage (V_T) shift whereas power MOSFETs require high V_T for safe and reliable operation. Gate dielectric stack consisting of ultra-thin Lanthanum silicate ($LaSiO_x$) and thick SiO_2 enhance the mobility of SiC MOSFET while preserving an adequate positive V_T value. The $LaSiO_x$/ALD SiO_2 gate dielectric stack is formed by post deposition rapid thermal annealing of lanthanum oxide (La_2O_3)/ALD SiO_2 stack at in nitrous oxide (N_2O) at 900°C. For the given gate bias, lower electric field is maintained by high-κ silicate layer at the interface of SiC/dielectric than low-κ SiO_2 gate dielectric which helps to improves high field reliability of gate dielectric. FGA at 800°C in a gas mixture of 5 % H_2 and 95 % N_2 for a duration of 5 minutes results in significant reduction in V_T shift from 3.07 to 2.76 V while sustaining larger field effect mobility value of 122.7 cm^2/Vs.
The effects of annealing temperature on the electrochemical behavior of SiC anode films were reported in [35]. The results show that compared to unannealed film or film annealed at 600˚C, the film annealed at 900˚C shows better electrochemical performance with a reversible capacity of 580 $mAhg^{-1}$ over 100 cycles. Further, film annealed at 900˚C exhibits finer rate performance with 12.2 % reduced degradation compared to other films. The other effects of annealing described by the above works were summarized in Table4.

Table 4: Related works on the other effects of Annealing

Biblical Work	**Published Year**	**Proposed Methodology**	**Results obtained**
N. I. Cho et al [28]	2002	Laser annealing on the amorphous silicon carbide films deposited on to a single crystal silicon substrate	Laser annealing of a-SiC film using simultaneous UV and IR lasers results in formation of SiC polycrystals through the process of structure reordering
S. Khanna et al [29]	2011	Rapid thermal annealing (RTA) is performed in N_2 ambience at different temperature	difference in barrier height obtained by both C-V and I-V measurements is reduced and is found be less at 400˚C. Further, the ideality factor is also improved to 1.12 after annealing at 400˚C.
M. De Silva et al [30]	2016	Creation of Ti-SiC Ohmic contacts using laser annealing for 4H-SiC power devices	Use of NiSi electrode on SiC results in carbon lumps at the interface of silicide/SiC causing larger contact resistance. Carbon agglomeration is controlled using nanoseconds laser annealing while contact resistance is reduced by non-equilibrium annealing condition. It produces the lowest specific contact resistance with the value of 2.4×10^{-4} Ωcm^2
T. Okuda et al [31]	2016	The surface passivation of SiC epitaxial layer deposited with SiO_2 which is followed by $POCl_3$ annealing	Passivation by SiO_2 with $POCl_3$ annealing has been reported to be considerably reduces both the surface recombination at the SiC epilayer and the interface state density at SiC/SiO_2 interface
Cristiano Calabretta et al [32]	2019	Laser annealing with XeCl laser pulses for 30 ns	Recovery of crystal damage. Laser annealing helps to accomplish complete recovery of crystal in the 0.50 and 0.60 J/cm^2 energy density range, strongly reduces the concentration of carbon vacancy in the implanted area and also avoids formation of intra-bandgap carrier recombination centers

3. CONCLUSION

Annealing is usually carried out after dielectric deposition and ion implantation processes. It plays a vital role in the fabrication process of semiconductor devices. Annealing repairs, the damage that has been induced by the implantation techniques. Some of the other applications of annealing includes the dopant activation and enhancement of the electrical characteristics of the device with a specific annealing temperature and annealing time. Most of the annealing methods have been done to analyze its effect on the electrical characteristics of the particular device. This paper was to oversee various type of annealing that has been performed under certain annealing temperatures and times for improving both the interface and electrical characteristics of silicon carbide-based devices. Hence considering the purpose of the given device, particular annealing scheme can be chosen in order to obtain desirable results.

REFERENCES

1. QIAN. C, **Integration of high-κ oxides with wide band-gap semiconductors**, Ph.D. thesis, National University of Singapore, 2011.
2. Bertilsson. K, **Simulation and optimization of SiC field effect transistors**, Doctoral Thesis Stockholm, Sweden 2004.
3. Neudeck. P. G., **Silicon carbide technology**, The VLSI Handbook, ch. 5., 2006. https://doi.org/10.1201/9781420005967.ch5
4. D Venkata Ratnam et al, **Effect of High-K Dielectric materials on Mobility of Electrons**, International Journal of Emerging Trends in Engineering Research, Volume 8. No. 2, February, 2020. https://doi.org/10.30534/ijeter/2020/12822020
5. G. Rakesh Chowdary et al, **Design and Performance Evaluation of D-Flip-Flop using Various Technology Nodes**, International Journal of Emerging Trends in Engineering Research, Volume 8. No. 5, May, 2020. https://doi.org/10.30534/ijeter/2020/86852020
6. M Siva Kumar et al, **Low Power Carry Look-Ahead Adder using Transmission Gate Multiplexer**, International Journal of Emerging Trends in Engineering Research, Volume 8. No. 1, January, 2020.
7. A. Toifl, V. Šimonka, A. Hössinger, S. Selberherr, T. Grasser and J. Weinbub, **Simulation of the Effects of Postimplantation Annealing on Silicon Carbide DMOSFET Characteristics**, IEEE Transactions on Electron Devices, vol. 66, no. 7, pp. 3060-3065, July 2019.
8. T. Kimoto and J. A. Cooper, **Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications**, Hoboken, NJ, USA: Wiley, 2014. doi: 10.1002/9781118313534
9. V. Šimonka, A. Hössinger, J. Weinbub, and S. Selberherr, **Empirical model for electrical activation of Aluminum-and Boron-implanted silicon carbide**, IEEE Trans. Electron Devices, vol. 65, no. 2, pp. 674–679, Feb. 2018. doi: 10.1109/TED.2017.2786086.
10. X. She, A. Q. Huang, O. Lucía, and B. Ozpineci, **Review of silicon carbide power devices and their applications**, IEEE Trans. Ind. Electron., vol. 64, no. 10, pp. 8193–8205, Oct. 2017. doi: 10.1109/TIE.2017.2652401.
11. H. Luo et al., **Reliability Investigation of 4H-SiC MOSFET Based on TCAD Simulation**, 2018 19th International Conference on Electronic Packaging Technology (ICEPT), Shanghai, 2018, pp. 956-960.
12. Cirne, K & Leite, F & Medina, N.H. & Santos, Roberto & Silveira, M. A. G. da Silveira **Study of Thermal Annealing on Irradiated MOSFET Devices**, SForum – SBMicro, 2015.
13. N. S. Saks, A. V. Suvorov and D. C. Capell CREE Inc., Durham, North Carlina, 27, **High temperature high-dose implantation of Aluminum in 4H-SiC**, Appl. Phys. Lett., Vol. 84, No. 25, pp. 5195-5197, 2004.
14. Liang-Yu Chen, Gary W. Hunter, Philip G. Neudeck, Gaurav Bansal, Jeremy B. Petit and Dak Knight, **Comparison of interfacial and electronic properties of annealed Pd/SiC and Pd/SiO_2/SiC Schottky diode sensors**, Journal of Vacuum Science and Technology A, pp. 1228-1234, 1997.
15. H.-F. LI, S. Dimitrijev, D. Sweatman, and H.B. Harrison, **Effect of NO Annealing Conditions on Electrical Characteristics of n-type 4H-SiC MOS Capacitors**, Journal of Electronic Materials, Vol. 29, No. 8, pp. 1027-1032, 2000.
16. P. T. Lai, Supratic Chakraborty, C. L. Chan, and Y. C. Cheng, **Effects of nitridation and annealing on interface properties of thermally oxidized SiO_2/SiC metal–oxide–semiconductor system**, Applied Physics Letters, volume 76, number 25, pp. 3744-3746, 2000.
17. S. Dhar, Y. W. Song, L. C. Feldman, T. Isaacs-Smith, C. C. Tin, J. R. Williams, G. Chung, T. Nishimura, D. Starodub, T. Gustafsson, and E. Garfunkel, **Effect of nitric oxide annealing on the interface trap density**

near the conduction bandedge of 4H–SiC at the oxide/(1120)4H–SiC interface, Applied Physics Letters, volume 84, number 9, pp. 1498-1500, 2004.

18. Z. Peng et al., **Re-investigation of SiC/SiO_2 interface passivation by nitrogen annealing**, 2016 European Conference on Silicon Carbide & Related Materials (ECSCRM), Halkidiki, 2016.
19. C. Boutopoulos, P. Terzis, I. Zergioti, A.G. Kontos, K. Zekentes, K. Giannakopoulos and Y.S. Raptis, **Laser annealing of Al implanted silicon carbide: Structural and optical characterization**, Applied Surface Science 253, pp. 7912-7916, 2007.
20. P. Fedeli, M. Gorni, A. Carnera, A. Parisini, G. Alfieri, U. Grossner and R. Nipoti, **1950˚C Post Implantation Annealing of Al^+ Implanted 4H-SiC: Relevance of the Annealing Time**, ECS Journal of Solid State Science and Technology, pp. P534-P539, 2016.
21. H. Hanafusa and S. Higashi, **Activation of High-temperature-implanted Phosphorus Atoms in 4H-SiC by Atmospheric Pressure Thermal Plasma Jet Annealing**, 2018 18th International Workshop on Junction Technology (IWJT), Shanghai, 2018, doi: 10.1109/IWJT.2018.8330284.
22. Junji Senzaki, Kazutoshi Kojima, Shinsuke Harada, Ryoji Kosugi, Seiji Suzuki, Takaya Suzuki, and Kenji Fukuda, **Excellent Effects of Hydrogen Postoxidation Annealing on Inversion Channel Mobility of 4H-SiC MOSFET Fabricated on (1120) Face**, IEEE Electron Device Letters, vol. 23, no. 1, pp. 13-15, 2002.
23. Masato Noborio, Jun Suda, and Tsunenobu Kimoto, **P-Channel MOSFETs on 4H-SiC {0001} and Nonbasal Faces Fabricated by Oxide Deposition and N_2O Annealing**, IEEE Transactions on Electron Devices, vol. 56, no. 9, pp. 1953-1958, 2009.
24. Yuichiro Nanen, Muneharu Kato, Jun Suda, and Tsunenobu Kimoto, **Effects of Nitridation on 4H-SiC MOSFETs Fabricated on Various Crystal Faces**, IEEE Transactions on Electron Devices, vol. 60, no. 3, pp. 1260-1262, 2013. https://doi.org/10.1109/TED.2012.2236333
25. T. Hayashi, J. Liang, S. Nishida, N. Shigekawa and M. Arai, **Improvement in electrical properties in SAB-based n+-Si/n-4H-SiC junctions by annealing**, 2014 IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK), Kyoto, pp. 1-2, 2014.
26. P. Esakky and B. J. Kailath, **Improvement on the electrical characteristics of Pd/HfO_2/6H-SiC MIS capacitors using post deposition annealing and post metallization annealing**, *Appl. Surf. Sci.*, vol. 413, pp. 66–71, 2017.
27. E. Papanasam and B. J Kailath, **Effect of post deposition annealing and post metallization annealing on electrical and structural characteristics of Pd/Al_2O_3/6H-SiC MIS capacitors**, Microelectron. Int., vol. 35, no. 2, pp. 65–73, 2018.
28. N.I. Cho, Y.M. Kim, J.S. Lim, C. Hong, Y. Sul and C.K. Kim, **Laser annealing effect of SiC films prepared by PECVD (plasma enhanced chemical vapor deposition)**, Thin Solid Films 409, 2002.
29. S. Khanna, A. Noor, S. Neeleshwar and M.S. Tyagi, **Effect of annealing temperature on the electrical characteristics of Platinum/4H-SiC Schottky barrier diodes**, International Journal of Electronics,2011.
30. M. De Silva, T. Kawasaki, T. Kikkawa and S. Kuroki, **Low resistance Ti-SiC ohmic contacts for 4H-SiC power devices using laser annealing**, 2016 European Conference on Silicon Carbide & Related Materials (ECSCRM), Halkidiki, 2016.
31. T. Okuda, T. Kobayashi, T. Kimoto and J. Suda, **Impact of annealing temperature on surface passivation of SiC epitaxial layers with deposited SiO_2 followed by $POCl_3$ annealing**, 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Fayetteville, AR, pp. 233-235, 2016.
32. Cristiano Calabretta et al, **Laser Annealing of P and Al Implanted 4H-SiC Epitaxial Layerss**, Materials, 12(20), 3362, 2019. https://doi.org/10.3390/ma12203362
33. Dongqing Hu, Jingwei Zhang, Yunpeng Jia, Yu Wu, **Radiation and annealing effects of SiC MOSFETs at high voltage gate bias**, 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, 2018.
34. X. Yang, B. Lee and V. Misra, **Improvement of Threshold Voltage Reliability of 4H-SiC MOSFETs With Lanthanum Silicate by High Temperature Forming Gas Anneal**, in IEEE Electron Device Letters, vol. 39, no. 2, pp. 244-247, Feb. 2018.
35. F. Zhang, Y.Z. Cao, X.X. He, F. Li, J.J. Shi, Q.A. Huang and X.D. Huang, **Effects of Annealing Temperatures on the Electrochemical Properties of Silicon Carbide Anode Film for Lithium Ion Battery**, 019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Xi'an, China, 2019. https://doi.org/10.1109/EDSSC.2019.8754064