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FPGA Based Efficient LFSR Architecture for Verification Using Optimized BIST Technique

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ABSTRACT

Built InSelf Test (BIST) is generally used to verify the correctness of the design in real time at hardware level. For this reason, the test architecture must generate most of the test cases in random manner upon which the signature is created and verified. In this paper, we propose FPGA based Efficient Linear Feedback Shift Register (LFSR) Architecture for verification of Digital circuits using Optimized BIST Technique. The modified LFSR has been designed with minimum XOR gates and clock gating circuit which improves the performance of the system. The test patterns generated are applied to standard architecture IC 74283 of 74xx series and response is analyzed using Multiple Input Signature Register (MISR) response analyzer to validate the results. The entire architecture is implemented on Diligent ATLYS Spartan-6 (xc6slx45-3csg321) FPGA device and Xilinx ISE 14.5 tool is used to synthesize the architecture and validate the parameters such as area, speed and power.

Key words :LFSR (linear feedback shift register), PRPG (pseudo random pattern generator), MISR(multiple input signature register), Primitive polynomial and BIST (built in self test).

1. INTRODUCTION

Verification is a major part in any design which ensures that the design operates in correct manner within the design specifications. This makes the verification crucial for any design which must have to perform correctly at every design stage. The verification has a major role to play in the cost of the IC manufacturing process. The verification technique must be accurate with less amount of testing time and it must cover all the possible combinations. Like other design methods, verification is an art of finalizing the technique based on application essential for any VLSI design. In general, the VLSI verification is mainly divided into two parts namely software and hardware verification, respectively. In software verification, the soft version of the design which is coded using some software languages is verified using some pieces of software codes which is normally known as testbench. On the other hand, in hardware verification the fabricated chip using VLSI technique is verified physically by some techniques. Normally, Built In Self-Test (BIST) is a

common hardware verification technique used in VLSI design which is added with the processing element to check the correctness of the operation of it. The extra circuit added for this reason increases the area but reduces the overall test time and cost. This type of verification is done through the uses of signature analysis technique where a Pseudo-Random Sequence Generator (PRSG) is used to generate pseudo random signal which is fed as input to the design and the corresponding signature generated by the design is analyzed by Signature Analyzer to decide the correctness of the unit.

2. LITERATURE SURVEYS

Many works related to the verification were presented. Some of the works are as follows:

Anju Rajput [1] presented a BIST architecture to check different types of multipliers operations. Here the linear feedback shift register is used to generate random number through which the operation of the multiplier circuit is verified. Xilinx ISE 14.4 is used to synthesis the design and simulated using ModelSim 10.0c. Ben John et al., [2] implemented BIST using verilog to test VLSI circuits. LFSR is used to generate test pattern for the circuits and the same circuit is also used as response monitor. This architecture is designed using verilog language and synthesize through Xilinx 14.2 tool. Devika and Ramesh [3] presented programmable BIST architecture. The whole module is designed through Test pattern generator, Response Analyzer, ROM, and Comparator respectively. The architecture is simulated for different input sizes and synthesize it for Xilinx Spartan 3E and Spartan 6 FPGA boards. The author compares the hardware parameters of this architecture with existing.

Ramesh et al., [4] presented BIST architecture using power reduction technique to reduce the extra power required for the verification without affecting the test coverage. To implement this, the authors considers different types of power dissipations occurs in the BIST architecture and try to minimize those at architectural level. This architecture is implemented and tested on Spartan 3 FPGA. Gunavathil et al.,

[5] presented a new test pattern generator circuit for BIST. In this case the authors tried to reduce the power required for switching operations. The whole design is mainly based on ROM where the test patterns are stored. The whole design is implemented and tested in backend simulation tools. Divya et al., [6] presented memory verification through BIST architecture. For this case, the authors considered stuck at faults only. Moreover, to reduce test time, test cases are reduced which reduce the effectiveness of the architecture. The architecture is tested in Xilinx 14.2 tool. Supriya et al. [7] presented UART communication where BIST is implemented along with UART which can communicate with any design. This architecture is designed using VHDL language and synthesize through Xilinx ISE tool for Spartan 3 FPGA.

Preethy and Rony [8] presented verification of memory in SOC chip where multiple memory cores are considered in parallel format. This case the authors modified the March test technique is used which is designed using HDL language and synthesize through Xilinx ISE tool. HaribhanuPriya et al. [9] presented BIST architecture for memory testing where the architecture also capable of repair the memories in the case of any single fault occurs. In this case, time bouncing and signature prediction schemes are used which is mainly based algorithmic rule for constitutional self-repair (BISR) programme. The architecture is implemented using Xilinx ISE tool. Praveen and Shanmukha [10] presented low power test vector generation for BIST circuits where bit complements test vector generation technique is used. In this case the bulkiness of the test cases are reduced by almost 50%. The architecture is implemented by backend simulation and synthesis tool. Zhiting Lin et al. [11] presented a BIST architecture to test embedded SRAM where cost effective solutions are provided. The March algorithm is used to design the BIST architecture. The external signals are used to control the BIST which allow any small changes in the test patterns through input data. Pushpraj and Priyanka [12] presented BIST architecture for multiplier circuits which is implemented using VHDL language.Nandhini et al. [13] presented novel LFSR architecture for BIST toreduce the power consumption of the whole architecture. To reduce the power consumption, the authors reduce the transitions of intermediate nodes of the architecture named as BS-LFSR technique.Gayathri and V.Sanjivee [14] presented LFSR architecture to build BIST where reseeding technique with NLFSR architecture is used.

3. PROPOSED ARCHITECTURE

The block diagram of BIST architecture consisting of Controller, PRSG, Circuit Under Test, Response Analyzer, ROM and Comparator is shown in Figure 1. The random input sequences are generated by PRSG where the clock gated circuits are used which is then fed to the Circuit Under Test block. The signature bits are generated from the output of Circuit Under Test with the help of MISR block which is then compared with the corresponding signatures stored in ROM using a Comparator block depending upon which the architecture generates test results to indicate the status of the Circuit Under Test. The controller block is used to synchronize the entire operation of the circuit in proper manner. The novelty lies with the modified LFSR with reduced number of XOR gates with clock gating technique. Also the adder circuit is modified to parallel feed the test pattern which reduces the considerable testing time of the circuit.

3.1 Controller

For proper operation of any hardware architecture, it is essential to control the data-flow from one block to another block in proper sequences. This is normally implemented by control signals through which each blocks turns on and off conditionally.

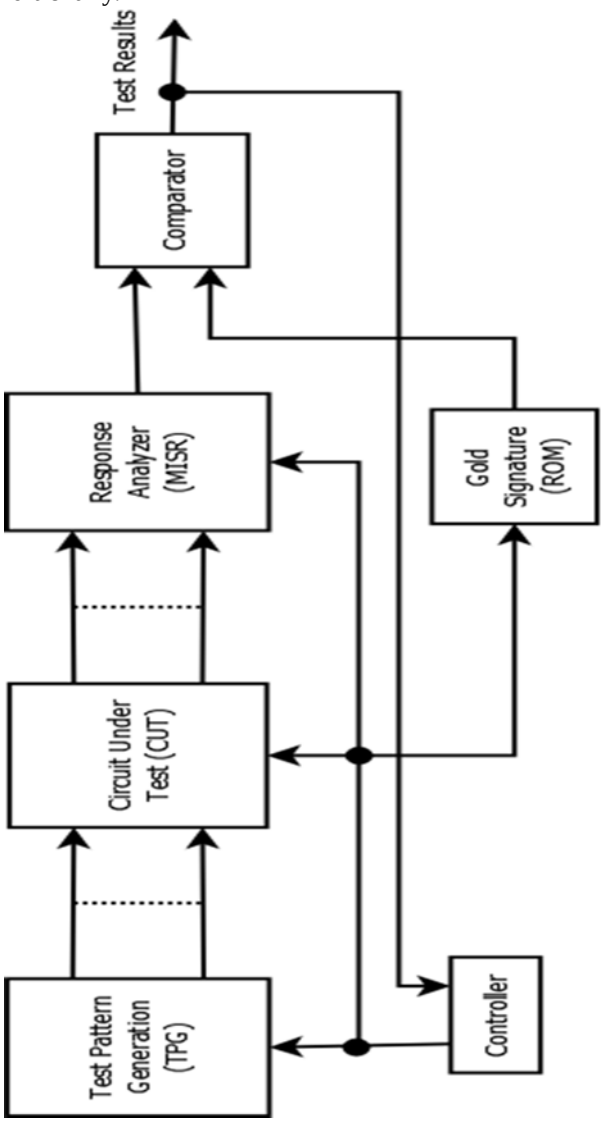

Figure 1: Architecture of the Enhanced Fuzzy Resolution Mechanism using ANFIS

3.2Test Pattern Generator

The test vectors are generated by the Test Pattern Generator block which are used to test the circuit by feeding the required test vector to the design. Normally PRSG or LFSR is used in

this case which generates pseudo random patterns based on the feedback polynomial. It is a kind of shift register where selected bits called taps are XORed to construct the feedback polynomial which is fed to LSB flip-flop of LFSR. The basic theory behind LFSR used is Galois field. Every arithmetic operation in LFSR is based on modulo 2 where multiplication is equivalent to AND operation and addition is considered as XOR operation. Shifting bits from one flip flop to other, pseudo random sequences are generated in PRSG where a large amount of power is consumed at the time of each shift operation performed. To minimize the power, it is essential to skip some shift operations which is implemented by clock gating circuit along with normal PRSG/LFSR. To get optimized architecture in-terms of both power and hardware utilizations, modular PRSG architecture is used with clock gating circuit. The architecture of the proposed PRSG is shown in Figure 2 and the architecture of the Clock Gating circuit [15] is shown in Figure 3 respectively.

The internal structure of an n-bit LFSR using characteristic polynomial of degree n over GF (2) defines characteristic polynomial [16] is given by y(x)

$$y(x) = 1 + h_1x + h_2x^2 + \cdots + h_nx^n \quad (1)$$

Where, coefficients hi denote the existence of feedback path

$$\text{Degree of Polynomial} = n \quad (2)$$

$$\text{Max Length of sequences generated} = 2n - 1 \quad (3)$$

The polynomials which cover maximum length are called primitive polynomials. The polynomial is used to generate the proposed PRSG which is implemented using Galois to reduce the critical path delay for 8 bits is given equation (4)

$$\text{PSRG Polynomial} = x^8 + x^6 + x^5 + x^4 + 1 \quad (4)$$

The powers of x terms represent the tapped bits and the term one represents the input to first flip-flop. So these polynomials are fed to the proposed LFSR in Logic BIST applications. In normal LFSR with Fibonacci has more critical delay due to external feedback. In our work Galois LFSR has been use which reduces the critical delay due to internal feedback.

3.3 Clock Gating

Before providing clock to every flip flop of LFSR we need to compare input and output and when both are same then clock should be gated. This means that if a particular flop of TPG having same data as previous to shift then it will be disconnected from clock and will not come into the shifting operation and then get eliminated from LFSR till the shift operation get finished and the eliminated flop power also disappear from total power.

3.4 Circuit Under Test

It is the entire circuit or a portion of the circuit which we want to test through BIST technique can be considered as Circuit Under Test. This circuit is visible but can be characterized by its input and output relations which are normally sequential, combinational or a memory. In our work the combinational circuit is consider verifying the working of the BIST architecture. These circuits are normally using gate level modelling and depending upon the characteristics of the circuit, the size of PRSG and Multiple Input Signature Register (MISR) should be decided. For analyzing. 74283 circuit architecture present in standard 74X-Series Circuits [17] is used as Circuit Under Test.

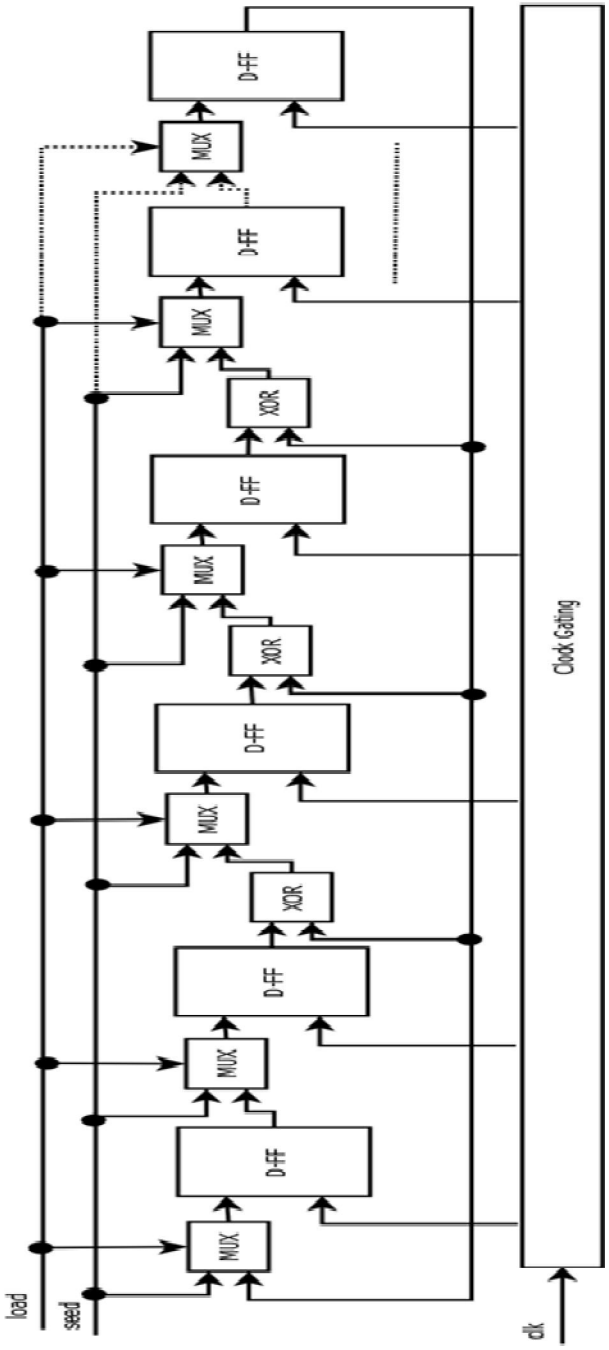

Figure 2: Proposed PRSG Architecture

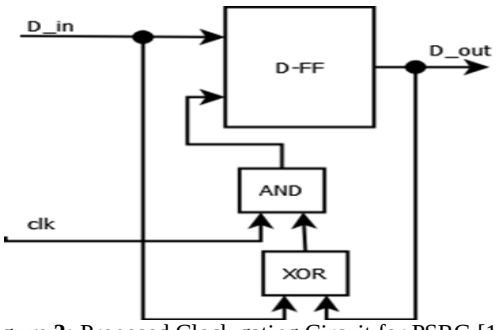

Figure 3: Proposed Clock gating Circuit for PSRG [13]

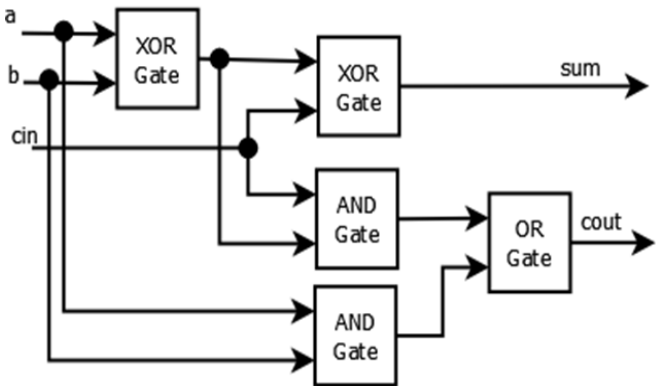

Figure 4: Full Adder Circuit

But due to the presence of more than one input with different bit sizes, it is difficult to apply the input directly from the Test Pattern Generator block. As a result, the whole test patterns are divided into input data (a, b and cin) depending upon the binary bit positions shown in the Figure 5 through Concatenation operations. Similarly, at the output side, the different output ports (sum and cout) are merged through Merger block. This process helps to synchronize the whole design and helpful to store all the output signals in a single file.

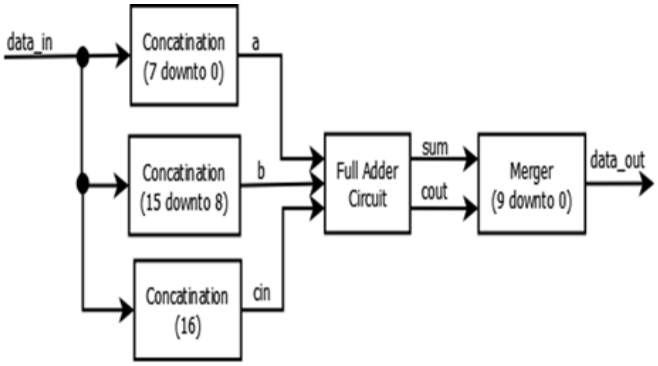

Figure 5: Modification of Adder Circuit to feed Test Patterns

3.5 Response Analyzer

The Response Analyzer is made of MISR which is used to generate unique responses using the data streams generated from the Circuit Under Test which is also known as signatures. This avoids the storing of responses which saves the memory. Due to linear properties, the Response Analyzer can be made by simple LFSR. Signature is thus obtained as a result of performing modulo operation of each primary output with feedback polynomial and then XOR sum of the resultant. The N-bit modular MISR architecture is shown in Figure 6. The resolution of N can be changed according to the design requirements and is designed with efficient resource utilizations. The clk is synchronized with all the D Flip Flops for proper operation of the circuit.

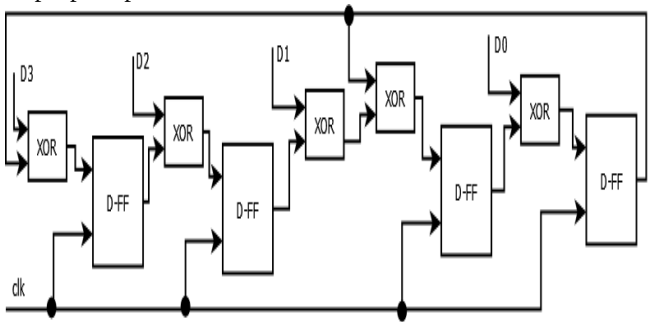

Figure 6: N-bit modular MISR architecture

3.6 ROM

It is a Memory module where the expected signatures of the correctly designed Circuit Under Test for all possible input are stored. These values are pre-calculated through simulations. Depending upon these signature values, the test result of the architecture is generated. Normally Golden Signature is used for this testing purpose. Since, this is hardware level testing, so the data present in the memory must not erased or modified at any condition. As a result, ROM is used here which is shown in Figure 7. The correct signatures are stored in the ROM Array which is read by the address generated by the Counter block to get correct signature values.

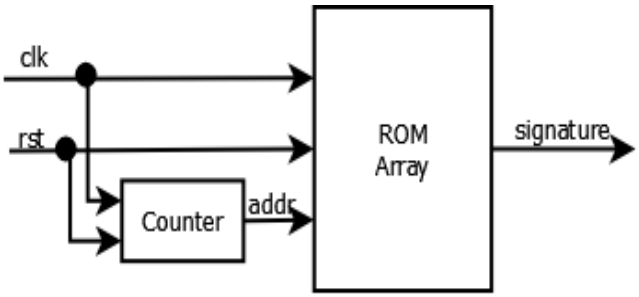

Figure 7: ROM architecture

3.6 Comparator

It compares the output of the Response Analyzer and ROM based on whether the given number is equal, greater, or less. This is the comparison between golden signature stored in ROM and the result and signature from MISR. Based on the result, the status of the circuit is decided. When the Golden signatures are equal to the signatures generated by MISR from the Circuit Under Test then the circuit is fault-free or else it is in faulty conditions.

The Comparator architecture is shown in the Figure 8 which consists of Comparator and Decision block. The comparator

block compares the stored signature with corresponding signatures generated by the Circuit Under Test block which is then used by the Decision block to decide the status of the Circuit Under Test.

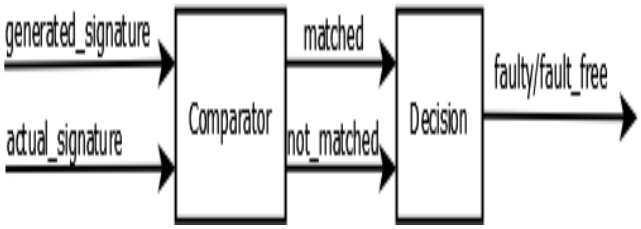

Figure 8: Comparator architecture

4. FPGA IMPLEMENTATION

The proposed architecture is implemented on Diligent Spartan-6 FPGA [18] where standard VHDL language [19] is used to code the entire architecture whereas Xilinx ISE 14.5 [20] is used to simulate and synthesize the architecture.

4.1 PSRG or LFSR

The generated technology schematic of the proposed PSRG or LFSR is shown in Figure 9 from where it can be observed that most of the logic components are connected in simple serial format which reduce the design complexity and reduce hardware utilizations. The simulation waveform of the proposed PSRG or LFSR is shown in Figure 10 where at each clock cycle pseudo random output is generating from the circuit.

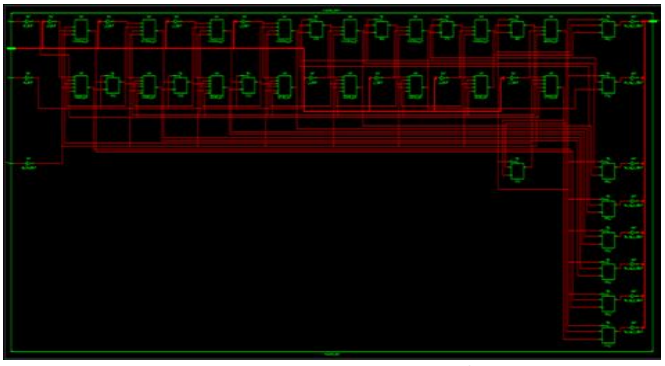

Figure 9: Technology Schematic of PSRG

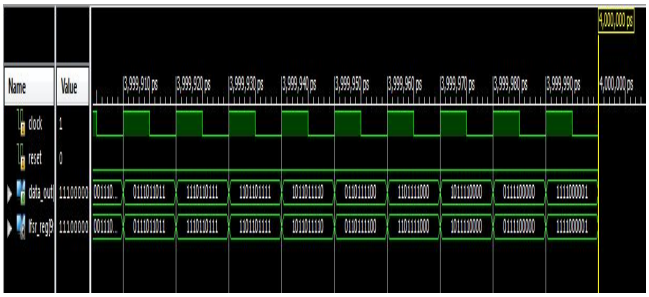

Figure 10: Simulation Result of PSRG

The hardware utilizations of the proposed PRSG or LFSR is given in Table 1 from which the proposed PRSG or LFSR architecture requires 8 Slice Registers, 16 Slice LUTs and 8 LUT-FF pairs. The power is obtained using Xilinx X-power Analyzer which is an approximate measure of 36 mw. It will be less compared to existing techniques due to minimum XOR gates in LFSR combined with clock gating circuit.

Table 1: Hardware Utilizations of Proposed PSRG

Parameters	Logic Utilization
FPGA	Spartan-6 (xc6slx45-3csg321)
Slice Registers	8
Slice LUTs	16
fully used LUT-FF pairs	8
Total Power (W)	0.036
Minimum input arrival time before clock (ns)	2.779
Maximum output required time after clock (ns)	3.597

4.2 BIST

The technology schematic of the BIST architecture using proposed PSRG is shown in Figure 11.

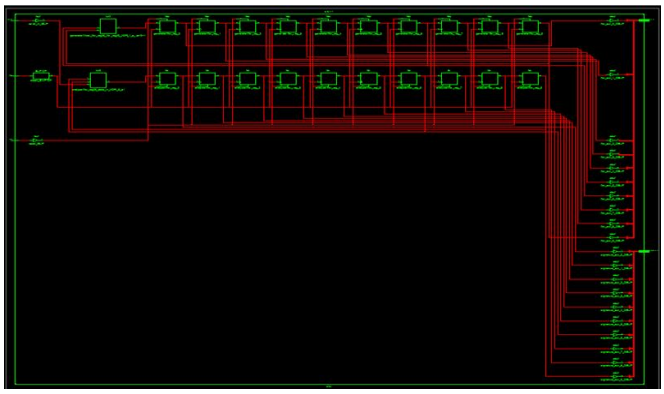

Figure 11: Technology Schematic of BIST

The simulation result of the BIST architecture for fault free and fault detection circuit is as shown in Figure 12 and Figure 13 respectively. To display the result, one extra signal status is used depending upon the test result this port generates a predefined number indicating the status. If the status is ‘1’ indicates fault free circuit else if it is ‘0' then there is fault detection. For automatic status detection, the status is displayed in the console window. The simulation results are obtained using Xilinx ISIM tool.

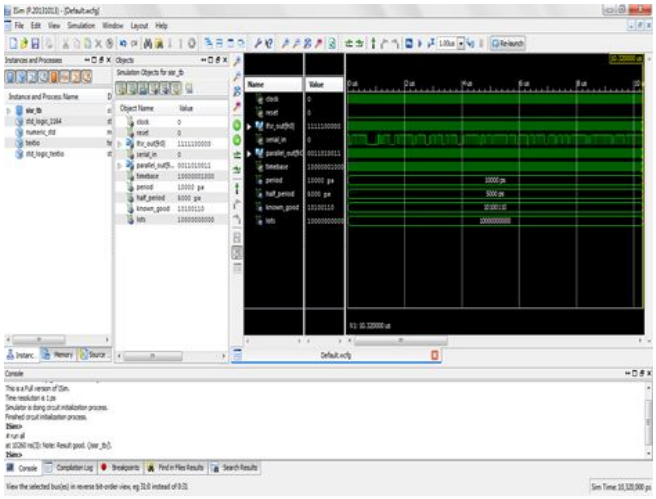

Figure 12: Simulation Results of BIST for Fault-Free Circuit

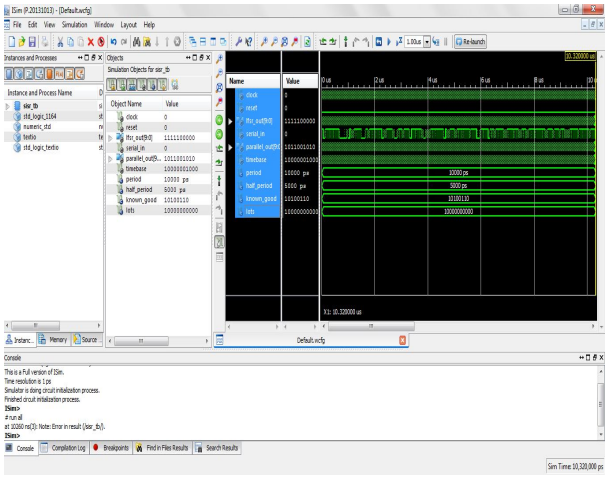

Figure 13: Simulation Results of BIST for Faulty Circuit

The hardware utilizations of the BIST architecture is given in Table 2 which requires 20 Slice Registers, 2 Slice LUTs, 2 LUT-FF pairs and the maximum operating frequency is 687.771 MHz.

Table 2: Hardware Utilizations of BIST Architecture

Parameters	Logic Utilization
FPGA	Spartan-6 (xc6slx45-3csg321)
Slice Registers	20
Slice LUTs	2
fully used LUT-FF pairs	2
bonded IOBs	23
BUFG/BUFGCTRLs	1
Maximum Frequency (MHz)	678.771
Minimum period (ns)	1.47

5. COMPARISONS WITH EXISTING TECHNIQUES

The comparison of hardware utilizations of the proposed PRSG with existing is given in Table 3 where the proposed architecture is compared with the existing PRSG architecture presented by Ramesh et al. [4] and Devika and Ramesh [16] respectively. From the table, it is observed that the proposed PRSG requires less hardware resources than existing which proves the efficiency of the proposed PRSG architecture over existing.

Table 3: Comparisons of Hardware Utilizations of PRSG block

Parameters	Ramesh et al. [4]	Devika and Ramesh [16]	Proposed Architecture
FPGA	Spartan-3	Spartan-3E	Spartan-6
Slice Registers	103	10	8
Slice LUTs	----	17	16
Fully used LUT-FF pairs	104	16	8

5. CONCLUSION

In this paper, BIST architecture with modified LFSR is to verify Digital VLSI circuits in real time is proposed. Here the Pseudo Random Sequence Generator (PRSG) architecture is modified with minimum gates with clock gating circuit. The use of modular version of PRSG reduces the overall hardware utilizations by the block whereas the power consumption is also reduced by inserting Clock Gating technique into it. The comparison table prove that the proposed PRSG architecture requires less hardware than existing. In future the hybrid method of verification techniques can be explored to improve the area and speed utilization of the entire system.

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