ISSN 2347 - 3983
Volume 8. No. 10, October 2020
International Journal of Emerging Trends in Engineering Research
Available Online at http://www.warse.org/IJETER/static/pdf/file/ijeter1328102020.pdf
https://doi.org/10.30534/ijeter/2020/1328102020

HIGH SPEED AND LOW POWER MULTIPLIERS DESIGNED USING REVERSIBLE LOGIC METHODS

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ABSTRACT

Multiplier circuits take an important role in developing various digital gadgets, digital signal processing (DSP) and many other tasks. Multipliers are the main building blocks in conducting operations like convolution, filtering, etc. The research focuses on the nature of high-speed multipliers, decreased power consumption, and a lower region of low complexity. Recently, reversible logic has seen widespread use in the architecture of multipliers, low-power CMOS circuits, optical data processing, quantum circuits, etc. This paper uses reversible logic to construct compact multipliers using Vedic mathematics, Baugh-Wooley and Wallace tree architectures. In specific, the suggested multiplier designs are based on logics such as the reversible Half Adder, the reversible Full Adder, the Dual Key Gate and the Kogge Stone Adder. In order to ensure improved performance, a thorough distinction is made between different multipliers based on reversible logic circuits. The results of the proposed design are simulated and synthesized using the Xilinx ISE method.

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Key words : Baugh Wooley Multiplier (BWM), Full Adder (FA), Half adder (HA), Reversible Logic, Vedic mathematics, Xilinx ISE.

1. INTRODUCTION

The demand for high-speed multipliers has increased tremendously in recent years. In past literature several research efforts have been successfully carried out to design an energy-efficient multiplier [1-3]. Past studies have demonstrated that the circuits and systems designed in conventional design methods using irreversible logic results in higher power consumption and increased energy dissipation because of information loss [4]. The critical factor in the design and manufacturing of DSP devices for high-performance applications is low power usage and reduced delay [5-7]. The multiplier is a crucial circuit in a DSP application. The applications like Filtering (FIR, IIR), Fourier Transforms (FFT), convolution, etc. are depending on the multiplier circuits [8], [9], [10]. Multiplication is the most salient operations in almost all the computer processor, although it is more expensive and time-consuming [11, 12, and 13]. Multiplication can be carried out by different calculation problems that are regulated by speed [14]. Increased speed, reduced power and decreased area were observed using the multiplication process [15].

Reversible circuits are identical to standard circuits of logic except for gates that are implemented using reversible logic. There is a special one-to-one mapping of reversible gates with the inputs and outputs contradicting the traditional logic gates [16, 17]. Early work on reversible computing was carried out by R. Landauer's in early 1960s. If one bit of information is lost, the circuit dissipates heat in the form of energy which is at least KTln2 joules, where K and T are the Boltzmann constant and absolute temperature respectively [18]. The reversible logic gates are used to design the energy efficient circuits, and according to C. H. Bennett's research, reversible logic are capable of preventing KTln2 joules of energy dissipation in a circuit [19]. In [20], a 4*4 parallel multiplier has been designed. The design included 3 steps viz. Partial Product Generation (PPG), Partial Product Dropping (PPD) and Addition of the decreased partial product produced in the previous steps. In [21], a new reversible gate called the HNG gate was proposed by the authors. Also the work [22] implemented the same technique as the two previous works, multiplying in two stages. Peres Full Adder Gate (PFAG) has been suggested by the researchers in this study. Also in this work, like the existing works, Peres gates were used to get the PPG. In [23], a new reversible gate named the RAM gate was introduced by the researchers. In [24], the system of Wallace Tree was planned to use two

4-fold reversible multiplier circuits. The reversible multipliers were designed using the reversible gates like Feynman (FG), Peres (PG), Toffoli (TG), DKG and several other block operated as reversible half-adder and full-adder.

In this paper the half adders and full adders of the multiplier structure are replaced by the reversible logic gates. Instead of using a single reversible gate, here two different RG (Reversible gates) are used to design the adder. So that the garbage output is reduced, this in turn helps to reduce the delay and power consumed by the RG. All the existing design conceded with the garbage outputs, Ancillary inputs, quantum cost. But in this work, concentration has been focused on the parameters such as delay and power calculation. The proposed method has significantly reduced the depth of circuits and enhanced the speed. The delay and power in the proposed reversible multiplier design was very low compared with other existing circuit designs.

The rest of the paper is organized as follows: Section 2 briefs about the structure and its functionality of the basic reversible logic gates. The proposed reversible adder structure is described in the section III. The detailed architecture of various multipliers is studied in Section IV with the proposed Reversible Half Adder and Reversible Full Adder. Finally, the result has been discussed and analyzed with a conclusion of the proposed work.

2. Structure and Functionality of Reversible Gates

In general A (x, y) reversible logic gate has x number of inputs and y number of outputs. For example, A (1, 1) reversible logic is labeled as a gate for copying the inputs, i.e., the input goes unchanged through the gate. Meanwhile, there exists multiple input and output reversible gates and few are discussed below:

2.1 NOT GATE

It is the only reversible and irreversible logic gate [25], with input as A and output as A', which is shown in the below Figure.1

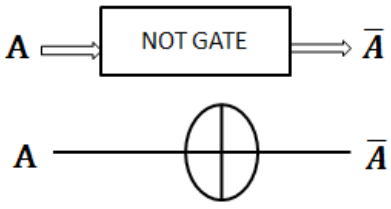

Figure. 1. Reversible NOT Gate

2.2 FEYNMAN GATE

With only 2 * 2 Feynman gates [26] and converters, all reversible linear functions can be created. The gate of Feynman is called a CNOT gate (copying gate), with two inputs and two output logic gates. The logic function W = X and V = $X \oplus Y$ are shown in Figure.2. Feynman gate with an input as (X, Y) and output as (W, V).

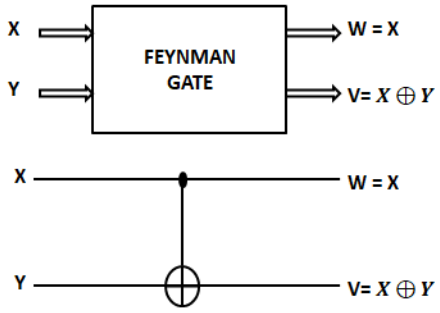

Figure. 2. FEYNMAN Gate

2.3 TOFFOLI GATE

The size of the Toffoli gate is incredibly small, which the most advantage of the gate. This logic gate has three inputs and three output [27]. The Toffoli portal is a "controlled-controlled-not gate" (CCNOT), in account of the two inputs (Y and Z) remain stable and when B = 1 and C = 1, the entrance inverts A. The logical function W = X, V = Y, U = Z ^ (XY), which is shown at Figure.3 is, in Toffoli Gate with input as (X, Y, Z) and output as (W, V, U).

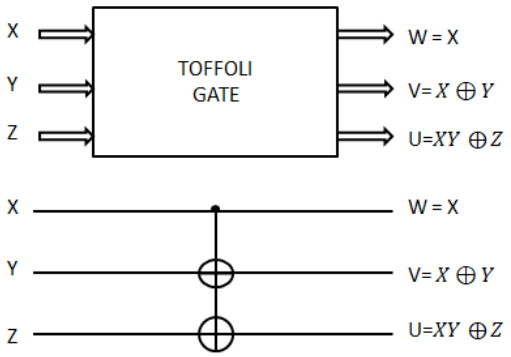

Figure. 3. TOFFOLI gate

2.4 DUAL KEY GATE

A 4 * 4 reversible DKG gate will function as a FA and a full subtractor only as shown in Figure. 4a and 4b. If A = 0 is used, the DKG gate serves as a FA, while A = 1 it will work as full Subtractor. To create special product combinations, a complete reversible circuit has been checked that at least 2 or 3 garbage outputs are required [26], [27].

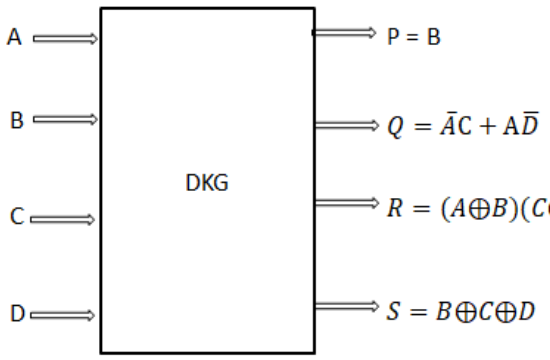

Figure. 4a. DKG gate

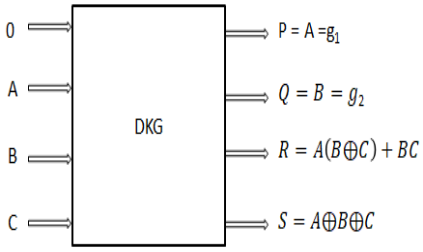

Figure. 4b. DKG gate as a Full adder

In the design of reversible logic gates, established design constraints have to be followed strictly or the constraints could be optimized for implementing any particular Boolean functions. It is essential that the number of inputs and outputs are retained equally in a reversible logic circuit. Similarly, each input pattern will have a specific output pattern. In a reversible logic circuit, fan out is not allowed as each output is used only once. Finally, the resulting reversible circuit should be an acyclic circuit. It must be taken care of some other considerations, the reversible circuits must use a less number of constant inputs, logic depth or gate rates, and the layout must be designed to minimize the number of garbage outputs. [28]. Toffoli gate and the Feynman Gates are used to design the Half Adder and Full Adder circuits which is discussed in the following sections.

3. Proposed Reversible Adders

In this section, several architectures of adders with reversible logic gates have been designed and are discussed as follows.

Approach I: Reversible Ripple Carry Adder (RCA) using DKG gate

From the discussion in the earlier section, the DKG gate can be used either as an adder or as a subtractor. Hence, in this work a reversible RCA using the DKG is designed which is shown in the Figure. 5. A 4 * 4 DKG reversible logic gate that can operate only as a completely reversible adder or as a complete subtractor. It can be verified whether a common output pattern is uniquely specified input patterns. If the A=0 input acts as a reversible DKG Full Adder gate and the A=1 input, then it acts as a DKG Full Subtractor Gate reversible. At least two waste outputs have been demonstrated to ensure the unique output combinations by the reversible full-adder circuit.

Approach II: Reversible Ripple Carry Adder using Feynman and Toffoli gates

Similarly, in the next approach the Reversible Half Adder (RHA) is designed using one Toffoli gate and one Feynman Gate which is shown in Figure 6. As per the logic, the single full adder performs addition of two 1-bit numbers and a carry input. Also, a reversible full adder (RFA) can be designed using two RHA and one OR gate as shown in Figure. 7a. In order to perform addition of numbers with more than 1-bit, parallel adders like RCA structure are designed using reversible full adder (RFA). Figure 7a and 7b shows the reversible full adder and Reversible RCA. The propagation delay in RCA is very high but by using the RHA and RFA the delay is getting reduced and power consumed by the reversible logic gates are very less because of switching of inputs, when compare to the logic gates.

Approach III: Reversible Kogge Stone Adder using RHA and RFA

Because of the complexity O (log2N) delay along the carry route compared to other adders, the parallel-prefix tree adders are more desirable in terms of size. The literature therefore considers that the Kogge-stone adder is the fastest adder in comparison with other additions. The adder choice in terms of worst-case delay is seen by Ripple-Carry, Carry-Look-Ahead, Carry-Select, and Kogge-Stone which are few famous parallel prefix adders. This is related to the "Reduced number of Stages". The implementation of KSA is very simple and uncomplicated structure and among all the other carries tree adders and it has the shortest critical path. Due to that there is a decrease in delay to generate the carry. But it consume larger area and routing of interconnects will be a complex one, which both are the disadvantage of KSA. Hence KSA is used for fastest arithmetic functions which are popularly used in DSP, Control Systems etc.

The RHA and RFA which has the ability to reduce the power which discussed in the above approach II, so the adder circuit of KSA is redesigned by using this to achieve the low power and high speed outputs

when compare to other tree adders.

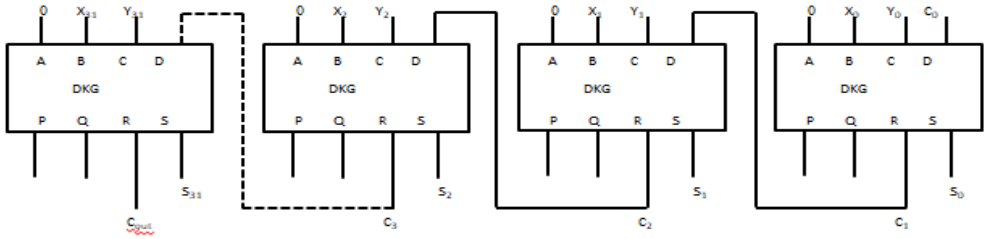

Figure. 5. 32-bit Reversible RCA using DKG.

4. Proposed Multiplier Architecture using the Reversible Adder

DSP operations such as convolution, discrete transformation wavelet, Fast-Fourier transformation and filtration, etc., the multipliers are the basic building blocks. The device speed is determined by the computation time of the multiplication operation. The Vedic approach for multiplication is one of the best places for the faster operation, by removing the unnecessary steps in the process of multiplication. Efficient adders should be chosen when designing the multipliers so that the multipliers have less delay and becomes power efficient. Similarly, the binary numbers multiplication problem should be resolved using similar methods to improve the consistency of the current aphorism with modern systems.

4. 1 Vedic Urdhva Tiryakbhayam Multiplier

Vedic math is an ancient mathematics have the sutra (aphorisms), including arithmetic, algebra, geometry, and so many mathematic functions. The term 'Vedic' comes from the term 'Veda' which is the house of power and divinity. [29,30]. The Vedic multiplier suggested is based on sutra (algorithm), "Urdhava Triyakbhayam." These Sutras were traditionally used in the decimal number system to subtract two numbers. *Urdhava Triyakbhayam (UT) Sutra* means “Vertically and Crosswise”. Shifting operation is not required in UT, as partial product measurement is carried out in one stage, saving time and power in turn. The Vedic multiplier has this huge benefit which is shown in Figure. 8[31]. A 32-bit UT multiplier is design with three methods, in all designs the RCA was replaced by the proposed reversible adders as shown in Figure. 8

4. 2 Baugh Wooley Multiplier

If the signed n * n multiplication is done, if the output has a bit width equal to the inputs then there won’t be any difference in the design. The effective algorithm in the multiplier to deal with this situation is BWM. In order to design structured multipliers suitable for the 2 supplementary numbers [30], this design method was established. By extracting the last two positive terms from the first two positives, it will generate the final output product. Instantly, the two can be applied to the last two words and adding both terms to deliver the final result instead of subtracting as normal multipliers.

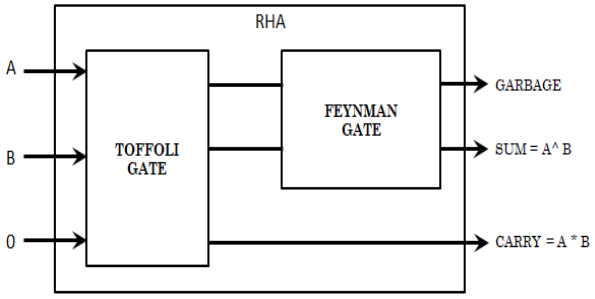

Figure.6. Proposed Reversible Half Adder (RHA) using Toffoli

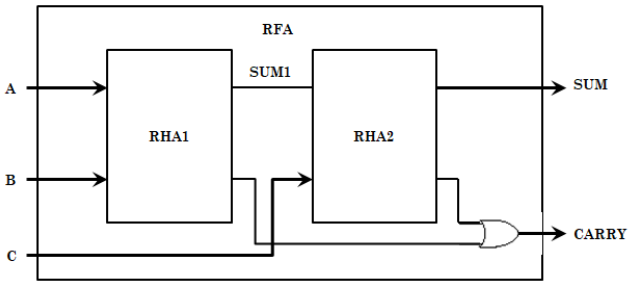

Figure. 7a. Proposed Reversible Full Adder (RFA) using RHA

Reversible BWM:

The BW multiplier is the efficient to handle signed bit. The 2’s complement number can be easily handled by the BWM. In the paper [33], the reversible multiplier is designed using Reversible TSG gate as a full adder and FRG gate for the AND gate and compared the

delay and power. Likewise, the reversible logic gates are utilized to design the Baugh Wooley Multiplier and analyzed the power and delay with the existing Baugh Wooley Multiplier. The following Figure. 9 shows the block diagram of 32*32 BMW. In this Baugh-Wooley, there are two different blocks, one is grey block and other is white box. These two boxes the grey and white implementation which is implemented using proposed RFA and RHA (i.e. method II) as shown in Figure. 9.

Similarly, the RCA in the last stage of BWM is replaced by the proposed Adders from Method I to method III as shown in the Figure. 9. The power and delay is calculated for the each and every method and the result is shown in the below table 1.

4. 3 Wallace Tree Multiplier

Another high speed multiplier is the Wallace Tree Multiplier, and which consumes less power among all the other tree multipliers. There are two structures in the Wallace tree multiplier which are conventional multiplier and reduced complexity multiplier, here conventional multiplier is considering for the design. An assortment of number-crunching procedures has been introduced to plan compelling multiplier. Probably the best strategy is the Wallace tree method as shown in Figure.10. This approach allows efficient equipment containing full and half-adder circuits to be generated in three phases that similarly influence the rise in operation. The Wallace-based duplicating activity incorporates three phases [34] as follows

Satge 1: Multiply each multiplier (or better express AND) bit, and produce n2partial products by each multiplier bit.

Satge 2: Lower the number of PP with the Full and Half Adder block layers.

Satge 3: Two n-sets have been added to an n-bit adder from the previous step.

Similarly, the Adders (HA &FA), conventional Adder of the Wallace tree multiplier shown in Figure. 10 is replaced with DKG reversible gate which is described in the method 1, secondly it has been designed using the method 2 which is RFA, RHA and Reversible RCA and finally the last stage of the Wallace tree multiplier is designed and implemented using the proposed RKSA. The Power and Delay of all the three methods have been calculated using the Xilinx Tool. The Result is compared with the existing method in which is given in the paper [24].

5. RESULT ANALYSIS AND SYNTHESIS

The implementations of the proposed methods are designed using Verilog HDL. The comparison of delay and power of 32 * 32 of the proposed multipliers and reversible array multiplier using Xilinx ISE tool with the Virtex 5 device is shown in table 1. The reversible multiplier architectures are designed and implemented using Xilinx ISE tool to calculate the delay. Xpower analyze tool is used to calculate the power.

6. CONCLUSION

In this paper, the reversible multiplier architectures based on different techniques like Vedic mathematics, Baugh Wooley and Wallace tree methods are designed, simulated and analyzed. The reversible multipliers are extensively used to build higher order multipliers, DSP applications and complex circuits like quantum computers. The performance of the different multiplier structures are evaluated by measuring the parameters like delay and power. In terms of delay, Vedic Multiplier with Proposed RKSA has recorded the best performance with lowest delay and lowest power consumption. Wallace tree architectures based on RHA and RFA as well as DKG based design has also produced best results in terms of delay and power consumption. The proposed multiplier structures are implemented in hardware using Xilinx Virtex 5. As a future work, the area requirements, number of gates, garbage outputs for each of the reversible multiplier structure will be computed and the results are analyzed.

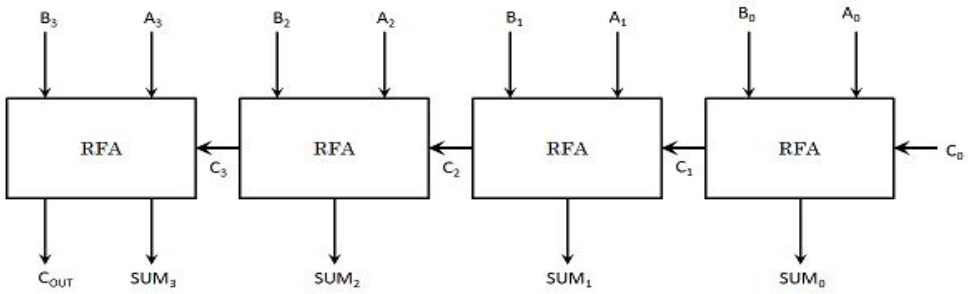

Figure.7b. Proposed Reversible RCA using proposed RFA

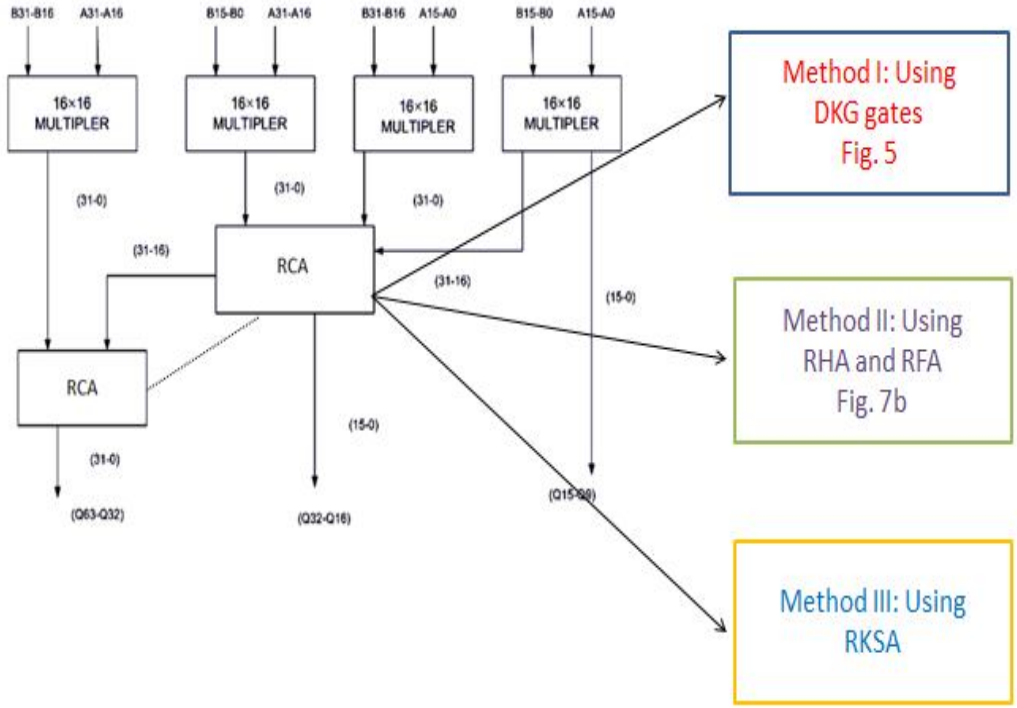

Figure. 8. 32- bit Urdhva Tiryakbhayam Sutra

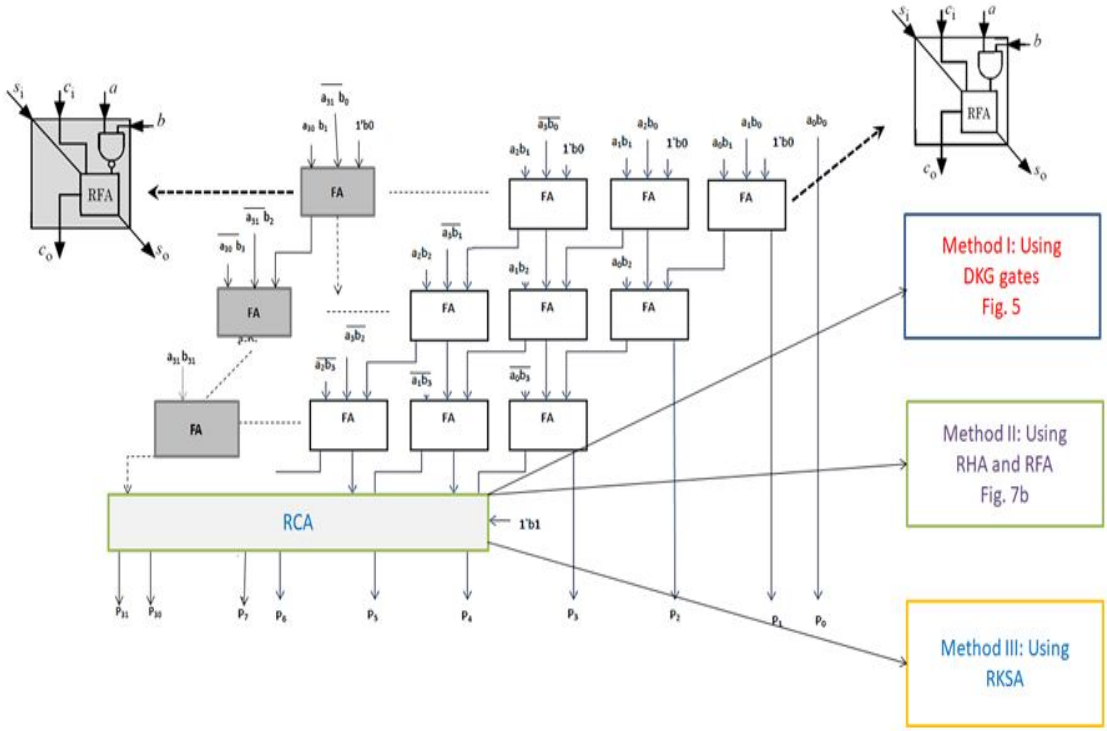

Figure. 9. Block diagram of 32 * 32 BWM with proposed methods.

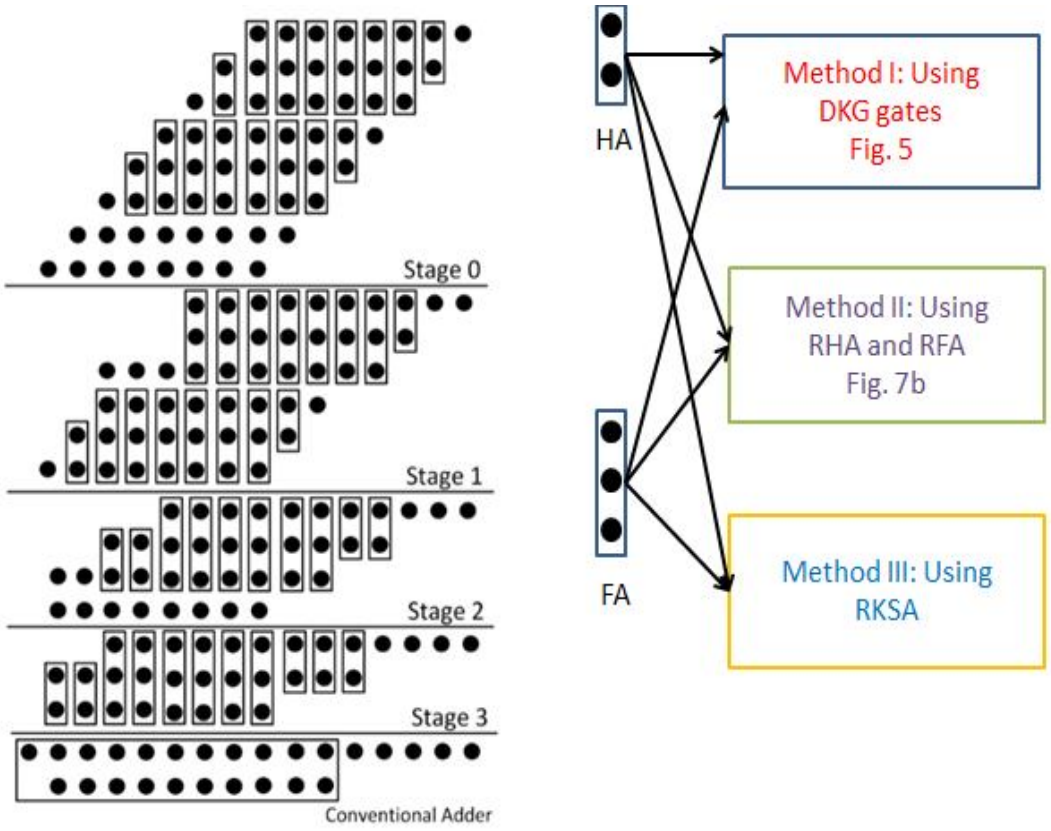

Figure. 10. Conventional Wallace Tree Multiplier.

Table 1: Comparison of Performance metrics of existing and proposed Designs

Design	Delay (ns)	Power (mW)
Vedic Multiplier UT [29]	35.76	166
Vedic Multiplier with DKG method 1	11.870	189.402
Vedic Multiplier with Proposed RHA and RFA method 2	8.161	182.37
Vedic Multiplier with Proposed RKSA method 3	7.770	170
Baugh Wooley with RCA [40]	63.79	195.574
Baugh Wooley with proposed reversible logic 1(DKG)	54.626	228.012
Baugh Wooley with proposed reversible logic 2 (proposed RHA and RFA)	16.825	188.210
Proposed Baugh Wooley Multiplier with Reversible KSA	11.863	171.019
Wallace Tree Multiplier with proposed reversible logic method 2 (proposed RHA and RFA)	9.421	168.23
Wallace Tree with reversible logic proposed method 1 (DKG)	10.761	170.815
Wallace Tree with reversible logic with RKSA	10.294	196.016
Wallace tree multiplier [24]	15.876	182.911

FUTURE SCOPE

The Vedic methods are efficient in reducing the delay and the power also. So the Vedic sutra can be implemented in several other multipliers and so many arithmetic operations to make the digital system very efficient. And in similar way reversible logic also plays a vital role in reducing the power. Several other designs of adders can be designed using reversible logic to get a better performance in different parameters.

ACKNOWLEDGEMENT

We acknowledge the support of Department of Micro and Nano Electronics, School of Electronics Engineering, Vellore Institute of Technology, Vellore.

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