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Design of Wallace Tree Encoder for Flash ADC

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ABSTRACT

Analog to digital converter plays a very important role in today's digitized world as they have wide range of applications. Wallace tree encoder is an effective hardware implementation in VLSI circuits that is utilized for the analogue to digital conversion process. The Wallace tree encoder transforms thermometer code into binary code in an ADC. The suggested flash digital to analogue converter confirmed the energy, and speed. The proposed technique provides Less Delay, Less Power Consumption, and a lesser number of transistors compared to existing techniques. In this project, the proposed transmission gate full adder technique provide Less Delay, Less Power Consumption, Better Power Delay Product and a lesser number of transistors. The proposed encoder is made to count the 1s available to the logic gates for designing ROM encoders and fat tree conversion. The power may be conserved by building a low power, high performance Wallace tree encoder implementing transmission gate logic and modified full adders since Wallace tree encoder uses more power. The proposed system focuses at lowering the transistor count to improve power efficiency and delay comparator, and it is effective in minimizing the bubble errors. The Wallace tree encoder is designed by using transmission gate based full adder circuits. The proposed designs are designed and simulated using LTspice Tool with 45nm CMOS technology. The power consumption of the encoder circuit must be decreased in order to create a low power Flash ADC. The power consumption of this encoder changes noticeably when the internal full adder circuit is modified

Key words *:* ADC, CMOS, Wallace Tree Encoder, Full Adder,Transmission Gate, Low Power

1. INTRODUCTION

In analogue circuits speed, power dissipation and area are very important parameters of any VLSI based systems. Data conversion circuit plays an important role in high-rate data communications. The Analogue to Digital Converter (ADC) is an electrical integrated circuit that transforms analogue signals, such voltages, into binary form, which consists of 1s and 0s. Most ADCs accept voltage input in the range of 0 to 10 volts, -5 to 5 volts, etc., and provide digital output in the form of a binary integer in response.

The figure 1 depicts the basic model of flash adc.In the analogue to digital conversion procedure, a Wallace tree encoder is used to translate the thermometer's coding into binary[1]. As a resistor ladder, encoder, and comparator circuit, this can be referred to as a high-speed application and a flash kind of flash ADC. An analog-to-digital converter (ADC, A/D, or A-to-D) in electronics is a device that transforms analogue signals into digital ones, such as sounds picked up by a microphone. Usually, flash structures are present in high-speed converters[2-3]. A pattern called "Thermometer code" is produced in flash converters using comparators. An ongoing pattern of 1s and 0s is the thermometer code. We need to employ two input XOR gates since a traditional ROM encoder requires an input of one out of N codes. "Wallace Tree encoder" accepts the thermometer code as input directly, therefore these transformations are not necessary[4-5]. This paper proposes a low power Wallace tree encoder by modifying the basic components i.e. full adder circuit.

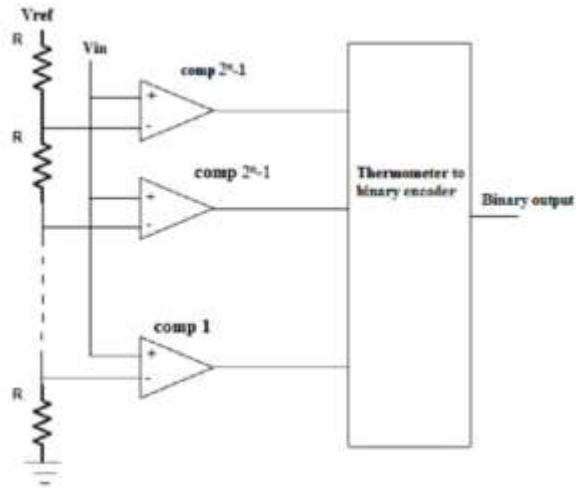

Figure 1 : Block Diagram of Flash ADC

An encoder is a necessary component of a Flash ADC. It converts the comparator output-generated thermometer code into binary code. Numerous encoders have already been created for flash ADC. A Wallace tree encoder adds the number of 1s produced by 2n - 1 comparators using complete adder circuitry[6-7]. Wallace Tree's in-built bubble error corrector circuit in the encoder is a key distinction between it and other systems[9-11]. The suggested design uses a hybrid full adder circuit because of this benefit, which improves its performance at high speed.

2. METHODLOGY AND PROPOSED CIRCUIT

2.1 EXISTING SYSTEM

The block diagram for 15:4 Wallace tree encoders is shown in Figure 2. Eleven complete adders with 15 thermometer code inputs and four b3, b2, b1, and b0-coded binary outputs make up this system. A Wallace tree encoder uses its inbuilt full adder circuits to count the number of "ones" in a data stream. The thermometer's "ones" series might have one or two "zeroes," which are known as bubble mistakes. In the current version of the Wallace tree encoder, each of the 15 inputs, i1 through i15, is channelled via an equal number of full adders. The existing encoder is made up with the use of conventional standard full adders.

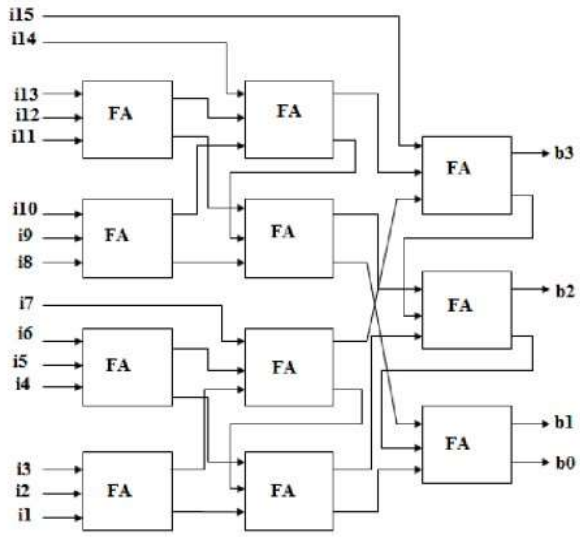

Figure 2: 4-bit Wallace Tree Encoder

As a result, the propagation delays between each input and the matching output are efficiently regulated and also equal. Therefore, the present design's speed of operation is respectably excellent. The conventional static CMOS structure is used to construct the 28 transistor traditional CMOS full adder. 14 NMOS pull-down and 14 PMOS pull-up transistors are used in the design and exhibit through figure 4. This design's primary benefit is its capacity generate full swing voltages. Due to the fact that sum realizes on this circuit, it causes undesirable delays. The conventional Full Adder circuit is shown in Figure 3. This design requires 28 transistors thus, the silicon area and the complexity are more for larger designs. The current circuit consumes more energy since a complete adder Wallace design tree encoder requires 308 transistors in total.

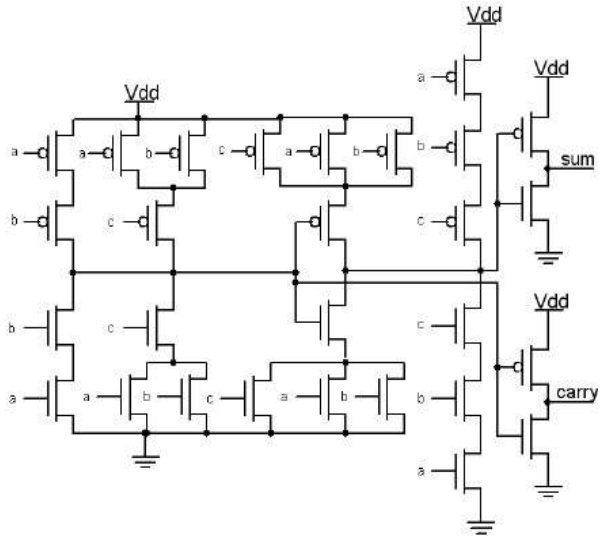

Figure 3: Conventional Full Adder with 28 Transistors

$$sum = (a \oplus b) \oplus c$$

$$carry = a.\ b + c.\ (a + b)$$

The figure 4 shows the modified full adder circuit with sum and carry. This design is used in Wallace Tree Encoder after

the conventional full Adder in figure 3 to improve the speed. The modified full adder have similar to the standard conventional full adder circuit with same number of transistors use. But the major difference is that this adder work effectively to give better delay and power consumption than the standard Full adder. In this modified full adder circuit the four transmission gates are used to improve the speed and delay.

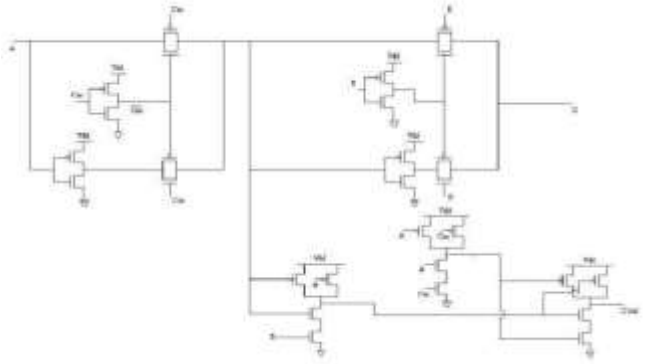

Figure 4: Modified Full Adder with 28 Transistors

2.2 PROPOSED SYSTEM

The main goal of the suggested study is to design a Wallace tree encoder that uses the least amount of energy, operates at less than ideal speed, and has the least amount of complexity for both old and current conversion processes. The Wallace tree encoder's energy consumption is reduced in the suggested design by the full adder's revised design is shown in the figure 5. The conventional CMOS full adder shows robustness against voltage scaling and transistor sizing. The disadvantages are high input capacitance and requirement of buffers. The power consumption of the encoder circuit must be decreased in order to create a low power Flash ADC. The power consumption of this encoder changes noticeably when the internal full adder circuit is modified. To overcame this disadvantages of existing system the transmission gate based full adders are designed. Figure 5 depicts the modified adder circuit.

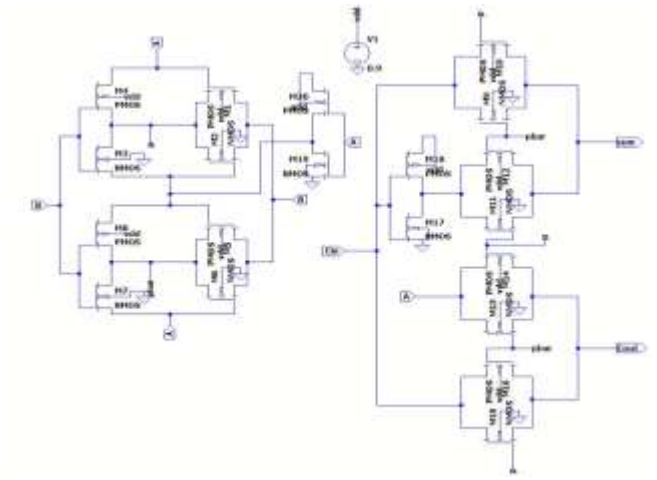

Figure 5: Modified Transmission Gate based Full Adder

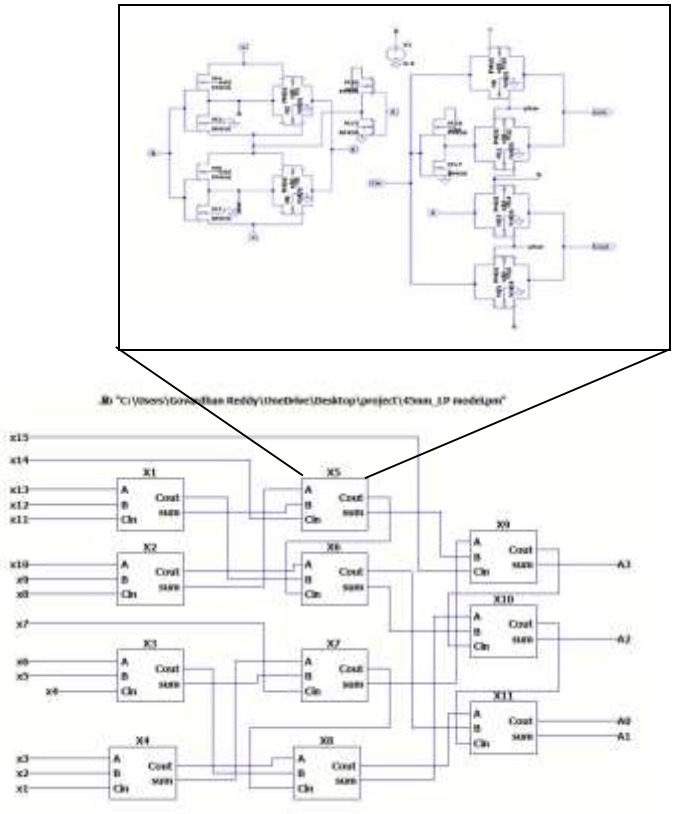

Figure 6: Proposed Wallace Tree Encoder with Modified Full Adder

The recommended complete adder is made up of n- and p-channel transistors with independent gate connections and shared source and drain connections. NMOS, PMOS, and transmission gates make up the circuit's 20 total transistors. High speed and minimal power dissipation are made possible by the employment of gearbox gates in the circuit. The main advantage of TG based full adder is lesser number of transistors. This advantage makes the circuit with faster speed, less area occupancy and less delay. The below figure 6 shows the proposed work with modified full adders

3. SIMULATION AND RESULTS

The proposed system is simulated in LTspice using 45-nm CMOS technology with 1-V supply. Simulated Transient Waveform shows through figure 7 and Time Delay conveys through figure 8.

Transient Waveform:

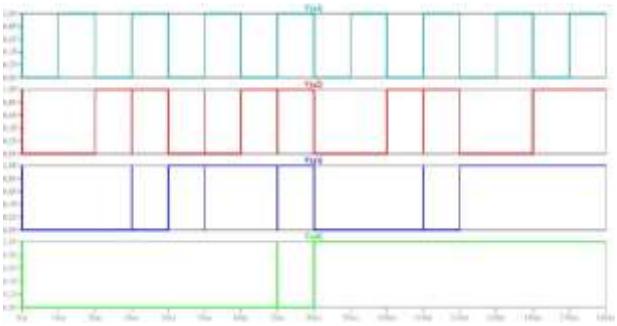

Figure 7: Simulated Transient waveform for proposed System

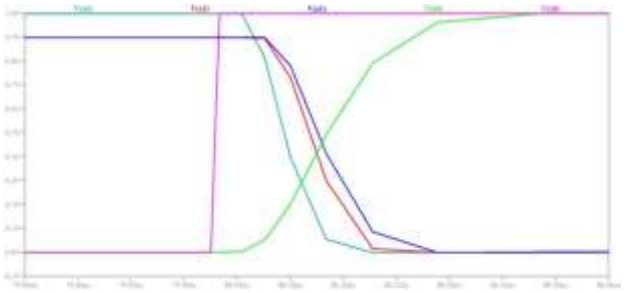

Figure 8: Time Delay

Table 1 conveys the Transistor Count, Delay, Power between Existing and Proposed Encoder.

Encoders	Transistor Count	Delay*(ns)*	Power(nw)
Existing Encoder	308	57.5	14.72
Proposed Encoder	220	0.1272	7.106

Table 1: Contrast between Existing and Proposed Encoder

4. CONCLUSION

The proposed work provides an efficient complete adder architecture that results in a Wallace Tree encoder with low power consumption, minimal complexity, and little latency.

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