



## Effect of High-K Dielectric materials on Mobility of Electrons

D Venkata Ratnam<sup>1\*</sup>, Rakesh Chowdary Gutta<sup>2</sup>, M. Ravi Kumar<sup>3</sup>, L. Eswara Rao<sup>4</sup>, M. V. Siva Surya Reddy<sup>5</sup>, P. Sai Pavan<sup>6</sup>, Chella Santhosh<sup>7</sup>

Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Green Fields, Vaddeswaram, Vijayawada-522502, AP, India.

### ABSTRACT

MOSFET is easier to manufacture than BJT and uses less processing power. To follow the law of the MOORE, in this paper we have adopt the principle of replacing SiO<sub>2</sub> dielectric with high-k materials, but it produces some effects. Here we define the problem of mobility. The mobility degradation is due to Coulombic and Phonon scattering. Improvement considerations for the degradation of mobility were also based. This paper offers information on the mobility using different dielectrics.

**Key words:** Dielectric, Electons, Photon, Channel, Mobility

### 1. INTRODUCTION

Scaling become an important factor in industries over the past three decades. It has provided both a denser and faster process of integration. Today's transistors are very faster and require less area when compared to earlier. According to Moore's law, count of transistors in a chip has grown exponentially in the past twenty years. The performance improves as the channel length is increasing, the energy required for switching decreases, and of improved density. There has been a rise in number of circuits per chip, power density and power consumption of a chip. Need for more performance and more transistor count on a chip has improved scaling methods in nearly all device factors. Those device factors are decreasing leakage currents, size of the channel etc.

Many high-k dielectrics have shown promising results after the research by various groups [1,2]. Nevertheless, there was many challenges still hindered the implementation of those successful candidates. The major challenges is reduced mobility of channels compared with their counterpart. The reasons behind the decreasing in mobility have not yet been explained [2]. From the study of channel mobility dependence on fields and temperature in HfO<sub>2</sub> and ZrO<sub>2</sub> -gated nMOSFETs, we acquired clear proof for the scattering mechanism.

Due to tunneling, leakage currents increase exponentially as the thickness scales down 2 nm, resulting in high power consumption and decreased performance of the system. As the SiO<sub>2</sub> is needed to be replaced with some other dielectric having high dielectric constant, we have several oxides such

as HfO<sub>2</sub>, ZrO<sub>2</sub> and various lanthanides. Instead of SiO<sub>2</sub> the aim of using high dielectric oxides is to build more dense and faster devices. The device's speed depends on source to drain current, depending on carrier mobility. In terms of drain current, effective mobility is defined in the linear region as:

$$I_d = \mu_n \frac{W}{L} [(V_{GS} - V_{th})V_{DS} - V_{DS}^2/2] \quad (1)$$

The degradation of effective mobility is major problems with the combination of high-k / and metal gate. Devices with SiO<sub>2</sub> as gate oxide the electrical field and concentration of doping used up to 300 cm / V-s. This value is below the mobility given by high K oxides. Active mobility is easily predicted to be decreased by high dielectric directly in contact with Si. Due to the roughness of the surface over the distance, flexibility is limited.

### 2.CHANNEL MOBILITY

To research the mechanisms of scattering it is important for accurately measure the channel mobility. Here, we achieved the effective channel mobility from the I<sub>d</sub>, from the following formula in the linear region [4]:

$$\mu_{eff} = \frac{L}{w} \cdot \frac{I_d(V_g)}{V_d Q_{inv}} \cdot \frac{1}{V_g} \quad (2)$$

The inverse charge density is obtained by calculating the  $\overline{C_{gc}}$  as a function of  $\overline{V_g}$ , using split-capacitance-voltage (C-V) technique and integrating it [5].

$$Q_{inv} = \int_{-\infty}^{V_g} C_{gc}(V_g) dV_g \mu_j \quad (3)$$

### Mobility Degradation

Degradation of mobility in MOSFET is the major drawbacks of using high dielectric constant materials as a gate oxide instead of SiO<sub>2</sub>. There are certain growing mechanisms in charge carriers mobility. Such specifics about the device's internal mechanisms that need to be examined and monitored only after careful observation. There are some solutions that can remedy the flexibility limitation that is addressed at the end of this article. Zhu's observations indicated that electrons mobility and holes mobility depends on the effective field applied to the gate and Silicon surface[6]-[7]. Under Matthiessen's law, the individual components of flexibility incorporate,

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_c} + \frac{1}{\mu_{ps}} + \frac{1}{\mu_{sr}} \quad (4)$$

Where  $\mu_c$  defines coulombic scattering mobility  
 $\mu_{ps}$  defines phonon scattering mobility  
 $\mu_{sr}$  defines surface roughness mobility

Different factors in different electrical fields decrease the mobility, as each complies with a different power law with field. Coulombic scattering (C) limits mobility in low fields by trapped charges. In medium and high fields it is limited by phonon and surface scattering respectively.

**Coulomb scattering**

Coulomb scattering is the major mechanism in decreasing the mobility at low fields of high dielectric gated MOSFETs due to trapped charges. That's why the energy distribution of the interface traps is asymmetrical. The interface trap density near the edge of the conductive band is lower than that near the edge of the valence as seen by the n-MOSFET's greater sub-threshold swing relative to p-MOSFETs. Therefore, the reduction in p-MOSFET hole mobility is usually less lethal than the reduction in n-type MOSFET electron mobility [8]. Under the presence of electric field, electrostatic forces on electro causes coulombic scattering.

**Phonon scattering**

Coulomb scattering caused by trapped charges and oxide charge, soft optical phonon scattering cannot be ignored [8]. The mobility limited in HfO<sub>2</sub> gated MOSFETs is lower than SiO<sub>2</sub> gate oxides, as shown in the figure [8]. MOSFETs with very high oxides like HfO<sub>2</sub> is an extra source of phonon scattering.

**3.SIMULATION RESULTS**

Here, we are referring to Zhu, W's journal [6]. We implemented the effect of high dielectric constant gate on mobility of charge carriers using Silvaco ATLAS method. Here we are observing the simulation result of channel mobility for HfO<sub>2</sub>, ZrO<sub>2</sub> and SiO<sub>2</sub>. Here we mostly observe HfO<sub>2</sub> (Atlas) and ZrO<sub>2</sub> (Atlas) scattering graphs only. HfO<sub>2</sub> (Zhu's) and SiO<sub>2</sub> (Zhu's) are for reference purpose.

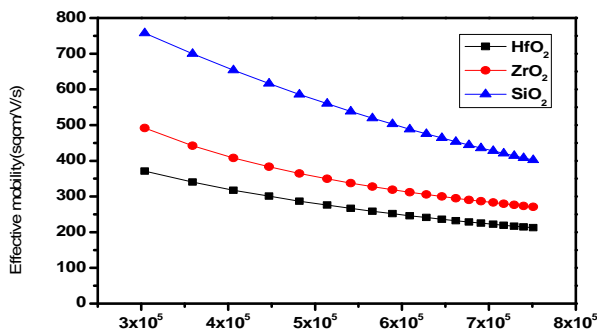


Figure 1: Effective mobility for different dielectrics at 2nm thickness

Figure 1 shows the effective mobility of electrons for various dielectrics (HfO<sub>2</sub>, ZrO<sub>2</sub> and SiO<sub>2</sub>) at 2nm oxide thickness. At 2nm thickness the effective mobility of electrons is high for SiO<sub>2</sub> when compared with other high dielectric constant materials. At the same time rate change of mobility is also high for SiO<sub>2</sub>.

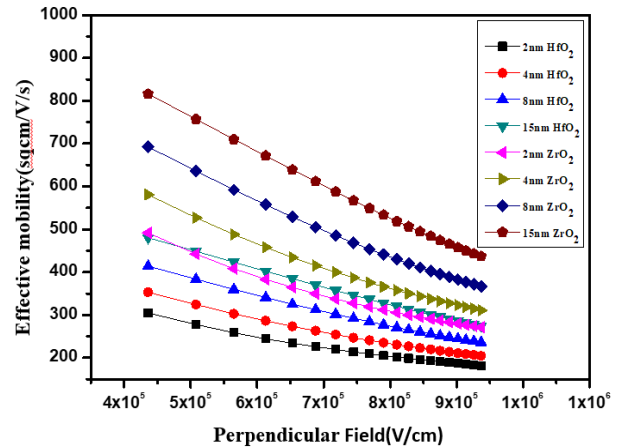


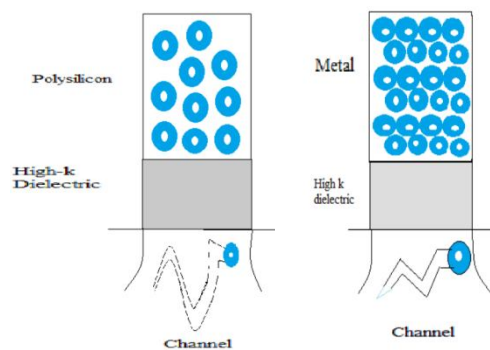
Figure 2: Effective mobility for different dielectrics at different thickness

Figure 2 shows the effective mobility of electrons for various dielectrics (HfO<sub>2</sub>, and ZrO<sub>2</sub>) at different oxide thickness (2nm, 4nm, 8nm,15nm).It is clearly observed that if the thickness of oxide increases then the effective mobility also increases.so one of the way to increase mobility in the case of high dielectric constant is to increase the oxide thickness. Figure 2 clearly shows that by increasing the thickness of the high dielectric constant materials oxide layer effective mobility increases. But alone increasing in thickness along does increase the mobility equal to SiO<sub>2</sub>. Along with this adding some more techniques will increase its mobility.

**Methods to improve mobility**

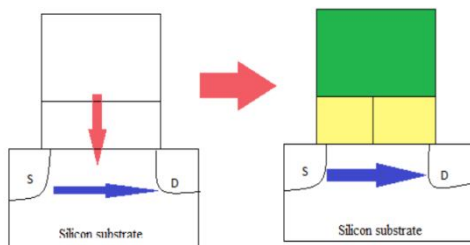
Mobility degradation can be solved by using metal gate in place of poly silicon gate. The poly-silicon substrate conductivity is low and the load accumulation is low due to this low conductivity, resulting in delays in channel creation and therefore unnecessary circuit delays. The polysilicon layer is doped with impurity of P or N type to act it as a conductor and to minimize the delay. poly-silicon doped with P or N type is a semiconductor and thus, when voltage is applied, will form a "depletion" region.

This "depletion area" reduces the inversion by acting like a thick oxide. But there is an decrease in the drive current. Metal gate have more free carrier density, which helps to monitor the weak phonon modes from high dielectric constant materials. The metal gate helps to screen the remote phonon scattering dipole coupling. This reduces the phonon dispersion and reduces the problem of mobility degradation.



**Figure 3:** Device with high-k dielectric and metal gate

Through large concentration of electrons in the gate, the effect of dipole vibrations on the channel electrons can be significantly reduced. Figure shows how to boost flexibility by placing metal gate in place of poly silicon gate. High-K oxides with metal gate are therefore more mobile than with poly silicon gate.



#### 4.CONCLUSION

Here we discussed, the effect of high dielectric constant oxides on charge carriers mobility, accurate measurements, and reduction of mobility of charge carriers with  $\text{HfO}_2$  and  $\text{ZrO}_2$  at different thicknesses. Some mobility degradation mechanisms were also focused. Coulomb scattering is a major cause for decreasing in channel mobility due to trapped charges. Soft optical phonons also contribute to the degradation of mobility as well. Remedies have also been discussed for the escalation of mobility values. We finally concluded that increasing the thickness of the high dielectric constant materials oxide layer effective mobility increases.

#### REFERENCES

[1] WILK, G. D., WALLACE, R. M. AND ANTHONY, J.M. High- gate dielectrics: current status and materials properties considerations. *Journal of Applied Physics*. 2001, vol. 89, iss. 10, pp. 5243–5275. ISSN:0021-8979.DOI: <https://doi.org/10.1063/1.1361065>.  
 [2] GUSEV, E. P., et al., Ultrathin high-gate stacks for advanced CMOS devices. International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224) 2001, pp. 451–454. ISBN: 0-7803-7050-3. DOI: 10.1109/IEDM.2001.979537.

[3] FISCHETTI, M., NEUMAYER, D., and CARTTIER, E. Effective electron mobility in Si inversion layers in MOS systems with a high-insulator: the role of remote phonon scattering, *Journal of Applied Physics*. 2001. vol. 90, pp. 4587–4608. ISSN:0021-8979.DOI: 10.1109/IEDM.2001.979537  
 [4] SUN S.G., and PLUMMER, J. D. Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces. *IEEE Transactions on Electron Devices*. 1980, vol. 27, iss. 8, pp. 1497-1508. ISSN 0018-9383. DOI: 10.1109/T-ED.1980.20063.  
 [5] SODINI, C. G., EKSTEDT, T. W., and MOLL, J. L. Charge accumulation and mobility in thin dielectric MOS transistors, *Solid-State Electron*. 1982, vol. 25, iss. 9, pp. 833–841. ISSN 0038-1101. DOI: [https://doi.org/10.1016/0038-1101\(82\)90170-8](https://doi.org/10.1016/0038-1101(82)90170-8)  
 [6] ZHU, W., HAN, J.P., and MA, T. P. Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-k dielectrics. *IEEE Transactions on Electron Devices*. 2004, vol. 51, iss. 1, pp. 98-105. ISSN 0018-9383. DOI: 10.1109/TED.2003.821384  
 [7] FISCHETTI, M. V., NEUMAYER, D. A., and CARTIER, E. A. Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-k insulator: The role of remote phonon scattering. *Journal of Applied Physics*. 2001, vol.90, iss.9, 4587. ISSN 0021-8979. DOI: <https://doi.org/10.1063/1.1405826>  
 [8] PANCHOLI, A., TYAGI, D. and KUMAR A. Simulation of High-K Dielectric Gate Effect on Carrier Mobility Using SILVACO TCAD, *Journal of Basic and Applied Engineering Research*, 2015, vol. 2, iss.22, pp. 1950-1953. ISSN 2350-0077.  
 [9] Chella Santhosh, K. Hari Kishore, G. Pavani Lakshmi, G.Kushwanth, P. Rama Krishna Dharma Teja, R. S. Ernest Ravindran, Sree Vardhan Cheerla, M. Ravi Kumar, Detection of Heavy Metal Ions using Star-Shaped Microfluidic Channel, *International Journal of Emerging Trends in Engineering Research*, 2019, Vol. 7, No.12, pp. 768-771.  
 [10] M Siva Kumar, Syed Inthiyaz, M Aditya, P Rupanjani, B Aravind, M Mukesh, Sanath Kumar Tulasi, Implementation of GDI Logic for Power Efficient SRAM Cell with Dynamic Threshold Voltage Levels, *International Journal of Emerging Trends in Engineering Research*, 7(12), December 2019, 902 – 906.