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Grid-connected photovoltaic systems synchronization algorithms under disturbances: a low-cost hardware implementation using Arduino DUE

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ABSTRACT

In grid-connected renewable systems, synchronization with the utility grid is the most important matter. Generally, the PLL is the most commonly adopted. This paper presents a performant analysis and comparison of the popular synchronization algorithms under grid normal and abnormal conditions based on several simulations in MATLAB software. It has been proved that the best output performance is resulted by the Dual Second Order Generalized Integrator PLL. This latter was developed and implemented to Arduino DUE as a low-cost real time implementation based on real hardware components. The setup provided in this work could make the operation of grid-connected renewable (particularly photovoltaic) systems practicable in terms of cost and good performance.

Key words: Renewable sources, Synchronization, Phase Locked Loop, Arduino DUE, Real-time implementation.

1. INTRODUCTION

Grid-connected PV systems currently dominate the photovoltaic market, particularly in Europe, Japan, and the United States. Grid-connected PV systems have not been widely developed in Morocco due to safety, economic, and especially technical obstacles.

The voltage generated by solar energy sources cannot be fed directly into the low-voltage distribution network, as it is a direct voltage. To overcome this obstacle, the frequency of the fed-in voltage has to be adapted, so-called synchronized. In order to achieve this, a three-phase inverter is used. The success of the conversions carried out by the inverter is dependent on the correct switching of this equipment. The switches are controlled by the signals from a digital signal processor, which, in order to produce correct control signals, must obtain continuous information about the photovoltaic generator output and grid voltages. The phase of the three-phase voltages is considered as the most important and critical information for the correct operating of photovoltaic systems connected to the low-voltage network. To obtain the phase angle, generally, the phase locked loop technique (PLL) is used [1].

Several published studies show different synchronization techniques used in grid-connected PV systems in order to provide the three-phase grid voltages information (phase and frequency), but these researches are based only on simulations using software such as MATLAB/Simulink which make their implementations in electronics platforms and devices such as dSPACE (Digital Signal Processing and Control Engineering), DSP (Digital Signal Processing), FPGA (Field-Programmable Gate Array) [2], [3].. much easier, however, these devices are expensive. This makes the installation of PV systems connected to the grid very cumbersome in terms of price.

Among the popular synchronization techniques due to their simple structure and performance, we can cite: the Synchronous Reference Frame PLL using Park transformation (dqPLL) [4], the Positive Sequence Detector PLL (PSD+dqPLL) [5], the Dual Second Order Generalized Integrator PLL (DSOGI-PLL) [6], the Decoupled Double Synchronous Reference Frame PLL (DDSRF-PLL) [7], etc. All these synchronization methods give satisfactory results in normal conditions with no noise neither disturbances in grid voltages. But for real-time situations, several factors in the distribution grid occur and can cause the appearance of harmonics, voltage unbalances, and frequency change. As observed in Figure 1, the fundamental PLL block diagram consists of (1) a phase detector (PD), (2) a loop filter (LF), and (3) a phase angle generator (PG) (also called a voltage-controlled oscillator VCO).

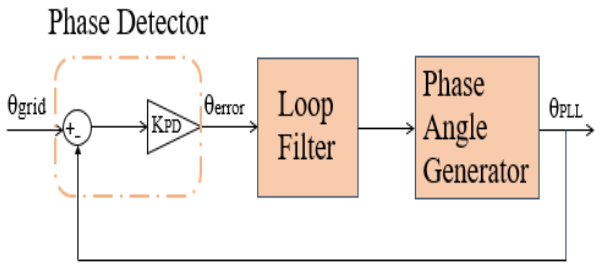


Figure 1: Phase Locked Loop block diagram

It must be pointed out that many up to date papers resume several synchronization algorithms [8], [9], although they lack of experimental results applicable for grid-connected systems using low-cost real hardware components.

Therefore, the main objective of this article is to present the most popular PLL algorithms, by providing a detailed explanation of their operations to help the engineers and the scientific community to have more information about their advantages and disadvantages, as well as a general idea for determining the technique to be used according to the grid type powered by the renewable energy source. To validate and compare the performance of the sub mentioned synchronization algorithms, MATLAB software was used. Then a real time digital implementation was developed, of the synchronization technique that has given satisfactory results, using Arduino DUE as a low-cost method with prominent and performance results to be used in connected PV projects operation.

In the Section 2, we will present an analysis of popular synchronization algorithms existing in the literature, by discussing their structures and operating concept. In Section 3, several simulations using MATLAB tool will be developed in order to evaluate the synchronization methods behaviors when disturbances occurred in the utility grid voltages, three-phase grid voltages with a peak value equal to 311.12 V. In Section 4, a real time digital implementation of the DSOGI-PLL will be performed using Arduino DUE development board with voltage sensors, several I/O, and power supply as a low-cost and performant prototype in order to strengthen the validity of the DSOGI-PLL in extracting grid phase to ensure a suitable integration. Finally, conclusions are given in Section 5.

2. SYNCHRONIZATION TECHNIQUES

2.1 Synchronous Reference Frame Phase Locked Loop (SRF-PLL)

By analyzing the different synchronization algorithms that exist in the literature, we can notice that the synchronous reference frame PLL, also called dqPLL is the simplest one. Its structure is diagramed in Figure 2 [10]. It is considered to be the core of the advanced algorithms at the final phse to generate the phase and frequency. It consists of Park and Clarke transformations [4] (abc to dq transformation) as presented in (1) and (2), the PI controller [11], and the integrator. Its inputs are the three-phase utility grid voltages (v_a, v_b, v_c), and as output, the dqPLL generates the calculated phase angle (θ_{PLL}). To identify the phase angle, the quadrature component v_q is fed to the PI controller and tuned to make it zero, then, v_d gives the amplitude of the positive sequence component of the input voltages. The phase angle is obtained after integrating the estimated angular frequency ω, this angle is used as a feedback for the Park transformation.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_o \end{bmatrix} = \frac{2}{3} \times \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \times \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_{PLL}) & \sin(\theta_{PLL}) \\ -\sin(\theta_{PLL}) & \cos(\theta_{PLL}) \end{bmatrix} \times \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (2)$$

Using the dqPLL model, we can obtain the linear second-order transfer function as expressed in (3), and comparing it with the canonical second-order transfer function presented in (4), the proportional K_p and integral K_i terms can be obtained.

$$H_\theta(s) = \frac{LF(s)}{s+LF(s)} = \frac{k_p s + k_i}{s^2 + k_p s + k_i} \quad (3)$$

$$H_\theta(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (4)$$

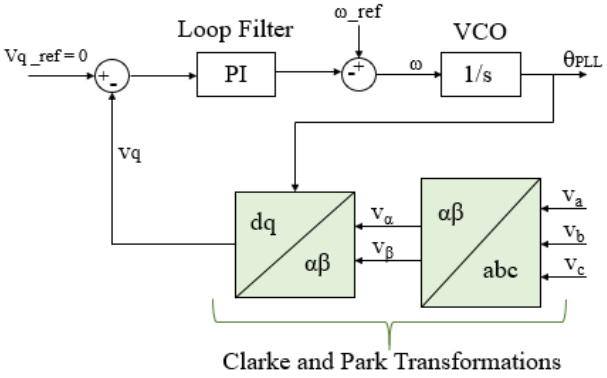


Figure 2: dqPLL structure

The dqPLL can be considered as the easiest technique to be implemented using different electronic devices; in addition, a reasonable performance of the dqPLL is noted when a negligible frequency change occurs in the voltages of the three-phase grid. But its sensibility to voltage unbalances and harmonic distortions is considered high. This method could be used with a stiff grid, where unbalances and harmonics are almost negligible [12].

2.2 Positive Sequence Detector Phase Locked Loop (PSD-PLL)

In order to overcome the limits of the dqPLL, a block of a Positive Sequence Detector (PSD) [5] is added, this latter is based on Fortescue theorem (or the symmetrical component method) [13], used to extract the voltages positive sequences.

Equations (5), (6) and (7) give the formulas to calculate positive sequence components [14].

$$v_a^+(t) = \frac{1}{3}v_a(t) - \frac{1}{6}\left(v_b(t) + v_c(t)\right) - \frac{1}{2\sqrt{3}}\,S_{90}\left(v_b(t) - v_c(t)\right) \quad (5)$$

$$v_b^+(t) = -\left(v_a^+(t) + v_c^+(t)\right) \quad (6)$$

$$v_c^+(t) = \frac{1}{3}v_c(t) - \frac{1}{6}\left(v_a(t) + v_b(t)\right) - \frac{1}{2\sqrt{3}}\,S_{90}\left(v_a(t) - v_b(t)\right) \quad (7)$$

Where S_{90} is a discrete filter, it can be expressed by the expression in the following formula [14].

$$H_{S90}(s) = \frac{1 - \frac{s}{\omega_{cut}}}{1 + \frac{s}{\omega_{cut}}} \quad (8)$$

By adding the PSD block to the dqPLL structure presented previously, we obtain the overall structure of the PSD-PLL shown in Figure 3. This approach could be considered as a good solution for ensuring a reliable integration/synchronization of solar energy sources to the utility grid. But if we observe the transfer function of the discrete filter, we can note that it has been expressed using a non-adaptive nominal angular frequency, which makes its operation very sensitive to the grid frequency variation, leading to power factor degradation of the grid-connected inverter.

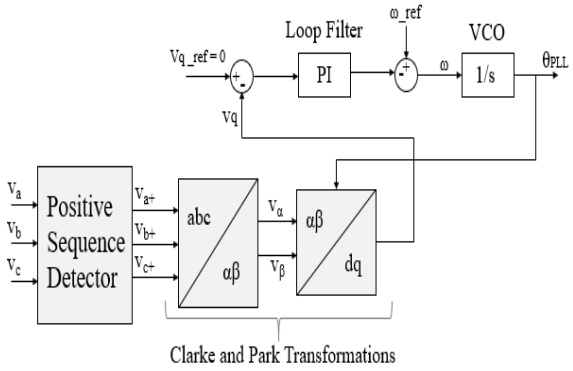


Figure 3: PSD-PLL structure

2.3 Decoupled Double Synchronous Reference Frame Phase Locked Loop (DDSRF-PLL)

Contrary to the dqPLL and the PSD-PLL, the DDSRF-PLL handle simultaneously both of the grid voltage sequences in order to estimate the two sequences of the grid voltages (positive and negative) [7]. Figure 5 shows the structure of the DDSRF-PLL, it has two rotating reference frames (positive and negative) that are rotating at the fundamental grid angular frequency. The positive rotating reference frame d_q+ rotates in the positive direction with the positive angular speed ω and its phase angle is θ_{PLL}, while the negative rotating reference frame d_q-, rotates with the negative angular speed -ω and its phase angle is $-\theta_{PLL}$. Therefore, the DDSRF-PLL separates the positive and negative components of unbalanced voltages as shown by its structure. The expression of the voltages after the conversion is presented by (9) and (10).

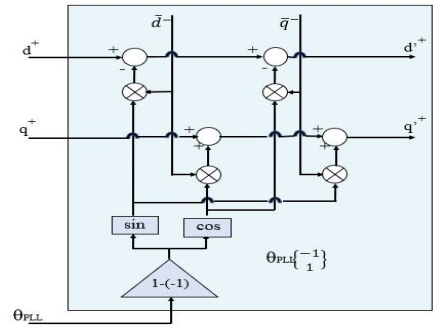


Figure 4: Decoupling network block diagram

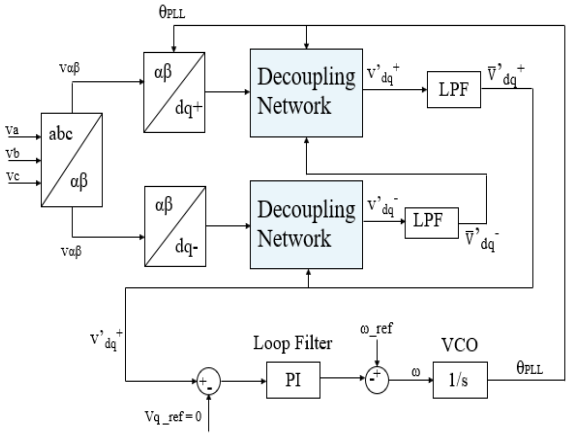


Figure 5: DDSRF-PLL structure

$$v_{\bar{d}\bar{q}}^{+1} = \begin{bmatrix} v_{\bar{d}}^{+1} \\ v_{\bar{q}}^{+1} \end{bmatrix} = \left[T_{\bar{d}\bar{q}}^{+1}\right] \cdot v_{\alpha\beta} \quad (9)$$

$$v_{\bar{d}\bar{q}}^{-1} = \begin{bmatrix} v_{\bar{d}}^{-1} \\ v_{\bar{q}}^{-1} \end{bmatrix} = \left[T_{\bar{d}\bar{q}}^{-1}\right] \cdot v_{\alpha\beta} \quad (10)$$

Where:

$$\left[T_{\bar{d}\bar{q}}^{+1}\right] = \left[T_{\bar{d}\bar{q}}^{-1}\right]^T = \begin{bmatrix} \cos(\theta_{dsrf}) & \sin(\theta_{dsrf}) \\ -\sin(\theta_{dsrf}) & \cos(\theta_{dsrf}) \end{bmatrix}$$

2.4 Dual Second Order Generalized Integrator Phase Locked Loop (DSOGI-PLL)

Another method known as Dual Second Generalized Integrator Phase Locked Loop [12] is developed to overcome the problems caused by the voltage unbalances. In this, four main functional blocks are present: (1) Clark transformation, (2) Second Order Generalized Integrator – Quadrature Signal Generator (SOGI-QSG), (3) Positive Signal Detector (PSD), and (4) Synchronous Reference Frame-Phase Locked Loop (SRF-PLL). Its structure is given in Figure 6.

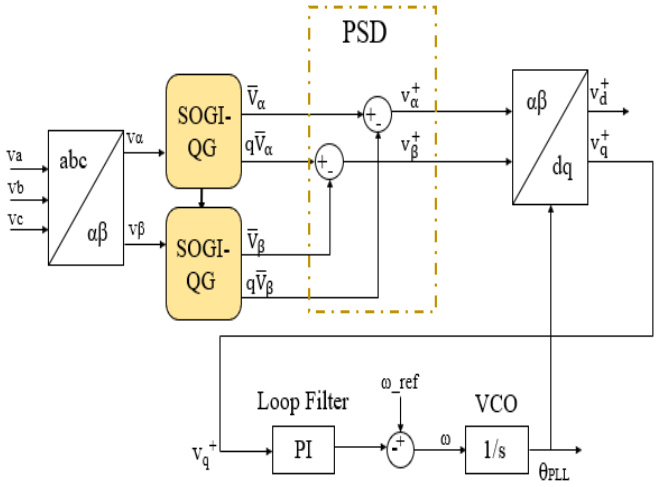


Figure 6: DSOGI-PLL structure

components are feeding to a PSD in order to calculate the positive sequence voltages. Finally, the positive sequences of the αβ components ($v_{\alpha\beta}+$) are used to estimate the frequency using the dqPLL block. The estimated frequency is referred back to the SOGI-QG block. The DSOGI-PLL could be a good choice when voltage unbalances occur.

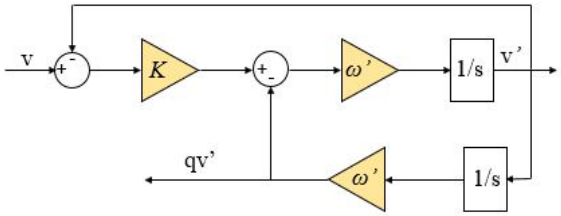
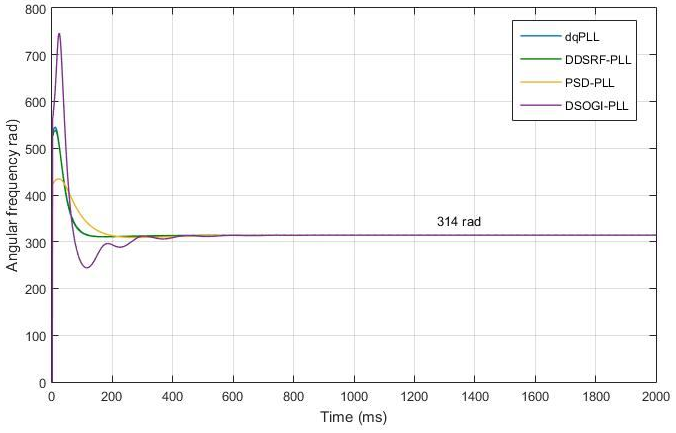
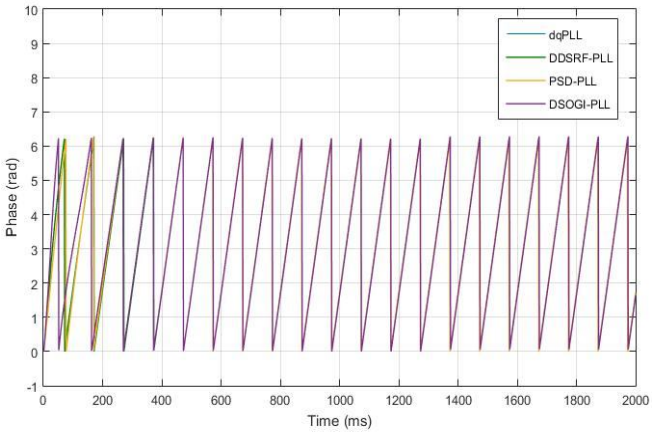


Figure 7: SOGI block diagram

Clarke transformation is used to calculate the αβ components, whereas an adaptive bandpass filter under the name of SOGI-QG [15], is used to provide the 90° shifted version of the αβ components, as shown in Figure 7. Then, the shifted αβ



(a)



(b)

Figure 8: Time evolution of the estimated **(a)** angular frequency and **(b)** phase angle, under normal conditions

3. SIMULATION RESULTS

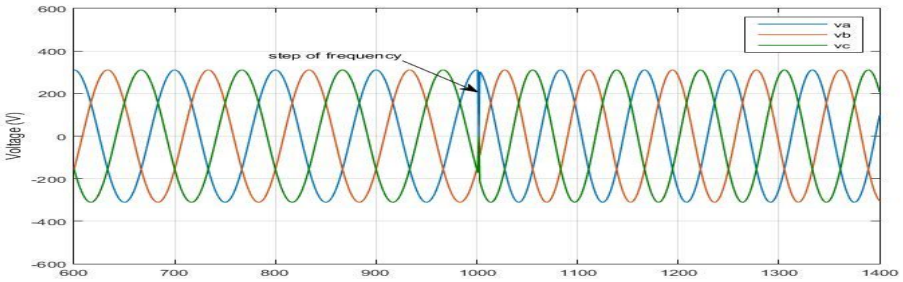
In order to evaluate the responses of the described synchronization algorithms, some simulations are performed using MATLAB C-files. The parameters of the grid voltages are: Nominal grid frequency = 50 Hz and Nominal voltage line to neutral = 311 Volt.

Figure 8 (a) and (b) present the behavior of the mentioned PLLs in normal conditions of the utility grid voltages, it can be clearly seen that almost all algorithms have shown their capabilities to estimate grid information (phase and angular frequency), by providing satisfactory results when it concerns a grid voltage free of noise and disturbances. Otherwise, Since the grid synchronization depends on grid parameters and operating conditions, the performance of the PLLs was tested under various grid disturbances.

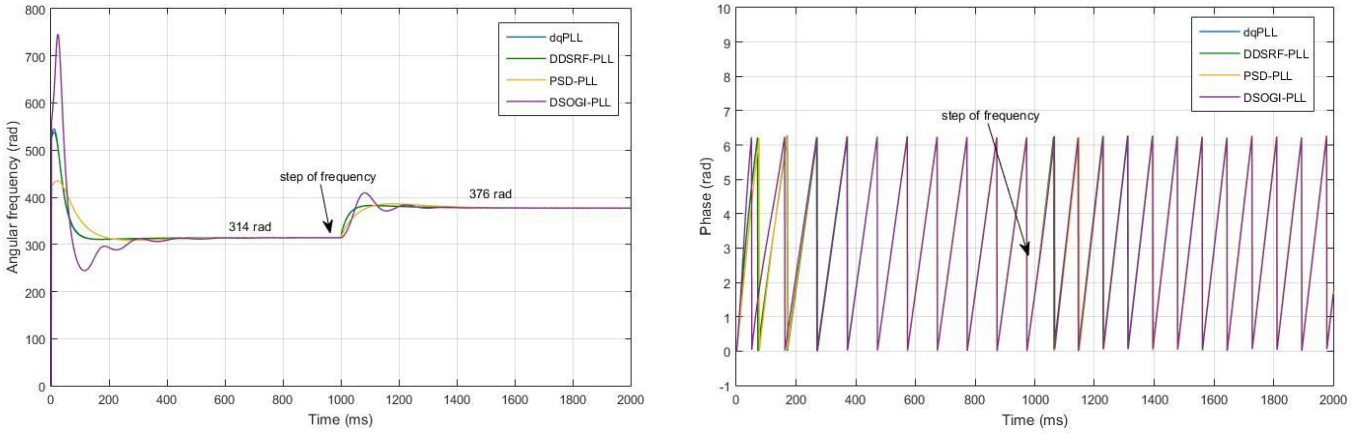
A. Influence test of the nominal frequency variation

The transient fault presence in the utility grid is the principal cause of the grid frequency variation. In this case, a change in frequency is exerted from 50Hz to 60Hz at 1 s. The peak values of the three-phase utility grid are V_{peak} = 311 V as given in Figure 9(a).

Figure 9 (b) shows the estimated phase angles and frequencies for each algorithm in real time evolution when a step change in grid nominal frequency occurs. The performance of the synchronization methods to track the frequency change could be clearly observed from the figures above, we can say that the frequency output is almost not influenced. It should be also noted that an overshoot is presented at the beginning of the disturbances using almost all the developed algorithms. SRF-PLL, PSD-PLL, and DDSRF-PLL had almost similar settling time, unlike DSOGI-PLL which needs more time to stabilize.



(a)

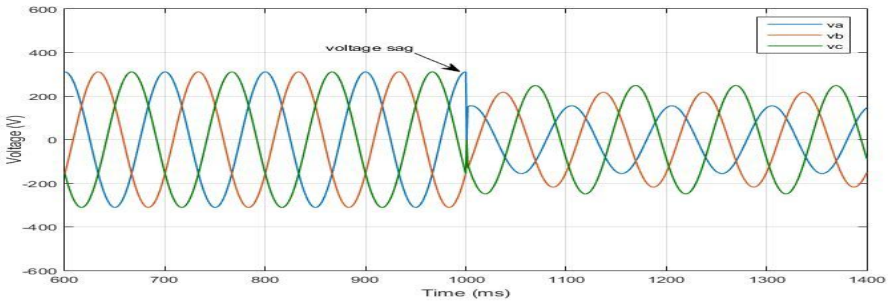


(b)

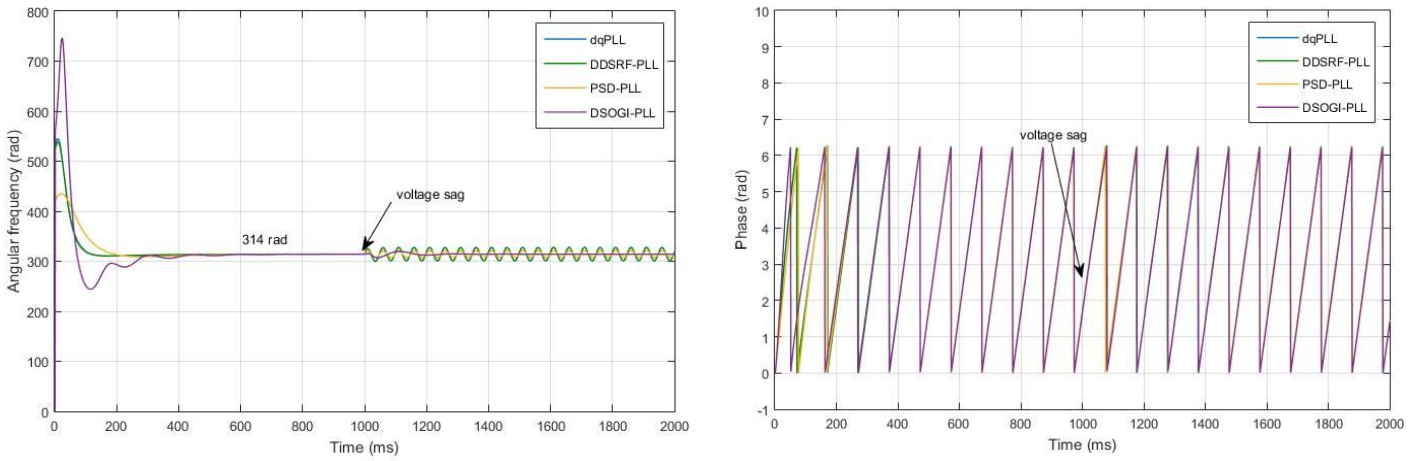
Figure 9: (a) Grid voltages during a step of frequency. **(b)** The estimated phase angle and frequency

B. Influence test of voltage unbalances

In order to analyze the response of the synchronization algorithms when voltage unbalances are introduced, the voltage profile for the simulation is proposed in Figure 10 (a). As shown in the figure, the magnitude of the grid voltages is 311 V at the initial time of simulation, then at 1s, different voltage sags were introduced to the grid voltages. The frequency/phase generated using the given algorithms are observed in Figure 10(b). When voltage unbalances occur in the utility grid, all algorithms have a good ability to estimate phase and frequency in steady state. Otherwise, at the moment when the voltage change occurs, DSOGI-PLL has a short transition period and settling time to stabilize and detect the grid information. While, SRF-PLL, PSD-PLL, and DDSRF-PLL present an undamped small oscillation during the voltage change duration.



(a)

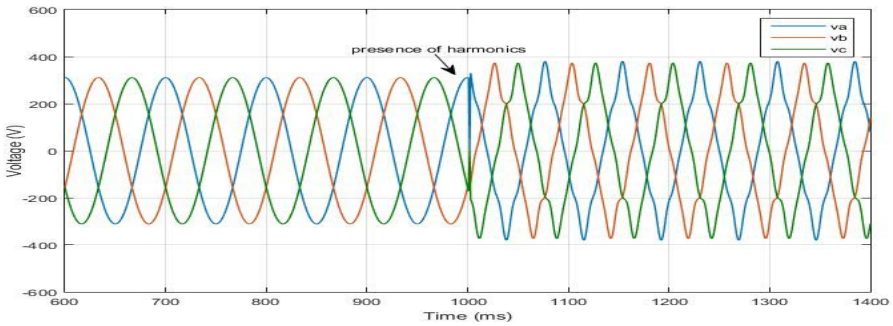


(b)

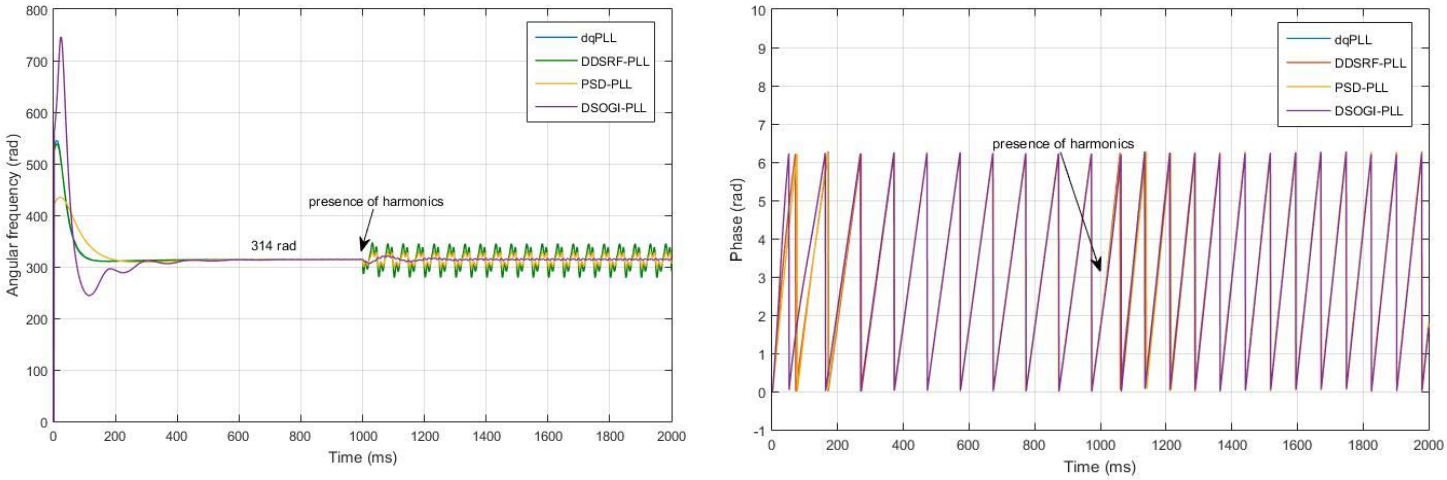
Figure 10: (a) Grid voltages when voltage unbalances occur. **(b)** The estimated phase angle and frequency

C.Influence test in the appearance of harmonics

The analysis of synchronization algorithms under harmonic distortions is described in this section. In this case, we have introduced the +5th order harmonic to the voltages of the three phases at 1 second, Figure 11(a) describes the voltages evolution in time for this case. The behavior of the PLLs under this condition is shown in Figure 11(b).



(a)



(b)

Figure 11: (a) Grid voltages when harmonics occur. **(b)** The estimated phase angle and frequency

Figure 11 (b) presents the detected frequency and phase by the different PLLs. On one hand, the test results show that dqPLL, DDSRF-PLL, and PSD-PLL have almost similar behaviors to detect grid phase and frequency. PSD-PLL has an undamped oscillation, with a small amplitude compared to dqPLL and DDSRF-PLL. On the other hand, the DSOGI-PLL has given good performances by rejecting disturbances.

4. EXPERIMENTAL SETUP

The simulation results presented in the previous section have shown that the DSOGI-PLL outperforms the presented synchronization algorithms by giving a high capacity to estimate and detect the frequency of the three-phase utility grid in normal and abnormal grid conditions. The reason, in this section, the DSOGI synchronization algorithm is designed and tested experimentally using the Arduino DUE board. To validate the developed DSOGI algorithm, the experimental setup presented in Figure 12 is used. It consists of three voltage sensors, Arduino DUE development board, balanced three-phase low voltages, and measurement devices.

Figure 12: Materiel used for the experimental setup

4.1 Arduino programming of the DSOGI-PLL

To evaluate the performance of the system studied, it is necessary to initially simulate it and then implement it on an appropriated platform that gives the possibility to verify that the results obtained are adequate to what is theoretically expected. For developing, coding, and testing the proposed algorithm, the Arduino DUE was adopted. To implement DSOGI-PLL, it is necessary to formalize it in a programming language known by Arduino DUE board, to guarantee so, it is necessary to obtain its mathematical model in discrete time. If we consider the diagram of the DSOGI-PLL, we can note that the important block in its structure is the SOGI, presented in Figure 7. The transfer function giving the mathematical model of the SOGI is presented by (11).

$$\frac{v'(s)}{v(s)} = \frac{K_{sogi}\omega' s}{s^2 + K_{sogi}\omega' s + \omega'^2} \quad (11)$$

K_{sogi} is the gain of the SOGI and ω' the grid frequency, in rad/s, estimated by the dqPLL.

To obtain a discretized model of the SOGI, the trapezoidal approximation, also called bilinear approximation or Tustin's method was used [16], which consists of replacing, in the continuous-time transfer function, the variable s, by the expression given in the following formula (T is the sampling period, in seconds).

$$s = \frac{2}{T}\frac{z-1}{z+1} \quad (12)$$

4.2 ZMPT101B sensor module

ZMPT101B voltage sensor module [17] is a voltage sensor made from the ZMPT101B voltage transformer. It can measure up to 250V AC with high accuracy and good consistency for voltage and power measurement. Its mode of operation is simple based on a potentiometer to adjust the ADC output. Figure 13 presents the ZMPT101B voltage sensor module [17].

Figure 13: ZMPT101B module

The three voltages of the utility grid, which, under ideal operating conditions, vary sinusoidally between -220√2 V and 220√2 V, were converted into three sinusoidal signals, with the same frequency, ranging from 0 to 3.3 V. This transformation was performed using three ZMPT101B voltage sensors. The sinusoids from 0 to 3.3 V serve as input for Arduino DUE. Thus, theoretically, when, at a certain point in time, the mains voltage is, for example, 0 V, the Arduino will see 1.6 V on the corresponding analog input.

4.3 Experimental results

The two analog output pins of DUE, DAC0 and DAC1, are supposed to provide voltages from 0 to 3.3 V. Since the Arduino DUE has only two output ports Analogue, only two output signals can be displayed in an oscilloscope at a time. Figure 14 provides the voltages generated by the three voltage sensors after the transformation to the range 0-3.3 V. From the measurements of average voltage, maximum voltage and frequency made by the oscilloscope, it can be clearly observed that they present what is exactly expected, an average voltage of 1.6 V, and a frequency of 50 Hz.

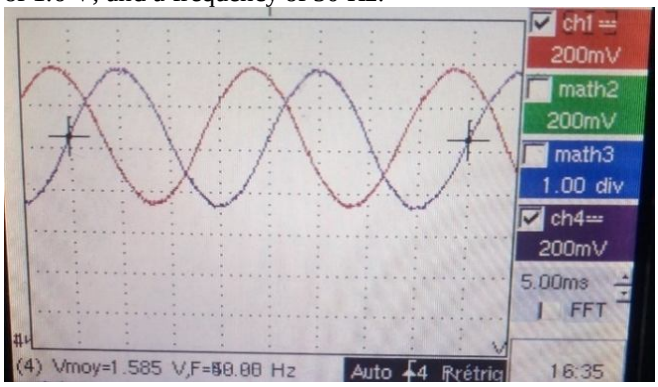


Figure 14: Two-phase voltages of v_α and v_β

Figure 15, presents the time evolution of the phase angle θ_{PLL} and the positive sequence component $v_\alpha+$, it is remarkable that the frequency of the two signals is approximately 50 Hz, as expected. It is also observable that the detected phase angle is synchronized with the $v_\alpha+$ voltage since the cycle of both signals starts and ends together. This proves that the phase angle calculated and generated by the proposed algorithm is adequate with the phase of the input voltage, therefore, the estimated frequency is equal to the grid frequency.

Figure 15: Time-evolution of $v_\alpha+$ and the detected phase angle

At this point, we can ensure that the synchronization with the grid has been done successfully. The obtained results experimentally correspond exactly to the results given by the simulations in the previous section.

4.4 Price comparison between Arduino DUE and the most used electronic devices

As mentioned previously in this paper, many published papers in the literature use DSP, DSPACE, or FPGA for the real-time implementation of synchronization algorithms, the model blocks of the algorithms are firstly built in MATLAB/SIMULINK and then, the C-code of the algorithms are generated with Real Time Workshop and downloaded into the mentioned platforms, which make the implementation simple and easy. But these platforms are quite expensive, Table 1 gives price comparison of the proposed overall experimental setup using the Arduino DUE and the other platforms.

Table 1: Cost comparison between DUE, DSPACE, DSP, and FPGA.

	Price	Experimental setup price
DUE	30 $	51 $
FPGA	150 $	171 $
DSP	400 $	421 $
DSPACE	7000 $	7021 $

5. CONCLUSION

The aim of this paper was to establish a powerful analysis where the advantages and limits of four popular synchronization algorithms are presented. After this analysis, it can be said that DSOGI-PLL outperforms the other algorithms and could be considered as the most reliable synchronization technique.

An important objective of this work was to develop and implement a performant algorithm of the DSOGI-PLL using a low-cost real time implementation based on Arduino DUE and real hardware components, that makes the operation of grid-connected photovoltaic systems practicable in terms of cost and good performance. The obtained experimental results of the proposed synchronization system have revealed its validity to guarantee the synchronization between the renewable energy source and the utility grid.

REFERENCES

1 I. Setiawan, M. Facta, A. Priyadi, and M. H. Purnomo, **Comparison of three popular PLL schemes under balanced and unbalanced grid voltage conditions**, *2016 8th International Conference on Information Technology and Electrical Engineering (ICITEE)*, 2016, pp. 1–6, doi: 10.1109/ICITEED.2016.7863282.

2 K.-J. Lee, J.-P. Lee, D. Shin, D.-W. Yoo, and H.-J. Kim, **A Novel Grid Synchronization PLL Method Based on Adaptive Low-Pass Notch Filter for Grid-Connected PCS**, *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 292–301, Jan. 2014, doi: 10.1109/TIE.2013.2245622.

3 Y. Yang, L. Hadjidemetriou, F. Blaabjerg, and E. Kyriakides, **Benchmarking of phase locked loop based synchronization techniques for grid-connected inverter systems**, *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015, pp. 2167–2174, doi: 10.1109/ICPE.2015.7168077.

4 R. H. Park, **Two-reaction theory of synchronous machines generalized method of analysis-part I**, *Transactions of the American Institute of Electrical Engineers*, vol. 48, no. 3, pp. 716–727, 1929.

5 P. Rodríguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre, and F. Blaabjerg, **New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions**, *2006 37th IEEE Power Electronics Specialists Conference*, 2006, pp. 1–7, doi: 10.1109/pesc.2006.1712059.

6 M. Gholami and G. Ardeshir, **Dual phase detector based on delay locked loop for high speed applications**, *International Journal of Engineering-Transactions A: Basics*, vol. 27, no. 4, pp. 517–522, 2014.

7 P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos, and D. Boroyevich, **Decoupled Double Synchronous Reference Frame PLL for Power Converters Control**, *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 584–592, Mar. 2007, doi: 10.1109/TPEL.2006.890000.

8 F. Filipović, B. Banković, M. Petronijević, N. Mitrović, and V. Kostić, **Benchmarking of Phase Lock Loop Based Synchronization Algorithms for Grid-Tied Inverter**, *Serbian Journal of Electrical Engineering*, vol. 16, no. 1, pp. 1–19, 2019.

9 S. Golestan, J. M. Guerrero, and J. C. Vasquez, **Three-Phase PLLs: A Review of Recent Advances**, *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017, doi: 10.1109/TPEL.2016.2565642.

10 A. SATIF, L. HLOU, N. HMINA, and R. ELGOURI, **Modeling and Simulation of a Photovoltaic System Connected to a Low-voltage Three-phase Utility Grid**. *International Conference on Industrial Engineering and Operations Management*, July 2018, pp. 2711-2719

11 O. M. Mohamed vall, **PI Controller Design for Networked Control Systems with Random Time Delay**, *International Journal of Emerging Trends in Engineering Research*, vol. 8, no. 1, pp. 114–118, January 2020, doi: 10.30534/ijeter/2020/15812020.

12 N. F. Guerrero-Rodríguez, A. B. Rey-Boué, A. Rigas, and V. Kleftakis, **Review of Synchronization Algorithms used in Grid-Connected Renewable Agents**, *REPQJ*, pp. 240–245, Apr. 2014, doi: 10.24084/repqj12.300.

13 C. L. Fortescue, **Method of Symmetrical Co-Ordinates Applied to the Solution of Polyphase Networks**, *Transactions of the American Institute of Electrical Engineers*, vol. XXXVII, no. 2, pp. 1027–1140, Jul. 1918, doi: 10.1109/T-AIEE.1918.4765570.

14 M. Karimi-Ghartemani and M. R. Iravani, **A method for synchronization of power electronic converters in polluted and variable-frequency environments**, *IEEE Transactions on Power Systems*, vol. 19, no. 3, pp. 1263–1270, Aug. 2004, doi: 10.1109/TPWRS.2004.831280.

15 Xiaoming Yuan, J. Allmeling, W. Merk, and H. Stemmler, **Stationary frame generalized integrators for current control of active power filters with zero steady state error for current harmonics of concern under unbalanced and distorted operation conditions**, in *Conference Record of the 2000 IEEE Industry Applications Conference. Thirty-Fifth IAS Annual Meeting and World Conference on Industrial Applications of Electrical Energy (Cat. No.00CH37129)*, 2000, vol. 4, pp. 2143–2150 vol.4, doi: 10.1109/IAS.2000.883122.

16 A. Tustin, **A method of analysing the behaviour of linear systems in terms of time series**, *Journal of the Institution of Electrical Engineers - Part IIA: Automatic Regulators and Servo Mechanisms*, vol. 94, no. 1, pp. 130–142, May 1947, doi: 10.1049/ji-2a.1947.0020.

17 "zmpt101b datasheet pdf, zmpt101b data sheet, zmpt101b.pdf, schematic, Datasheet4U.com." Available: https://datasheet4u.com/share_search.php?sWord=zmpt101b.