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Spin-Orbit-Torque Magnetic Tunnel Junction Transistor Based Area Efficient Low Power Non-Volatile Master-Slave Flip-Flop

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ABSTRACT

A Spin Orbit Torque (SOT) Magnetic-Tunnel-Junction (MTJ) transistor based area efficient F) is discussed in this paper. The modified NV-MSFF has consumed less area and less power consumption when compared to the existing NV-MSFF. Hence, the proposed NV-MSFF is more suitable for low power applications. The proposed NV-MSFF is designed and implemented as hybrid CMOS-Spintronics circuit using 45 nm CMOS process technology and Verilog-A model based MTJ-Transistor for Spintronics. The proposed NV-MSFF has been designed and simulated using Cadence Virtuoso-Analog-Design-Environment (ADE) with Spectre as the simulator and the simulation temperature as 27°C. The proposed NV-MSFF has 44% reduction in the area occupied. The overall energy requirement of the prevailing NV-MSFF is 1.961 µW whereas it is 194.2 nW only for modified NV-MSFF. The delay of the existing NV-MSFF is 1.175 ns whereas it is 383.3 ps only for the modified NV-MSFF. The proposed NV-MSFF outperforms in terms of area, power and the propagation time.

Key words: Low-Power, Magnetic-Tunnel-Junction (MTJ), Non-Volatile Master-Slave Flip-Flop (NV-MSFF), Spin-Orbit-Torque (SOT), Spintronics

1. INTRODUCTION

Electrical controlled Magnetic Tunnel Junction (MTJ) Transistors through spin-polarized current pulses provides greater opportunities to improve speed, power consumption, and device density in various applications such as memory devices [1]-[3], logic circuits [4] and RF oscillators [5]. Conventional two terminal MTJs are electrically controlled through spin transfer torques using spin-polarized technique [6]. Current-induced Spin–Orbit Torques (SOTs) have recently attracted greater attention for high-performance and low power spintronic applications [7]-[10]. An adaptive compact magnetic tunnel junction model and SOT-MTJ based CMOS-Spintronics hybrid NV-MSFF [11, 12] are intended for high performance low power computing and storage applications.

Recently, the Spin Orbit Torque (SOT) based no-volatile Static Random Access Memory (SRAM) circuits [13], [17] are gaining more popular due to its low power consumption and the non-volatile property. MTJ-based low power non-volatile flip-flops [14], [18] are being used in the latest high-performance System on Chip (SoC) applications [22], [23]. Spin Transfer Torque (STT) based multi-bit nonvolatile flip-flops [15], [19] are being used for non-volatile storage applications. Energy and area efficient SOT based Non-volatile flip flop for power-gating [16] are employed in the latest SoC applications. Energy and Reliability Trade Offs were considered in Low Voltage ReRAM based Non-Volatile Flip Flop [20] for the high performance low power circuits. In this paper, Verilog-A model based SOTMTJ is connected to 45 nm CMOS transistors to realize the proposed design as CMOS-Spintronics hybrid circuit. Section-II deals with the existing work. Section-III describes the modified work and the Section-IV explains about the simulation results and analysis. Conclusion has been presented in Section-V.

2. EXISTING NV-MSFF

The existing NV-MSFF [12] operates like conventional CMOS flip-flop, while in active-mode. Once the back mode signal has been enabled, the data is stored by the SOT-MTJ devices by flipping the directions. Once the supply voltage is enabled, the stored data has been restored and the flip flop works as a conventional flip flop. To backup the latched bit by storing the bit within the PMTJs before gating Vdd OFF, the B signal is asserted high and the C signal has been held low.

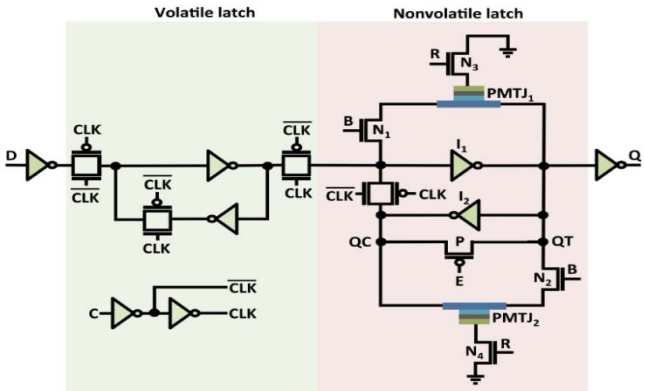

Figure 1: NVFF based on three terminal PMTJs based nonvolatile-slave-latch [12]

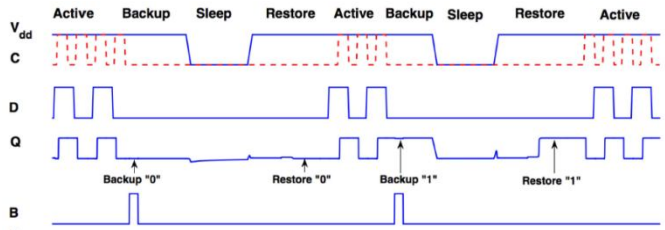

Figure 2: Input-Output Signals of the Existing NV-MSFF Signals [12]

Once the B signal has been kept high, a programming-current will through the channel of both PMTJs due to the voltage difference between QC and QT. When QC is high and QT is low, inverter I1 sources current and inverter I2 sinks current, changing the magnetization of the FL of PMTJ1 and PMTJ2 to, respectively, P and AP states. Figures 1 and 2 shows the NVFT based on three terminal PMTJ's based Non volatile Slave latch and Input-Output signals of existing NVMSFF [21].

3. PROPOSED NV-MSFF

The proposed Non-Volatile Master-Slave-Flip-Flop has been designed as CMOS-Spintronics hybrid circuit. The proposed NV-MSFF has been designed using very less number of transistors compared to the existing NV-MSFF. The proposed NV-MSFF has been designed and implemented using Hybrid CMOS-Spintronics. The proposed NV-MSFF has been designed and implemented using 11 CMOS devices and 2 SOT-MTJ devices whereas the existing NV-MSFF was implemented using 25 CMOS devices and 2 SOT-MTJ devices. CMOS devices were taken from 45 nm CMOS process library and the Spintronic device SOT-MTJ has been realized using Verilog-A model. The schematic diagram of the proposed low power NV-MSFF has been depicted in Figure 3.The proposed NV-MSFF works in two phases according to the status of the clock pulse. During positive clock cycle, the data is stored in the back-to-back connected inverters in the master side and during the negative clock-cycle; the data will be stored in the slave side latch when the flip-flop is operated in the normal mode.

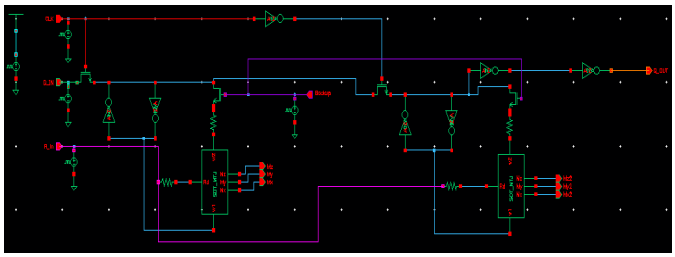

Figure 3: Schematic-Diagram of the modified low power NV-MSFF

Before the power supply is disabled, the "backup" signal has been activated to store the data present in the latch to SOT-MTJ device. Once the "backup" signal has been activated, the data present in the latch has been stored in SOT-MTJ which is a non-volatile storage element. Once the supply voltage resumes back, the data stored during the stand-by mode will be restored to the back-to-back connected inverter by initiating the "Read" signal. The proposed NV-MSFF circuit has been designed and implemented using hybrid CMOS-Spintronics devices with an improvement of 44 % in the occupied area.

4. SIMULATION RESULTS AND DISCUSSION

The proposed SOT-MTJ based low power NV-MSFF has been designed and implemented using hybrid CMOS-Spintronic devices. CMOS devices are taken from 45nm CMOS process library and the Spintronic device has been implemented using Verilog-A model. The simulations were carried out in Cadence Virtuoso-Analog-Design-Environment (ADE) with Spectre. The simulation-parameters are listed-out in the Table 1.

Table 1: Simulation Parameters

Items	Descriptions
CMOS Process	45 nm CMOS
Supply Voltage	500 mV
Spin Transistor	SOT-MTJ
EDA Tool	Cadence Virtuoso ADE
Simulator	Spectre
Simulation Temperature	27 °C

The input and output signals of the proposed NV-MSFF has been shown in Figure 4. The "Backup" signal plays the key role in the non-volatile storage operation. The "Backup" signal is enable before the supply voltage "V_{dd}" goes down. Once it is initiated, the data stored in the latch is stored in the SOT-MTJ devices in the Master and Slave sides. Once the supply voltage resumes, the "Restore" signal will be enabled to restore the data from the SOT-MTJ to the latch in both Master and Slave sides. After restoration process, the Master-Slave flip flop works as conventional flip flop. In the existing NV-MSFF, the non-volatile part was implemented using two SOT-MTJ devices in Slave whereas the non-volatile operation has been realized using one SOT-MTJ device both in the Master and Slave sides in the proposed NV-MSFF.

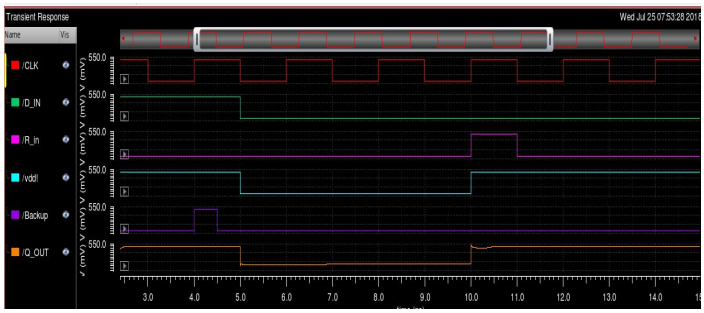

Figure 4: Input and Output Signals of the proposed low power NV-MSFF

The comparative analysis of the existing and the proposed NV-MSFF has been listed in Table. 2. The propagation delay of the existing NV-MSFF [12] is 1.175 ns whereas it is 383.3 ps only for modified NV-MSFF. The overall power requirement of the existing work is 1.961 µW whereas it is 194.2 nW only for the proposed design. The existing circuit was implemented using 25 CMOS transistors and 2 SOT-MTJ devices whereas the proposed NV-MSFF uses 14 CMOS and 2 SOT-MTJ devices. The occupied area improvement is 44% by the proposed technique.

Table 2: Comparative Analysis

Parameter	Existing NV-MSFF [12]	Proposed NV-MSFF
Delay	1.175 ns	383.3 ps
Power	1.961 µW	0.178 µW
Number of Transistors	CMOS = 25	CMOS = 14
	MTJ = 2	MTJ = 2

Table 3: Impact of Temperature on Total Power Consumption

Simulation Temperature (°C)	Total Power Consumption	
	Existing (µW)	Proposed (µW)
-25	3.376	0.164
0	4.592	0.172
25	5.811	0.177
50	7.046	0.182
75	8.281	0.186
100	9.516	0.190
125	10.772	0.193

The effect of operating temperature on overall power consumption of existing and the proposed NV-MSFF has been tabulated in Table 3. The effect of operating temperature on overall power consumption of existing and the proposed NV-MSFF has been plotted in Figure 5.

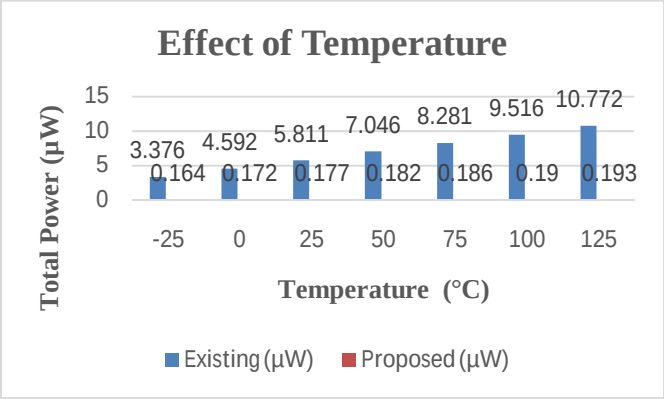

Figure 5: Effect of Temperature on Total Power Consumption

As the operating temperature increases the overall power requirement of the existing NV-MSFF upturns drastically whereas the impact of temperature is notably less on the overall power requirement of the proposed NV-MSFF.

5. CONCLUSION

Spin-Orbit-Torque-Magnetic-Tunnel-Junction (SOT-MTJ) transistor based area efficient low power Non-Volatile Master Slave Flip Flop (NV-MSFF) is discussed. The modified NV-MSFF has 44% reduction in the area occupied. The overall power requirement of the existing NV-MSFF is 1.961 µW whereas the it is 194.2 nW only for the modified NV-MSFF. The propagation-delay of the existing NV-MSFF is 1.175 ns whereas it is 383.3 ps for the proposed NV-MSFF. The proposed NV-MSFF outperforms in terms of overall power, number of transistors required to implement the design and the propagation delay.

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