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High-Performance Dynamic Comparator

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ABSTRACT

An essential approach to evaluate the performance of a dynamic comparator is proposed and simulated in different CMOS processes using the MENTOR GRAPHICS tool. The performance of the dynamic comparator is measured by using various parameters. Dynamic comparators with different configurations are simulated and compared in performance with power, delay and PDP. The dynamic comparator with less latency, low power and reduced PDP is identified and earmarks that particular comparator is best suited for high-frequency applications above 1 GHz.

Key words: Power, power delay product, delay dynamic comparator

1. INTRODUCTION

Comparators are vital building blocks in A/D converters. The accuracy and efficiency of the A/D converters depend on the performance of the comparator. A/D converters operate for converting an analog input signal to its equivalent digitized output.

In this process, A/D converters use a bank of comparators to compare the analog input with the reference signal. The comparators output are enclosed with an encoder to acquire the relevant digitized output. Comparators that are used in the A/D converters are capable to compare either two analog input signals or one analog input signal and a reference DC voltage [1], [2].

Many A/D converters are available in the market, of these, SAR A/D converters are highly accurate than other A/D converters. SAR A/D converters preferably use dynamic comparators for their conversion. Dynamic comparators are classified into various types based on their configuration like double tail, Elzaker, dynamic bias and calibrated comparator. Dynamic comparators constitute of two stages as preamplifier & latch.

In dynamic comparator, the preamplifier is in differential amplifier configuration to compare two inputs and amplify the differential output that is generated by comparing the two inputs [3]. The amplified differential output is stored in the latch stage. The amplified differential output that is stored in the latch is the required digital output. The operations like comparison and latch are controlled by using a clock signal.

The successive sections describe the operation and performance comparison of different dynamic comparators in two different modes of operation at a frequency of 1 GHz in terms of their characteristic parameters like power and PDP. The last section concludes the best high-performance dynamic comparator that suits for A/D conversion [3].

2. OPERATIONAL METHODOLOGY

The particular section presents the discussion on different operational modes of dynamic comparators and the variations in their characteristic performance parameters. A dynamic comparator has a preamplifier stage in which two analog inputs are applied to the two corresponding input terminals for comparison. The analog input that is supplied to the input terminals can be performed either by using a single analog voltage source or by using two analog voltage sources [4],[5]. The number of input sources determines the modes of operation are prescribed as common mode and differential mode respectively. Therefore, dynamic comparators perform their comparison operation in these two different modes.

Dynamic comparators like calibrated, double tail, Elzaker, and two-stage dynamic, comparator operations are compared with one another in terms of characteristic parameters like power, delay & PDP.

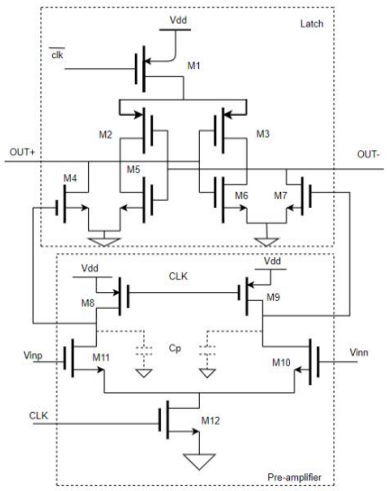

Figure 1: Double Tail Latch Dynamic Comparator

Figure1 depicts a double tail latch dynamic comparator that contains 2 stages, preamplifier and latch as the first stage & second stages respectively. The preamplifier is designed by using five MOS transistors with two PMOS and three NMOS transistors. From figure1 M8 and M9 are the PMOS transistors that are controlled by the clock signal. Likewise, M10, M11 and M12 are the NMOS transistors in the preamplifier. The analog inputs are applied across the NMOS transistors M10 and M11 to perform A/D conversion [3],[6]. The analog inputs across these transistors are applied in both common and differential mode. M12 is the tail transistor that is controlled by the clock signal which provides a discharge path to the ground.

The second stage or latch consists of seven MOS transistors with three PMOS and four NMOS transistors. PMOS transistors are M1, M2, & M3, whereas M4, M5, M6 & M7 are the NMOS transistors in the latch. M2, M5 and M3, M6 constitutes two inverters that are connected to form a latch with two supporting transistors M4 and M7. 'The output of one inverter is connected as an input of another inverter to form a bi-stable element'. Latch also contains one tail PMOS transistor that is controlled by clock bar to produce perfect logic high level at the output terminals. The perfect digital outputs are obtained across out+ and out- terminals respectively [7], [8].

Double tail dynamic comparator operates in both common and differential mode with a VDD=1.2V at 130nm process technology. Power and delay are evaluated by using transient analysis with the ELDO simulator. Power, Delay and PDP are derived from the simulation results for both modes of operation.

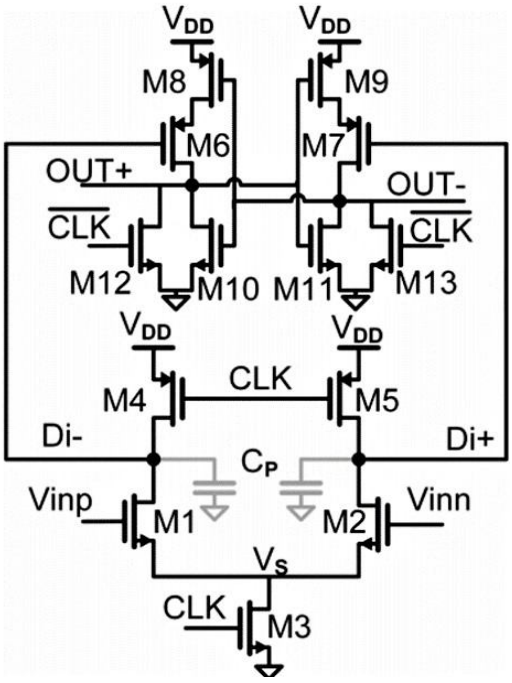

Figure 2: Elzaker Dynamic Comparator

A double tail latch dynamic comparator suffers from poor optimization of power, Therefore, to overcome this problem a modified version of the dynamic comparator is proposed in figure 2 presents a modified version of figure1 to perform A/D conversion. The preamplifier stage in Elzaker is identical to the preamplifier stage in the double-tail dynamic comparator. Elzaker comparator uses six transistors to design latch for A/D conversion whereas double tail dynamic comparator uses only five transistors [4],[5],[9].

The operation to perform A/D conversion in the Elzaker comparator is identical to the operation in a double tail latch dynamic comparator. Elzaker dynamic comparator has a tail transistor in the preamplifier stage only whereas a double tail dynamic comparator uses tail transistors in both preamplifiers & latch stages.

The absence of a tail transistor in Eslzaker dynamic comparator helps to prevent parallel operation of preamplifier & latch. Elzaker dynamic comparator helps to enhance the performance of the comparator by providing a delay for the latch when the preamplifier is in operation. It means that the preamplifier & latch do not operate at the same time. Delay is achieved by using separate transistors across the output nodes [9],[10],[11]. The latch comes into operation only if the two transistors M6 & M7 has inputs at logic '0'. The perfect digital outputs are obtained across out+ and out- terminals respectively.

Elzaker dynamic comparator operates in both common mode and differential mode with VDD=1.2V at 130nm process technology. Power and delay are evaluated by using

transient analysis with the ELDO simulator. Power, Delay and PDP are derived from the simulation results for both modes of operation.

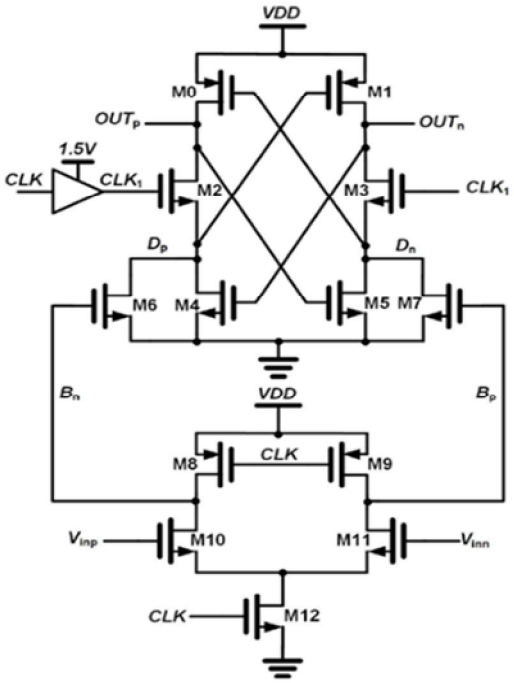

Figure 3: Two-Stage Dynamic Comparator

An altered version of a double tail dynamic comparator to overcome the problem of parallel operation for both the preamplifier stage and the latch stage is in figure3. The preamplifier stage of the two-stage comparator is identical to the double-tail comparator but the latch stage is complex compared with it. The complexity in the latch stage prevents the simultaneous operation of both the stages that decreases the power dissipation & increases in the delay to produce the final digital outputs in a typical A/D conversion [12],[13]

The latch stage contains a tristate buffer to provide a typical time delay for the operation of the latch stage. Tristate buffer is operated with a voltage greater than the supply voltage VDD. It operates with a voltage of 1.5V to provide the best logic levels across LOW and HIGH states. The delay of the two-stage dynamic comparator is diminished by decreasing the transconductance gm of the latch. Therefore, an optimized value of power, delay and PDP is obtained [14],[15].

Two-stage dynamic comparator operates in both common mode and differential mode with VDD=1.2V at 130nm process technology. Power and delay are assessed by using transient analysis with the ELDO simulator. Power, Delay and PDP are evaluated from the simulation results for both modes of operation.

A Calibrated dynamic comparator is in figure2 that contains three stages to perform A/D conversion. It incorporates an amplification stage, half latch & final latch for its operation. The major property of this calibrated comparator is that it can simultaneously reduce noise and delay. The dynamic comparator with calibration transistors is called a calibrated comparator. MSP & MSN are the two additional transistors that were connected to the preamplifier to attain calibration. In this calibrated comparator two more transistors are used at the nodes of XP & XN to provide stable amplification,[16].

The noise is reduced by providing a charge leakage path using the transistors MSP & MSN. The calibration performance is directly proportional to the size of the transistors MSP & MSN. The size of the transistors M1P & M1N is eight times larger than MSP & MSN to increase the performance of the comparator.

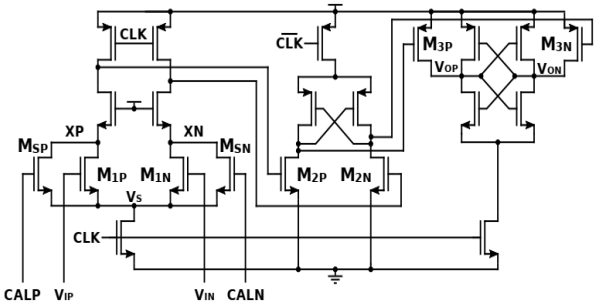

Figure 4: Calibrated Comparator

The calibrated comparator is operated in both common mode and differential mode with a VDD=1.2V at 130nm process technology. Power and delay are assessed by using transient analysis with the ELDO simulator. Power, Delay and PDP are derived from the simulation results for both modes of operation.

3. RESULTS & DISCUSSION

All the dynamic comparators presented in the earlier sections are simulated by using the ELDO simulator with transient analysis in 130nm CMOS by the MENTOR Graphics tool. From the simulation results, Power & delay are evaluated and compared with various types of dynamic comparators [17],[18]. The simulation results for the dynamic comparators are in figure5.

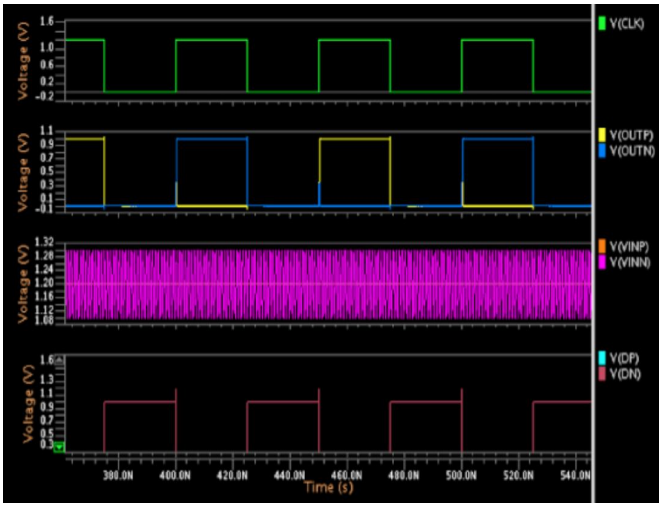

Figure 5: Simulation Result of Dynamic Comparators

All the comparators that were discussed here are simulated in both differential & common mode with separate input signals and a common input signal across the input terminals respectively. In differential mode, the two inputs terminals are applied with two different sinusoidal AC signals across VINP & VINN with equal magnitude and out of phase by 180^o [19],[20]. The amount of voltage applied to the input terminals will always be half of the sinusoidal magnitude value depending on the clock signal.

In common mode, a single sinusoidal AC signal is applied to both the input pins with the same magnitude and 180^o out of phase. Whenever an appropriate clock signal appears the two input terminals draw a full magnitude of voltage. Due to this reason, Dynamic Power dissipation increase compared with the differential mode of operation. As we know the dynamic power dissipation is

$$P_{DYNAMIC} = C_{L.} V_{DD}^2 . f \qquad (1)$$

Table 1: Comparative Analysis of Various Dynamic Comparators

Frequency = 1 GHz		Differential Mode			Common Mode		
S. No	**Dynamic Comparator**	**Power (uW)**	**Delay (ps)**	**PDP (fJ)**	**Power (uW)**	**Delay (ps)**	**PDP (fJ)**
1	Double tail	53.65	917.82	49.24	56.87	917.82	52.20
2	Calibrated	49.91	949.37	47.38	54.09	949.37	51.35
3	Two Stage	12.51	966.79	12.09	19.16	966.79	18.52
4	Elzakker	8.17	871.08	7.12	11.75	871.08	10.24

Equation (1) provides a relationship between dynamic power dissipation with load capacitance, supply voltage and frequency of operation. Therefore, dynamic power dissipated by the comparator in differential mode is less compared with the common mode of operation [21].

A comparative analysis of all various dynamic comparators is tabulated in the below table1 with different modes of operation and performance parameters like power, delay & PDP. The tabulated values are procured at f = 1GHz using the ELDO simulator with VDD=1.2V. The analog inputs are applied at VINP & VINN that are sinusoidal with the same magnitude and 180o out of phase to one another.

The final digital outputs are obtained at OUT+ & OUT- nodes in a typical dynamic comparator which performs A/D conversion [13], [14]. The conversion can be performed in 2 modes as differential mode & common mode. The characteristic parameters like power, delay & PDP are tabulated for various dynamic comparators and prove that the power and PDP are maxima in common mode compared with the differential mode of operation [18],[22].

The comparison of power with various dynamic comparators is in figure6. From figure6, dynamic power dissipation is maximum for double tail dynamic comparator and minimum is for Elzaker dynamic comparator.

For all the dynamic comparators the dynamic power dissipation in the differential mode of operation is less compared with the common mode of operation due to the utilization of voltage V_{DD} in both modes of operation while maintaining load capacitance C_L, frequency and temperature uniform at all intervals of time.[18],[22].

Figure7 describes the delay variations with various dynamic comparators and presents the delay is maximum for two-stage dynamic comparator due to utilization of buffer in the latch & delay is optimum for Elazker dynamic comparator.

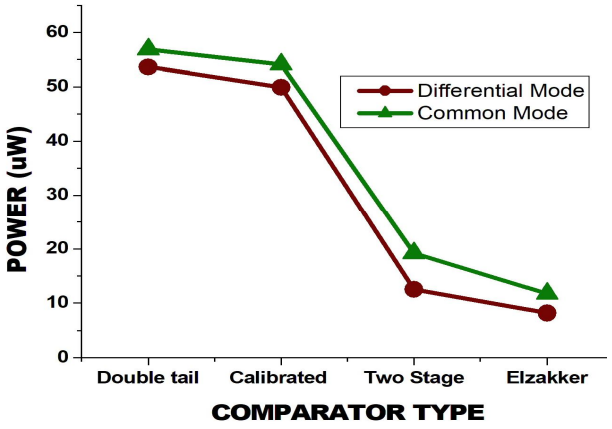

Figure 6: Comparison of power with Dynamic Comparators

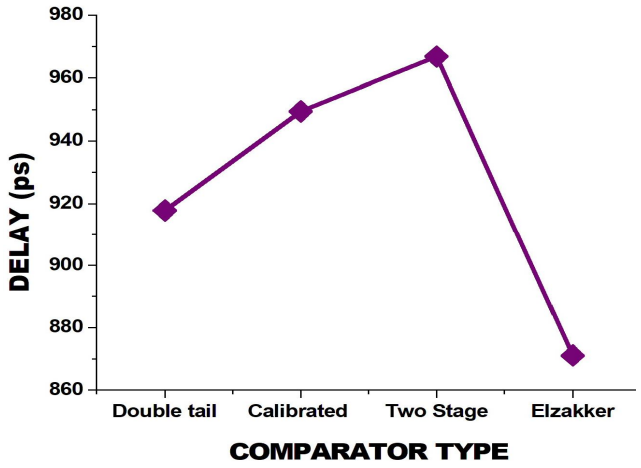

Figure 7: Comparison of delay with Dynamic Comparators

Figure8 describes the comparison of PDP with various dynamic comparators where this PDP comparison is identical to the power comparison in figure6. PDP is maximum for a double tail dynamic comparator and minimum for an Elzaker dynamic comparator. The PDP for the common mode of operation is more compared with the differential mode of operation for all the dynamic comparators discussed.

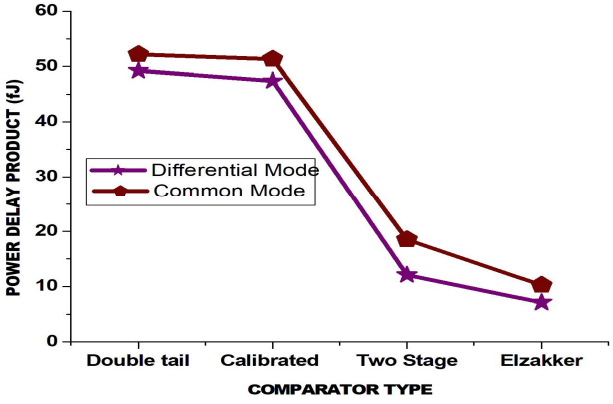

Figure 8: Comparison of PDP with Dynamic Comparators

4. CONCLUSION

An evident practical approach to identify the best dynamic comparator in performance is achieved by relating the performance of different dynamic comparators in terms of their characteristic parameters like power, delay & PDP. The best dynamic comparator earmarked is the Elzaker dynamic comparator with minimum dynamic power dissipation, less delay & minor PDP. The dynamic power dissipation, delay & PDP for an Elzaker dynamic comparator is reduced by 84%, 5% & 86% compared with the double tail dynamic comparator. Dynamic comparators proved that the best performance is achieved in the differential mode of operation compared with the common mode of operation with each characteristic parameter like power, delay & PDP with f = 1 GHz, V_{DD} =1.2V at a uniform temperature of 27^{o}C.

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