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Modelling and Performance Analysis of a DSTATCOM using ISCT Control Technique

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ABSTRACT

This paper chiefly deals with the performance of DSTATCOM as a load compensator. For enhancing the power quality and so as to mitigate harmonics it is employed on the load side. The reactive power is absorbed or generated by DSTATCOM by regulating the bus voltage. The most reason for occurring of the power quality issues is because of the non-liner loads that were employed by the consumers. DSTATCOM works as inductive or capacitive modes basing on the system voltage. The analysis is performed on the issues in the distribution side by employing the DSTATCOM compensation in this paper. In this paper,we had adopted Instantaneous Symmetrical Compound Theory (ISCT) controller to mitigate harmonics on the source side. The harmonics are due to the increase in the usage of non-linear loads by the consumers. The DSTATCOM regulates the bus voltage by absorbing or generating reactive power. The results are extracted using extensive digital simulation performed in MATLAB/SIMULINK environment.

Key words: Power Quality, *DSTATCOM, ISCT algorithm, VSC,* Active tuned hybrid power filter (ATHPF)

1. INTRODUCTION

Huge utilization of semiconductor devices, integrated-circuit (IC) chips, non-linear loads and other power electronic devices introduce the harmonics and other power quality problems in the power system.These introduced harmonics brought down the efficiency and power factor, increase the risk of electromagnetic interference with neighbouring communication lines.The main objective of electric utilities is to supply their customers an uninterrupted sinusoidal voltage of constant magnitude and frequency with sinusoidal balanced currents at the AC mains. However, present day AC distribution systems are facing severe power quality (PQ) problems such as high reactive power burden, unbalanced loads, harmonic rich load currents and an excessive neutral current.

Power quality problems in a distributed power system can be mitigated by usingActive Power Filters (APFs) and Distributed Static Compensator(DSTATCOM).DSTATCOM can be used for compensation of reactive power and unbalanced loading in the distribution system. Removal of harmonics in power system can be done in two ways:
By providing a low impedance path to ground for harmonic signal, for this passive tuned filter can be used.
By injecting compensating signals which are in phase opposition with the harmonic signal present in the system, this can be done by using active filters.
Series inductor allowing the reactive power control. Static DC bus capacitors and passive filters have been utilized to improve power quality (PQ) in a distribution system.

2. SYSTEM TOPOLOGY

A DSTATCOM consists of a 3-phase inverter using IGBTs. The design of the DSTATCOM includes a Voltage source inverter, interfacing inductor and ripple filter. The main function of DSTATCOM is to provide reactive power as demanded by the load. Therefore, with the help of DSTATCOM, source currents are maintained at unity power factor and reactive power burden on the system gets reduced. Rating of the DSTATCOM depends on the required reactive power compensation and degree of unbalance. The ripple filter is used to filter the switching ripples of the voltage and current at point of common coupling (PCC).
The design of the DC bus capacitor depends on the energy storing capability needed during the transient condition. The required compensation is provided by the DSTATCOM. The DSTATCOM is connected at the point of common coupling (PCC) through an interfacing ripple filter as shown in the fig.1.In order to generate the compensation current that follows the current reference, a hysteresis current control method is adopted

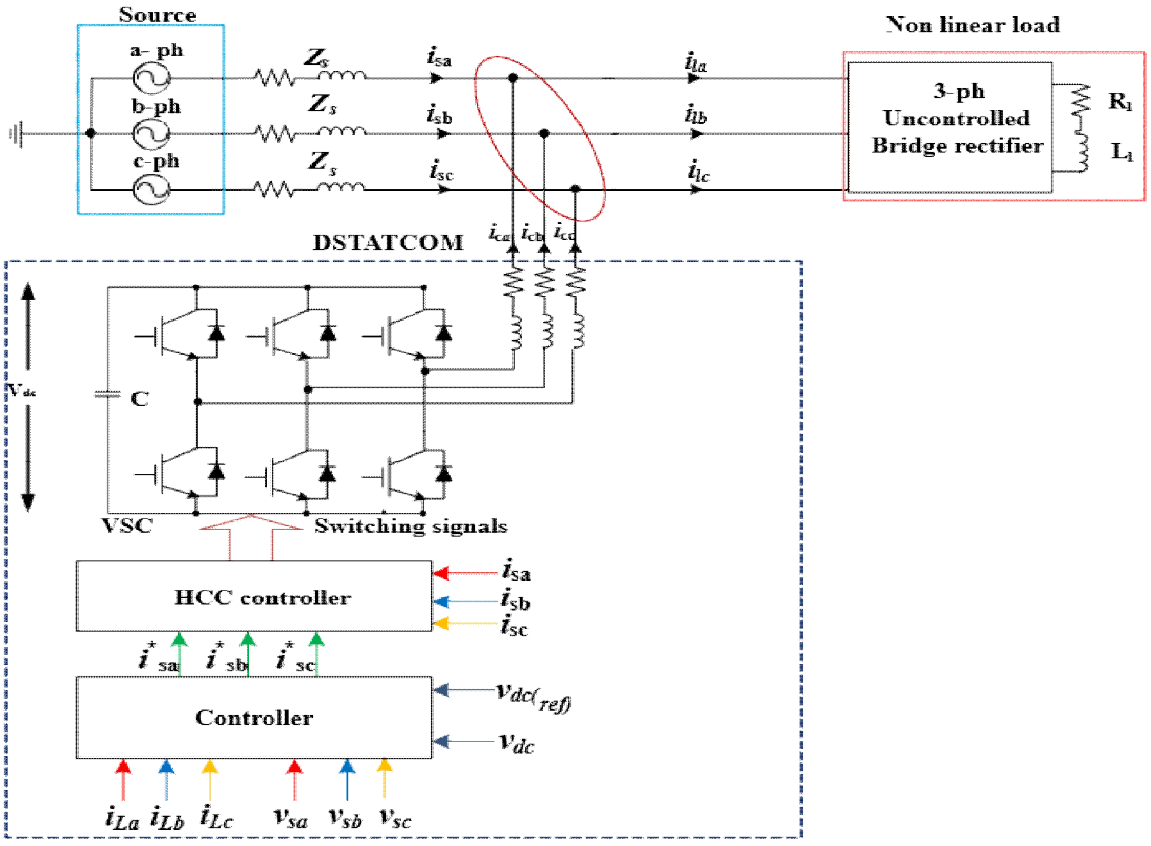

Fig.1. shows Design of distribution system with different topology based DSTATCOM

3. *ISCT* CONTROL ALGORITHM

Many control schemes are reported for control of DSTATCOM e.g Synchronous Reference Frame (SRF) theory, Instantaneous Symmetrical Component (ISCT) theory, Instantaneous Reactive Power (IRPT) theory, IcosΦ algorithm, Current Synchronous Detection (CDS) algorithm, power Balance theory (PBT), Adaline based algorithm etc. Generation of proper gating pulses for the IGBTs of VSC is very crucial for proper implementation of the load compensation.

The advent of the low switching loss IGBTs has enabled the designers to shift from fundamental frequency switching to PWM (Pulse Width Modulation) based switching. Further, custom power being a relatively low power application, PWM methods offer a more flexible option than fundamental frequency switching methods favoured in FACTS applications. Though various topologies of VSC have been reported, single 3-phase VSC Bridge with six IGBT switches is widely reported for DSTATCOM. In this chapter performance of following algorithms used for reference current extraction and for generating PWM gating pulses for the inverter, have been studied.

The control algorithm block diagram is shown in Fig 1. The DSTATCOM is controlled in such a way that the source currents (i_{sa}, i_{sb} and i_{sc}) and load currents (i_{la}, i_{lb} and i_{lc}) are balanced and sinusoidal in phase with the respective terminal voltages (v_{sa}, v_{sb} and v_{sc}). In addition, average load power (P_{lavg})and losses (P_{loss}) in the VSC are supplied by the source. Since the source considered here is non stiff, the direct use of terminal voltages to calculate reference compensator currents will not provide satisfactory compensation. Therefore, the fundamental positive sequence components of three-phase voltages are extracted to generate reference compensator currents (i_{ca}, i_{cb} and i_{cc}) based on the instantaneous symmetrical component theory.

Due to inverter switching and unbalanced loads, the PCC voltages will be distorted and unbalanced. Hence, fundamental positive sequence components of the PCC voltages are to be extracted. Let us denote instantaneous positive sequence voltages as V_{a1}, instantaneous negative sequence voltage V_{a2} and instantaneous zero sequence voltage V_{a0}, respectively for phase-a.

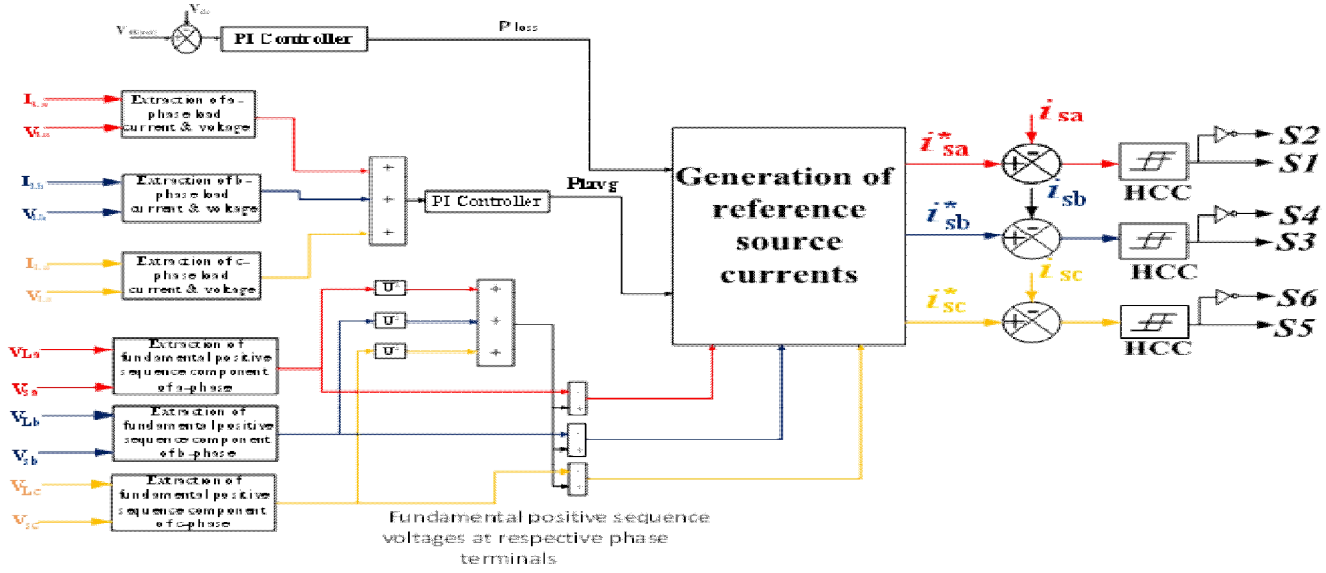

Fig.2. shows Block diagram of ISCT control technique

These sequence voltages are expressed using symmetrical transformation as follow:

$$\begin{bmatrix} V_{a_0} \\ V_{a_1} \\ V_{a_2} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

Where, '*a*' is a complex operator and is equal to $1\angle 120^0$ or $e^{-j2\pi/3}$

The calculation of the steady state positive sequence voltage can be carried using the following expression:

$$V_{a_1} = \frac{1}{3}[V_a + aV_b + a^2 V_c]$$

The term $V_{a1}$is a complex quantity and therefore has both magnitude and angle and can be expressed by (3).

$V_{a1}=|V_{a1}|\angle V_{a1}$

From equation (2), the three phase positive sequence components can be expressed in time domain as follows:

$V_{a1}=\sqrt{2}|V_{a1}|\sin(\omega t+\angle V_{a1})$

$V_{b1}=\sqrt{2}|V_{a1}|\sin(\omega t-2\pi/3+\angle V_{a1})$

$V_{c1}=\sqrt{2}|V_{a1}|\sin(\omega t+2\pi/3+\angle V_{a1})$

The method is simple as it involves synchronization of only one phase (phase-*a*).

These currents are given as follows:

$$i^*_{sa} = \frac{v_{a1}^+}{\Delta_1}(P_{lavg} + P_{loss})$$

$$i^*_{sb} = \frac{v_{b1}^+}{\Delta_1}(P_{lavg} + P_{loss})$$

$$i^*_{sc} = \frac{v_{c1}^+}{\Delta_1}(P_{lavg} + P_{loss})$$

Where,v_{a1}^+,$v_{b1}^+$and $v_{c1}^+$are fundamental positive sequence voltages at the respective phase load terminal.

$\Delta_1 = (v_{a1}^+)^2 + (v_{b1}^+)^2 + (v_{c1}^+)^2$

The terms Plavg and Ploss represent the average load power and the total losses in the VSC, respectively.

At any arbitrary time, *x*, it is computed as follows:

$$P_{lavg} = \frac{1}{T}\int_{x-T}^{T}(V_a i_{la} + V_b i_{lb} + V_c i_{lc})\,dx$$

The total losses in the VSC are computed using a proportional–integral (PI) controller at the positive zero crossing of phase-a voltage and is given as

$P_{loss}=K_P V_{dc(error)} + K_i \int V_{dc(error)}\,dx$

Where k_p and k_i are the proportional gain and integral gain of the PI controller respectively. The compensator currents (i_{ca}, i_{cb} and i_{cc}) are obtained by subtracting the actual load currents from the reference source currents. Then the compensator currents error is regulated around a pre-defined hysteresis current controllers(HCC_1,HCC_2&HCC_3) and IGBT Eight switching pulses are generated (S1, S2, S3, S4,S5, S6, S7 & S8).

However, in case of unbalanced and/ or distorted source voltage condition the reference current generation will be decided by using the Fundamental positive sequence component of unbalanced/distorted source voltages (v_a^+,v_b^+,v_c^+)

dx*dx*

Where k_p and k_i are the proportional gain and integral gain of the PI controller respectively. The compensator currents (i_{ca}, i_{cb} and i_{cc}) are obtained by subtracting the actual load currents from the reference source currents. Then the compensator

currents error is regulated around a predefined hysteresis current controllers(HCC_1,HCC_2& HCC_3) and IGBT Eight switching pulses are generated (S1, S2, S3, S4,S5, S6, S7 & S8).

4. HYSTERESIS CURRENT CONTROLLER

Hysteresis current control is a method of controlling a voltage Source converter so that an output current is generated to follow a reference current waveform. The principle of the hysteresis control method for an APF is implemented by presenting the upper and lower tolerance limits which need to be compared to the extraction error signal The maximum error is the difference between the upper and lower limit, and this hysteresis tolerance bandwidth is mostly equal to two times of the error.If the error signal is within the tolerance band, there will be no switching action for the filter. However, when the error leaves the tolerance band, switching pulses will be generated and the APF will produce signals to be injected into the supply line. Fig. 3 illustrates the ramping of the current between the two limits. The upper hysteresis limit is the sum of the reference current and the maximum error or the difference between the upper limit and the reference current. The lower hysteresis is defined by the subtraction of the reference current and the minimum error.

According to the operating principle of the inverter, the output voltages of each phase are significant of the switching pulses of the switches in each leg. As a result, the switching gates for the APF can be obtained.

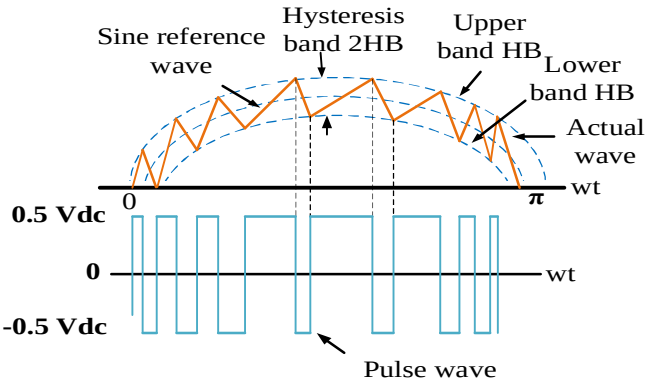

Fig. 3.shows Hysteresis Current Control (HCC) operation waveform

Table-1 shows Simulation parameters

Grid parameters	Source voltage:(V_s)=415V (L-L),50Hz
	Source inductance, (L_s)=8mH
	Source resistance, (R_s)=0.95 Ω
VSC parameters	$V_{dc(ref)}$ =700V, C_{dc} =900μF, L_c = 8 mH, R_c = 0.95 Ω
Load parameters	3-Ø non-linear RL load R1= 10Ω, L1=15mH

5. MATLAB RESULTS AND DISCUSSION RESULTS OF SIMULATION

The simulation performance of the DSTATCOM is carried out using MATLAB/Simulink. The ISCT control algorithm is considered to evaluate the effectiveness of both two topologies. These are as follows:

(a)Power distribution system with DSTATCOM under balanced condition

(b)Power distribution system with DSTATCOM under unbalanced condition

Case(a): POWER DISTRIBUTION SYSTEM WITH DSTATCOMUNDER BALANCED CONDITION

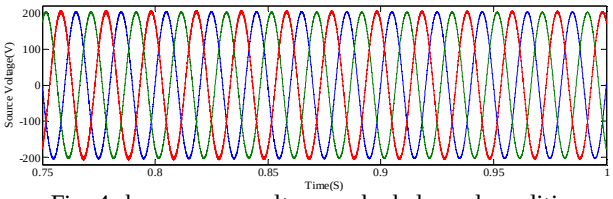

Fig. 4.showssource voltage under balanced condition

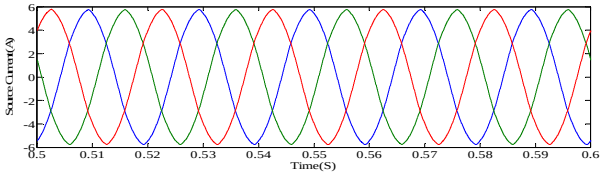

Fig. 5. Shows source current under balanced condition

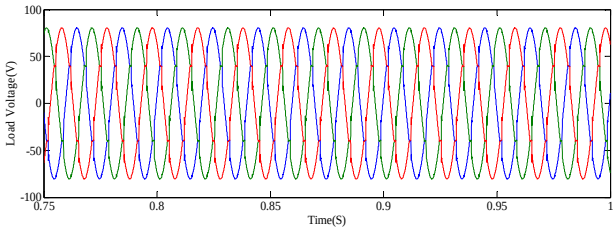

Fig. 6.Shows load voltage under balanced condition

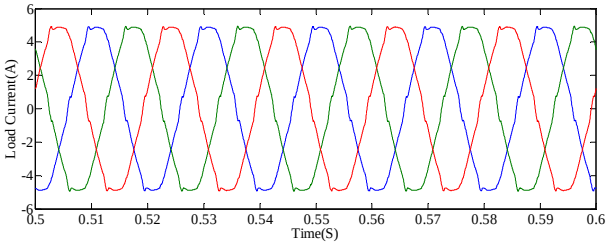

Fig. 7. showsload current under balanced condition

The above figures(4,5,6,7) show the results of DSTATCOM with the point of common coupling under balanced condition of : source volage, source current, loadvoltage, load current.

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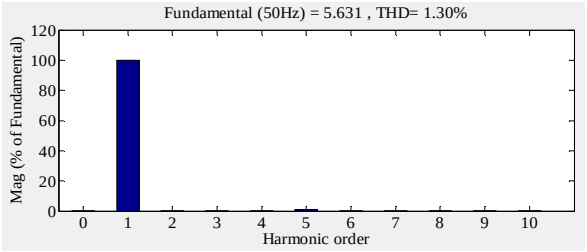

Fig. 8. Shows THD of source current with DSTATCOM under balanced load condition

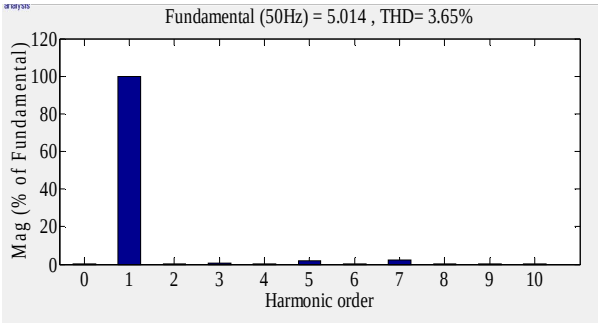

Fig. 9. Shows THD of load current with DSTATCOM under balanced load condition

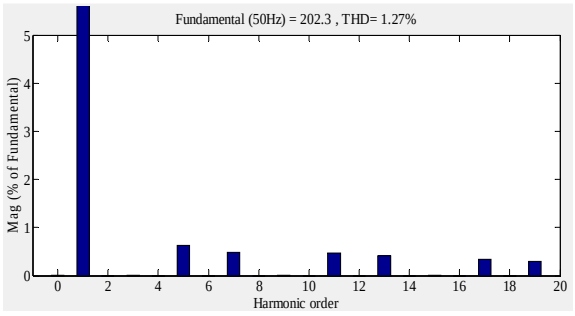

Fig. 10. ShowsTHD of source voltage with DSTATCOM under balanced load

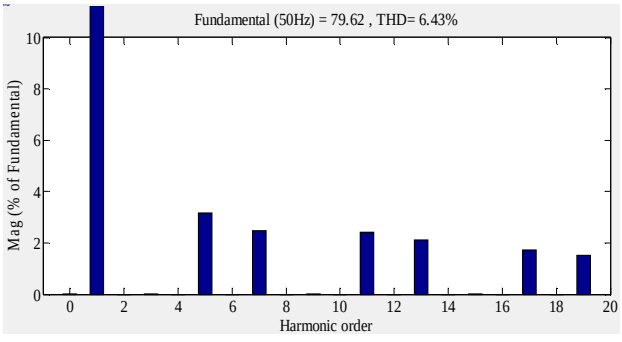

Fig. 11.shows THD of load voltage with DSTATCOM under balanced load

CASE(B): POWER DISTRIBUTION SYSTEM WITH DSTATCOM UNDER UNBALANCED CONDITION

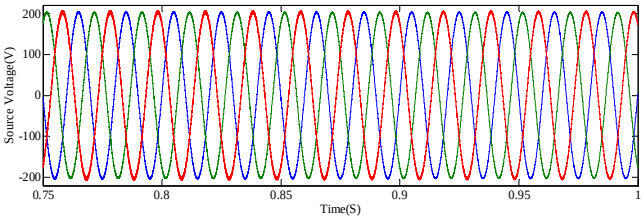

Fig. 12.shows source voltage under unbalanced condition

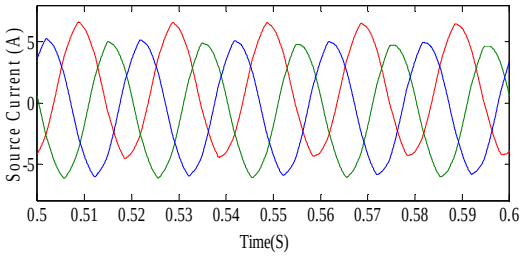

Fig. 13.shows source current under unbalanced condition

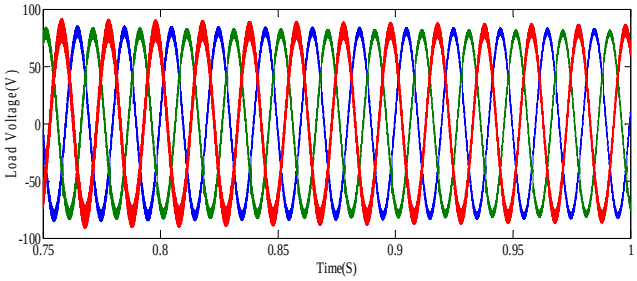

Fig. 14.shows load voltage under unbalanced condition

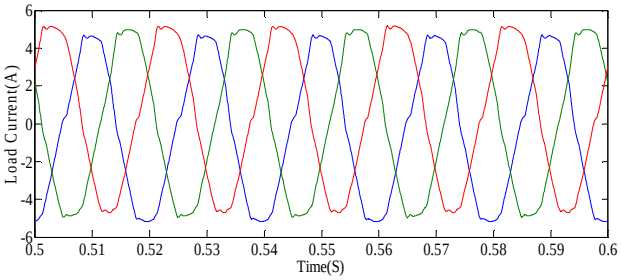

Fig. 15. Shows load current under unbalanced condition

The above figures(12,13,14,15) show the results of DSTATCOM with the point of common coupling under unbalanced condition of : source volage, source current, loadvoltage, load current.

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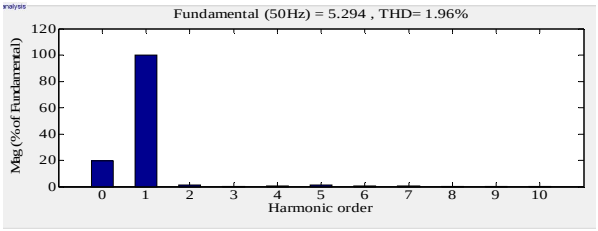

Fig. 16.shows THD of source current with DSTATCOM under unbalanced load condition

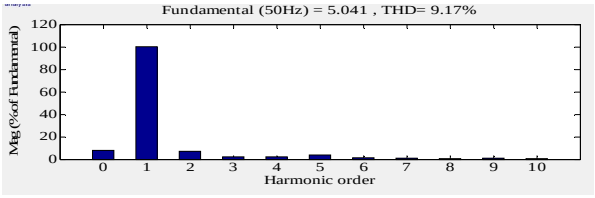

Fig. 17. Shows THD of load current with DSTATCOM under unbalanced load condition.

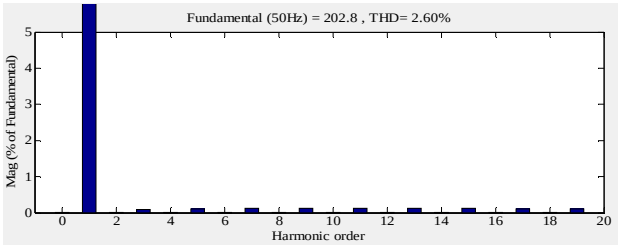

Fig. 18.Shows THD of source voltage with DSTATCOM under unbalanced load condition.

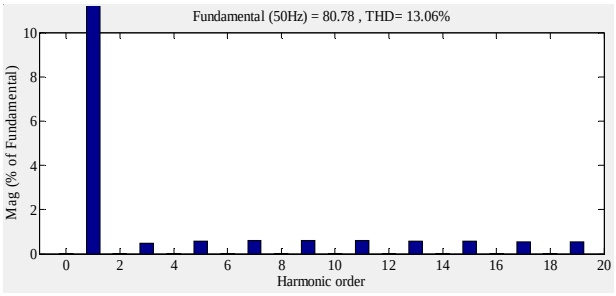

Fig. 19. Shows THD of load voltage with DSTATCOM under unbalanced load condition.

This section describes the system performance, when the single DSTATCOM using ISCT control algorithm (Table1). From above figures, it is observed that due to unbalanced and non-linear load, source currents and load currents get unbalanced and some distortion is present in their waveform. Also, power factor of the source is not unity, as voltage at PCC and source currents are not in Phase with each other. Total Harmonic Distortion for the source current is 18.42%, when no DSTATCOM is connected, when DSTATCOM is connected the THD of source current is 1.30%.

COMPARATIVE STUDY

Table.2. shows comparative study of DSTATCOM

S. No	Cases	Source current (mag, %)	Load current
1	Without DSTATCOM	42.93,18.42	42.93,18.42
2	With DSTATCOM (balanced)	5.63,1.30	5.014,3.65
3	With DSTATCOM (unbalanced)	5.294,1.96	5.041,9.17

5.CONCLUSION

The main purpose of employing the DSTATCOM on the distribution is to mitigate harmonics in source side as well as load side and also to maintain the constant voltage at Point of Common Coupling (PCC) for balanced and unbalanced load variation. From the simulation studies the percentage of THD of source current and load current are 1.30 and 3.65 using ISCT control technique. This control technique is capable of better shunt compensation including harmonic mitigation load balancing, voltage regulation as recommendations governed by IEEE 519-1992 standards than other conventional methods.

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