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Implementation of three phase five level multilevel inverter

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Abstract—A new configuration of a three-phase five-level multilevel inverter is introduced here. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, multilevel inverters used. These inverters include an arrangement of semiconductors and dc voltage sources required to generate a staircase output waveform, this waveform look like a sinusoidal waveform. The new topology constitutes the conventional three-phase two-level bridge with three bidirectional switches. A multilevel dc link using fixed dc voltage supply and cascaded half-bridge is connected in such a way that the new inverter outputs the required output voltage levels. Here, to generate the appropriate switching gate signals staircase modulation technique is used. The new topology results in reduction of installation area and cost. The validity of the inverter and its performance are verified by using MATLAB/SIMULINK and the results also presented.

Key words **—Bidirectional switch, fundamental frequency staircase modulation, multilevel inverter.**

1. INTRODUCTION

In Recent Years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network[1]-[2]. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels.

Multilevel inverters include an array of power semiconductors and voltage sources, the output of which generate voltages with stepped waveforms. This technology has started with the three-level converter followed by numerous multilevel converter topologies. The cascade multilevel inverter was first proposed in 1975. The common multilevel inverter configurations are neutral point clamped (NPC)[3], the flying capacitor (FC), and the cascaded H-bridge (CHB)[5]-[6]. The diode-clamped inverter was first used in a three-level inverter in which the mid-voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s. The deviating voltage of neutral-point voltage in NPC, the unbalanced voltage in the dc link of FC, and the large number of separated dc supplies in CHB are considered the main drawbacks of these topologies.

Asymmetrical and hybrid multistage topologies are becoming one of the most interested research area. In the asymmetrical configurations, the magnitudes of dc voltage supplies are unequal[6]. These topologies reduce the cost and size of the inverter and improve the reliability since minimum number of power electronic components, capacitors, and dc supplies are used. The hybrid multistage converters consist of different multilevel configurations with unequal dc voltage supplies. With such converters, different modulation strategies and power electronic components technologies are needed. For the purpose of improving the performance of the conventional single and three phase inverters, different topologies employing different types of bidirectional switches have been suggested in [7]–[8]. As compared to the unidirectional, bidirectional switch are able to conduct the current and withstanding the voltage in both directions. Bidirectional switches with an appropriate control technique can improve the performance of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels.

Based on this technical background, this suggests a novel topology for a three phase five-level multilevel inverter. The number of switching devices, insulated-gate driver circuits, and installation area and cost are significantly reduced. The magnitudes of the utilized dc voltage supplies have been selected in a way that brings the high number of voltage level with an effective application of a fundamental frequency staircase modulation technique. Simulation results are given and explained. This paper is organized as follows: The outline of this paper is as follows. In Section II, the three phase five level multilevel inverter and its operation. In Section III it includes simulations and results in Finally, Section VI presents some conclusions based on the results from this paper.

2. THE THREE PHASE FIVE LEVEL MULTILEVEL INVERTER AND ITS OPERATION

The new topology constitutes the conventional three-phase two-level bridge with three bidirectional switches. It use a multilevel dc link with fixed dc voltage supply and cascaded half-bridge is connected in such a way that the new inverter outputs the required output voltage levels. Figure.1 shows the typical configuration of the three-phase five-level multilevel inverter. It consists of one bidirectional switch and two diodes and two switches in each phase. The three bidirectional switches are S1-

S6,Da1-Da2. The other switches are named as Q1-Q6, the diodes are denoted as D1-D6. Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the conventional three-phase two-level bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o).A multilevel dc link built by a single dc voltage supply with fixed magnitude of 4*V*dc and CHB having two unequal dc voltage supplies of *V*dc and 2*V*dc are connected to bridge terminals. Moreover the CHB cells are added by the switching of T1-T4 switches. Based on the desired number of output voltage levels, a number of CHB cells are used. Since the new inverter is designed to achieve five voltage levels, the power circuit of the CHB makes use of two series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels.

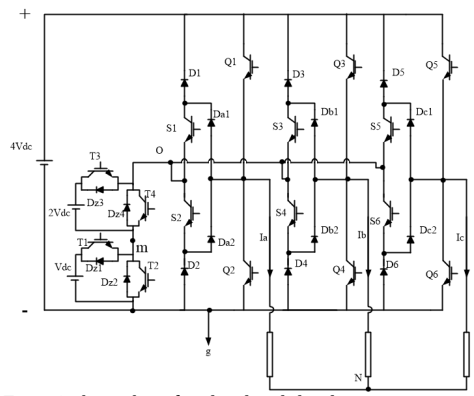

Figure1. three-phase five-level multilevel inverter

Operating Status Of The Switches

By considering phase *a*, the operating status of the switches and the inverter line-to-ground voltage *V*ag are given in Table1.

TABLE 1 Switching State *Sa* and Inverter Line-to-Ground Voltage *V*ag

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	Vag
4	On	Off	Off	Off	On	Off	On	Off	$+4V_{dc}$
3	Off	On	On	Off	On	Off	On	Off	$+3V_{dc}$
2	Off	On	On	Off	Off	On	On	Off	$+2V_{dc}$
1	Off	On	On	Off	On	Off	Off	On	$+V_{dc}$
0	Off	Off	Off	On	On	Off	Off	On	0

Depending on the switching sequence given in the table different voltage levels can be achieved. It is easier to define the inverter line-to-ground voltages *V*ag, *V*bg , and *V*cg in terms of switching states *Sa*, *Sb*, and *Sc* as,

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{4V_{dc}}{N-1} \times \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix}$$

where $N = 5$ is the maximum number of voltage levels. The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table 2. The inverter may have 24 different modes within a cycle of the output waveform. According to Table.2, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on state. As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current *I*b can flow in S3 and Db1 or S4 and Db2). Since some insulated gate bipolar transistors (IGBTs) share the same switching gate signals, the proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity.

TABLE 2 Switching States Sequence Of The new Inverter Within One Cycle

Sa, Sb, Sc	Period T[s]	ON switches Leg a	ON switches Leg b	ON switches Leg c	ON switches cascaded half bridge	V_{ag} [V]	V_{bg} [V]	V_{cg} [V]
400	t1	Q1	Q4	Q6	T1,T4	$4V_{dc}$	0	0
410	t2	Q1	S3,S4	Q6	T1,T4	$4V_{dc}$	V_{dc}	0
420	t3	Q1	S3,S4	Q6	T2,T3	$4V_{dc}$	$2V_{dc}$	0
430	t4	Q1	S3,S4	Q6	T1,T3	$4V_{dc}$	$3V_{dc}$	0
440	t5	Q1	Q3	Q6	T1,T3	$4V_{dc}$	$4V_{dc}$	0
340	t6	S1,S2	Q3	Q6	T1,T3	$3V_{dc}$	$4V_{dc}$	0
240	t7	S1,S2	Q3	Q6	T2,T3	$2V_{dc}$	$4V_{dc}$	0
140	t8	S1,S2	Q3	Q6	T1,T4	V_{dc}	$4V_{dc}$	0
040	t9	Q2	Q3	Q6	T1,T4	0	$4V_{dc}$	0
041	t10	Q2	Q3	S5,S6	T1,T4	0	$4V_{dc}$	V_{dc}
042	t11	Q2	Q3	S5,S6	T2,T3	0	$4V_{dc}$	$2V_{dc}$
043	t12	Q2	Q3	S5,S6	T1,T3	0	$4V_{dc}$	$3V_{dc}$
044	t13	Q2	Q3	Q5	T1,T3	0	$4V_{dc}$	$4V_{dc}$
034	t14	Q2	S3,S4	Q5	T1,T3	0	$3V_{dc}$	$4V_{dc}$
024	t15	Q2	S3,S4	Q5	T2,T3	0	$2V_{dc}$	$4V_{dc}$
014	t16	Q2	S3,S4	Q5	T1,T4	0	V_{dc}	$4V_{dc}$

004	t17	Q2	Q4	Q5	T1,T4	0	0	$4V_{dc}$
104	t18	S1,S2	Q4	Q5	T1,T4	V_{dc}	0	$4V_{dc}$
204	t19	S1,S2	Q4	Q5	T2,T3	$2V_{dc}$	0	$4V_{dc}$
304	t20	S1,S2	Q4	Q5	T1,T3	$3V_{dc}$	0	$4V_{dc}$
404	t21	Q1	Q4	Q5	T1,T3	$4V_{dc}$	0	$4V_{dc}$
403	t22	Q1	Q4	S5,S6	T1,T3	$4V_{dc}$	0	$3V_{dc}$
402	t23	Q1	Q4	S5,S6	T2,T3	$4V_{dc}$	0	$2V_{dc}$
401	t24	Q1	Q4	S5,S6	T1,T4	$4V_{dc}$	0	V_{dc}

3. SIMULATION RESULTS AND DISCUSSIONS

The new multilevel inverter is modelled using MATLAB/SimPowerSystems. The interfaces and controllers are done using Simulink toolbox. The studied system is modelled in continuous-time mode. The figure2 shows the simulation diagram of three phase five level multilevel inverter and the simulation results are also showed.

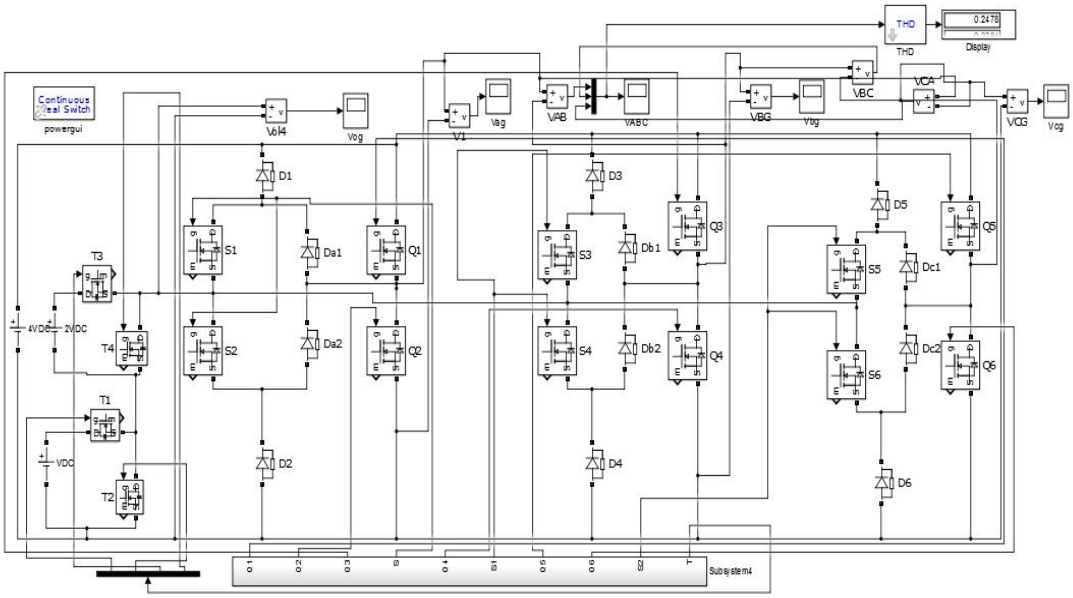

Figure2. Simulation diagram of the 3 phase five level multilevel inverter

Here in order to get the waveforms more clearly we use V_{dc} as 10v. So $4V_{dc}$ is equal to 40V, $3V_{dc}$ is equal to 30V, $2V_{dc}$ is equal to 20V and V_{dc} is equal to 10V. The gating signals for the switches are given by using the combinatorial logic. The Combinatorial Logic block implements a standard truth table for modelling programmable logic arrays (PLAs), logic circuits, decision tables, and other Boolean expressions. W can use this by specify a matrix that defines all possible block outputs as the Truth table parameter. Each row of the matrix contains the output for a different combination of input elements and also specify outputs for every combination of inputs. The number of columns is the number of block outputs.

Here the bidirectional switches are denoted as , S1-S2 as S, S3-S4 as S1, S5-S6 as S2. The inverter may have 24 different modes within a cycle of the output waveform. According to Table.2, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in onstate. In phase A the switch corresponding to 4 V_{dc} is Q1,ie, if we want to get 4 V_{dc} then switch on Q1 and for 0V switch on Q2. For getting the remaining corresponding bidirectional switches were turned on ie, CHB cells. This pattern for each phase is simply hard coded. Here it use three repeating sequence blocks, this sequence follows the same order of Sa, Sb,Sc in table 3.2 each contain 24 stages. Example if 4 appears in the repeating sequence, that denote $4V_{dc}$ is needed so Q1 should be turned on.0 appears in the repeating sequence that denote 0 is needed so Q2 should be turned on. 1,2,3 appears in the repeating sequence that denote V_{dc} ,$2V_{dc}$, 3 V_{dc} is needed so S should be turned on. Other phases are similar to this. Then corresponding sample time is calculated.

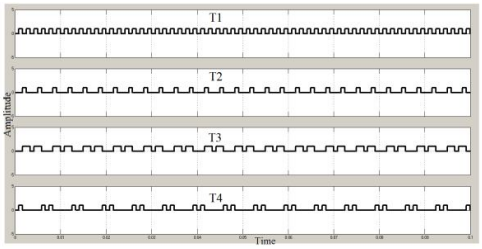

Figure3. gaiting signals for switches T1, T2, T3, T4.

The Figure.3 shows the gaiting signals for switches T1, T2, T3, T4. This is from the combinatorial logic. In

figure 4 we can see the five level voltages. The Figure5 shows the Waveform of line voltages V_{ab} V_{bc} V_{ca}.

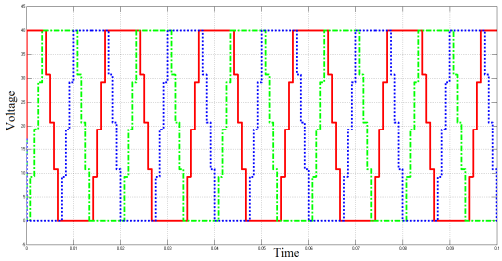

Figure4.Waveform of voltages V_{ag} V_{bg} V_{cg}

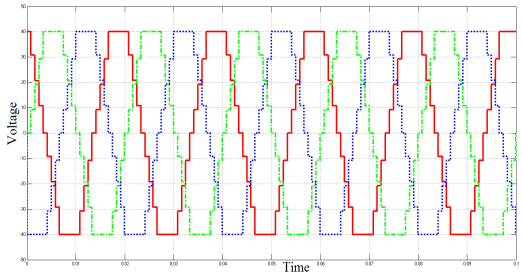

Figure 5. Waveform of line voltages V_{ab} V_{bc} V_{ca}

4. CONLUSION

Multilevel inverters have very important development for high power medium voltage AC drives. They are widely used in high power industrial applications such as ac power supplies, static VAR compensators, drive systems, etc.. Multilevel inverters include an arrangement of semiconductors and dc voltage sources required to generate a stepped output voltage waveform. The number of input DC voltages depends on the number of inverter output voltage levels and as the levels are increased the harmonics are reduced. A new topology of the three-phase five-level multilevel inverter was introduced. The suggested configuration was obtained from reduced number of power electronic components. Therefore, the new topology results in reduction of overall size and that results in reduction of installation area. Due to the reduction in the number of components and overall size will cause minimisation of overall cost. The fundamental frequency staircase modulation technique was comfortably employed and showed high flexibility and simplicity in control. Moreover, the new configuration can be extended to *N*-level with different methods. The obtained simulation results met the desired output. Hence, subsequent work in the future may include an extension to higher level with other methods.

REFERENCES

[1]. J. Rodriguez *et al.*, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2]. L. G. Franquelo *et al.*, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[3]. J. Rodriguez *et al.*, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[4]. M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.

[5]. C. Govindaraju and K. Baskaran, "Efficient sequential switching hybridmodulation techniques for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1639–1648, Jun. 2011.

[6]. M. Saeedifard *et al.*, "Operation and control of a hybrid seven-level converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 652–660, Feb. 2012.

[7]. P. Sung-Jun *et al*., "A new single-phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 831–843, May 2003.

[8]. C. Klumpner and F. Blaabjerg, "Using reverse-blocking IGBTs in power converters for adjustable-speed drives," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 807–816, May/Jun. 2006.