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Low Power High Performance 8bit Vedic Multiplier Using 16nm

A. Keerthi[1], S. Manoj[2], G. Manjula[3], Kashiraj Vitthal Kalashetti[4]
[1]Department of Electronics and Communication Engineering, Madanapalle Institute of Technology and Science Madanapalle, Andhra Pradesh, India, 19691a0485@mits.ac.in
[2]Department of Electronics and Communication Engineering, Madanapalle Institute of Technology and Science Madanapalle, Andhra Pradesh, India 19691a04A8@mits.ac.in
[3]Department of Electronics and Communication Engineering, Madanapalle Institute of Technology and Science Madanapalle, Andhra Pradesh, India, 19691a04A5@mits.ac.in
[4]Department of Electronics and Communication Engineering, Madanapalle Institute of Technology and Science Madanapalle, Andhra Pradesh, India, kashirajvk@mits.ac.in

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ABSTRACT
In this paper, an 8-bit Vedic multiplier is designed. The performance of the system basically works better if the performance of the multiplier is good. In today's digital time, Multiplier is one which consumes power at the same time speed of multiplier is playing very important aspects in this. Multiplier Optimization for power and delay both will play an important role. Adders such as Ripple carry adder and carry look-ahead adder and carry skip adder are also having a role in the selection of adder units in the multiplier. Here all the three adders are designed using transmission gates and compared using CMOS.

Keywords: Complementary Metal Oxide Semiconductor (CMOS), Transmission Gate (TG), Trigger, Target, Ripple Carry Adder (RCA), Carry Look Ahead (CLA), Carry Skip adder (CSA), Delay, area.

1. INTRODUCTION

Multipliers play an important role in today's digital signal processing and various other applications. In high performance systems uses addition and multiplication of two binary numbers is fundamental and most often used arithmetic operations. Statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. So, these operations overcome the execution time. That's why; there is need of high-speed multiplier. The demand of high-speed processing has been increasing as a result of expanding computer and signal processing applications. Low power consumption is also an important issue in multiplier design. To reduce significant power consumption, it is good to reduce the number of operations thereby reducing dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has increased. Designer mainly concentrates on high speed and low power efficient circuit design. The aim of a good multiplier is to provide a physically packed together, high speed and low power consumption unit.

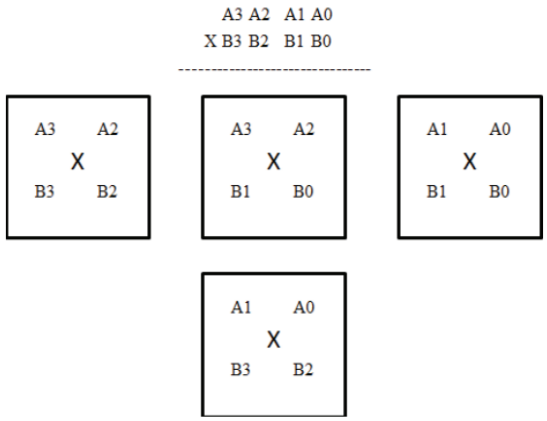

Figure 1: 4-Bit Vedic Multiplication

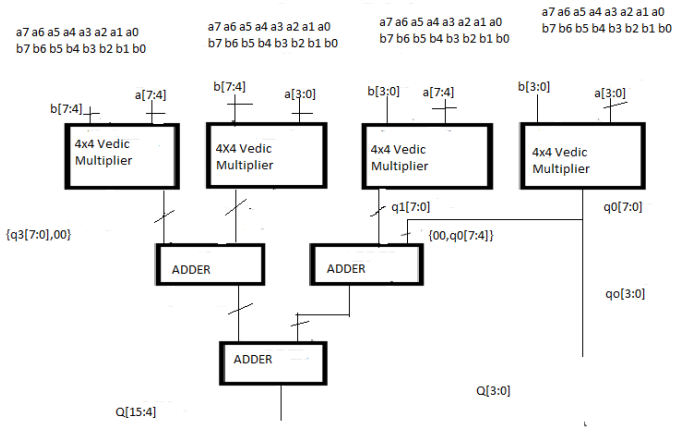

Figure 2: Block diagram of 8-Bit Vedic Multiplication

Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. We discuss a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. A simple digital multiplier (referred henceforth as

Vedic multiplier) architecture based on the Urdhva Triyakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. In this paper, after a gentle introduction of this Sutra, it is applied to the binary number system to make it useful in the digital hardware. The hardware architecture of the Vedic multiplier is presented and is shown to be very similar to that of the popular array multiplier. It is also equally likely that many such similar technical applications might come up from the storehouse of knowledge, Veda, if investigated properly [11-13].

Figure 1 shows the 4-bit Vedic multiplication can only multiply two 4-bit numbers. The 4-bit Vedic multiplier is a relatively simple circuit compared to larger multipliers, but it can still provide faster multiplication than traditional multiplication circuits. Similarly, in Figure 2 shows the 8-bit Vedic multiplication which multiplies two 8-bit binary numbers. But 8-bit Vedic multiplier is a more complex circuit than the 4-bit multiplier but it still can provide faster multiplication than traditional multiplication circuits especially for certain input patterns.

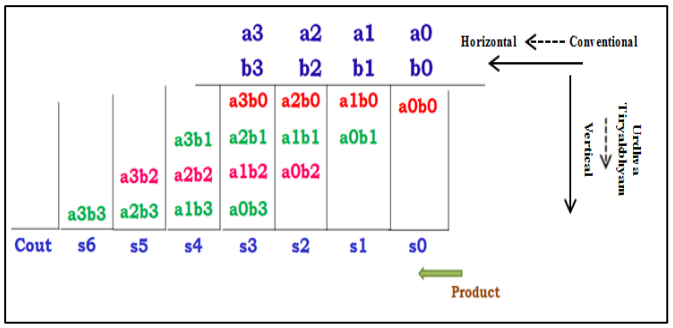

Figure 3: Conventional method Versus Vedic technique

The dedicated multiplication circuit uses Full Adder's circuit to perform Carryout Multiplication. Hence the performance of multiplier also depends on the performance of the adder [5]. Figure 3 shows conventional approach of multiplication partial products are summarized only after each partial product has been obtained horizontally. In Vedic multiplication technique partial products are summed vertically added simultaneously until all the items in the column are collected. The different types of adders are Ripple carry adder, carry look ahead adder, carry skip adder. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output [4]. A carry look-ahead adder reduces the propagation delay by introducing more complex hardware. In this design, the ripple carry design is suitably transformed such that the carry logic over fixed groups of bits of the adder is reduced to two-level logic. The carry out bit of the last adder doesn't wait the carry bits of previous adder. Here, all the carry bits of each adder are produced at the same time. Hence, the propagation delay reduces compared to Ripple Carry Adder [3].

A Carry Skip adder comes under the category of digital adders. In this the logic AND gate is used for every stage of adder to check whether the carry is present or not. If not, the carry bit is directly fed to the last stage of adder. By this, the carry need not to propagate through all the stages of adder in every sequence of input [2].

2. PROPOSED METHOD

[10] Advances in digital systems need to emphasize on high speed and low power circuits. As today era is related to portable devices where batter power is important issues. For the longer life of battery-operated devices, one has to work on different optimization techniques. Transistor counts are the design criteria for a multiplier with different adder cells, which largely influence the design complexity of several function units in the multiplier and MAC network. The design speed is constrained by the size of the transistors, parasitic capacitance and critical path delay. A multiplier's driving skill is very significant, as often arithmetic operations are used. In the last decade, the multiplier has played a very important role in power consumption, speed and size, but there is still scope to find out the best suitable multiplier with different adders. International Technology Roadmap for semiconductors has given the power reduction in the nearest future where handheld devices will require very less power. This paper presents a basic architecture of digital multipliers based on ancient Vedic mathematics Sutra (formula) called Urdhva Tiryakbhyam (Vertically and Crosswise) Sutra with three different adders. Comparison of the average power of TG and CMOS gate based 8X8 Vedic multiplier with RCA adder, CLA adder and CSA adder has been analysed figure 4 shows the 8-bit Vedic multiplier. All the multiplier has been designed at the transistor level and simulated in Tanner EDA [1]. In this paper Average power, Delay, Trigger and Target has been compared between both CMOS and TG.

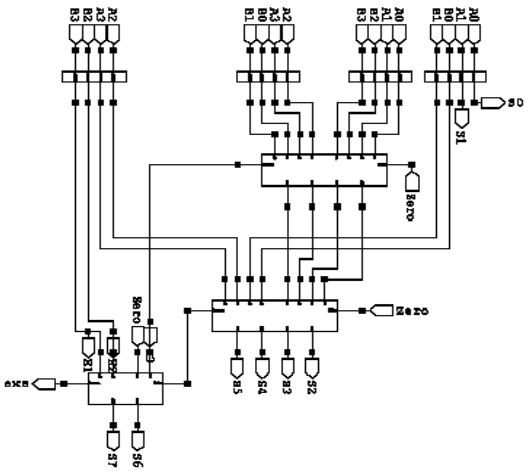

Figure 4: 8- bit Vedic multiplier

A trigger can be either an input signal or an internal signal generated within the circuit. A target is typically defined in terms of specific performance metrics, such as power consumption, speed, area, or reliability and the design process is often guided by the objective of optimizing these metrics to achieve the desired target. In general, triggers and targets are important concepts in VLSI designs.

3. SIMULATION RESULTS AND DISCUSSION

8-bit Vedic multiplier [6-7] has been designed using CMOS and TG logic style with the ripple carry, carry look ahead and carry skip adders in conventional MOSFET at 16 nm technology model. Simulation results show that the proposed architecture has advantages over conventional circuits in speed, area and power consumption. Figure 5 shows the circuit diagram of ripple carry adder in Tanner EDA. Figure 6 shows the output waveform of the RCA circuit diagram consists of voltage(V) and time (ns).

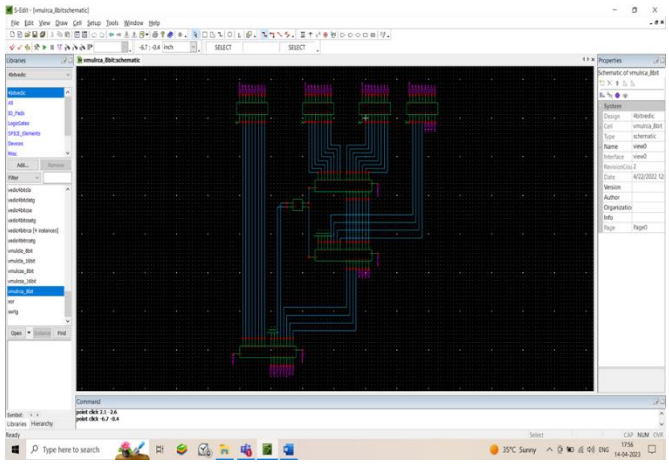

Figure 5: Ripple Carry Adder (RCA) Circuit Diagram

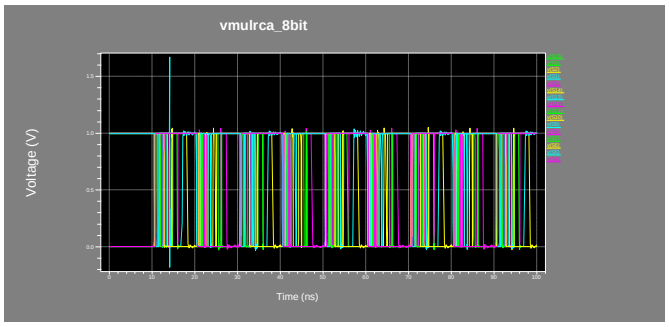

Figure 6: RCA Output Waveform

Similarly, we have designed for Carry Skip Adder (CSA) and Carry Look Ahead adder (CLA) and we will see the respective waveforms of the above adders with voltage(V) and time (ns). With A CMOS transistor having gate length 16nm, threshold voltage 0.5088 for NMOS and threshold voltage -0.450 for PMOS, also gate length 16nm, the threshold voltage is 0.469 for NMOS and threshold voltage is -0.418V for PMOS. All these parameters have been taken from predictive technology model.

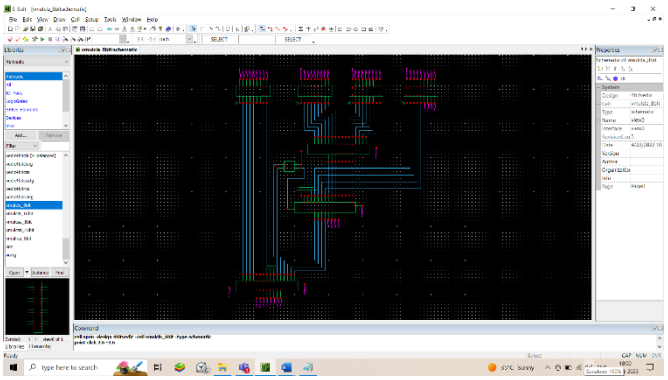

Figure 7: Carry Look Ahead Adder (CLA) Circuit Diagram

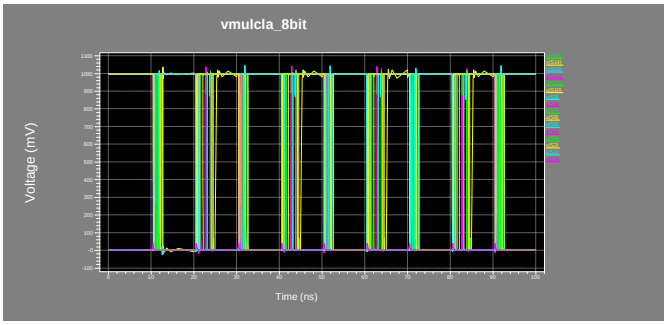

Figure 8.:CLA Output Waveform

In the above Figure 7 and Figure 8 we have designed the Carry Look Ahead Adder (CLA) circuit diagram and its output waveform.

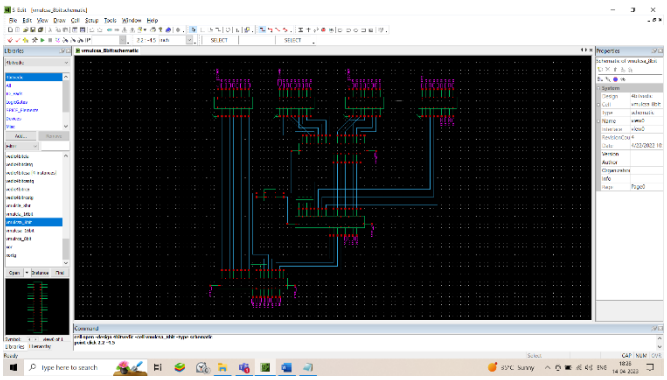

Figure 9: Carry Skip Adder (CSA) circuit diagram

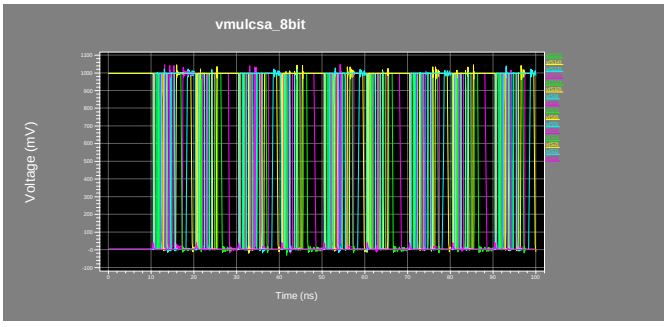

Figure 10: CSA Output Waveform

In the above Figure 9 and Figure 10 we have designed the carry skip adder circuit diagram and its output waveform. Table 1 shows the power, area and delay of CMOS and TG with comparison of 4-bit and 8-bit Vedic multiplier of CSA, CLA and RCA.

Table 1: The comparison values of 4-bit Vedic multiplier and 8-bit Vedic multiplier in CMOS and TG [8].

CMOS		Power	Area	Delay
CSA	4-bit	37.32uw	900	0.4607ns
	8-bit	8.103mw	4832	0.5384ns
CLA	4-bit	1.056mw	1032	0.56317ns
	8-bit	2.633mw	5660	0.5383ns
RCA	4-bit	35.64uw	828	0.4857ns
	8-bit	2.274mw	4436	0.53817ns
TG		**Power**	**Area**	**Delay**
CSA	4-bit	29.62uw	516	0.462ns
	8-bit	0.596mw	2700	42.38ps
CLA	4-bit	0.87mw	1104	37.64ps
	8-bit	0.628mw	6228	70.92ps
RCA	4-bit	26.53uw	444	0.417ns
	8-bit	0.545mw	2268	42.38ps

4. CONCLUSION

8-bit Vedic multiplier using RCA adder, CLA adder and CSA adder in TG and CMOS technique has been compared to find out most suitable one It is to optimize the area, the work has been carried out at high frequency with low power devices irrespective of the cost of power [9]. The area of a vedic multiplier design is an important design metric, as it can affect the cost, performance, and reliability of the circuit as you can see the difference between the delay, average power and area values in the above Table1. About the S-edit used in the Tanner EDA tool when you purchase a new design tool, licensing options can greatly affect your total cost of ownership. S-Edit is available in node-locked and networked configurations offering you the most flexible licensing possible. With a single solution, S-Edit will work whenever and wherever meeting the design needs of your main workgroup and remote workers. If you offshore design projects, S-Edit does not have geographic restriction on its licenses, thus, lowering your total cost of ownership.

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