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Clock Gating Using Energy Efficient Double Edge Triggered Flip Flop For Streaming Applications

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Abstract- This project investigates a promising technique for reducing the power dissipation of streaming applications yielded by asynchronous designs by using double edge triggered flip flop in the respective clock gating technique. With the scaling of technology and need for higher performance, power dissipation is becoming a major bottleneck. Thus, we can achieve power savings by selectively switching off parts of the circuits when they are temporarily inactive. Streaming applications include signal processing, digital media coding, cryptography, video analytics, network routing, packet processing, etc. The CG methodology applied to dataflow designs can be automatically included in the synthesis stage of a high level synthesis design flow. The experimental results show higher reduction in area, frequency and thereby reducing the dynamic power without any loss in data throughput.

***Keywords* —**Clock-gating, low power, high-level synthesis.

1. INTRODUCTION

There are three performance parameters on which a VLSI designer have to optimize the design i.e. Area, Speed and Power. Today's consumer demands more functionality, small size, high speed and optimized power devices. Consumer demands a smaller size battery with longer life. Power dissipation is currently the major limitation of silicon computing devices. Reducing power has also other beneficial effects, it implies less stringent needs for cooling, improved longevity, longer autonomy in the case of battery operated devices and obviously, lower power costs. Power consumed in a digital circuit is of two types. (1) Static power and (2) Dynamic power. Static power consists of power dissipated due to leakage currents whereas dynamic power consists of capacitive switching power and short circuit power.

In VLSI circuit clock signal is used for the synchronization of active components. Clock power is a major component of power mainly because the clock is fed to most of the circuit blocks, and the clock switches every cycle. Thus the total clock power is a substantial component of total power dissipation in a digital circuit [1]. Power dissipation increases linearly with frequency, largely due to the influence of parasitic capacitances. To counteract this effect, ASIC designers have employed *clock gating* (CG) techniques in the last 20 years [2]–[4].Clock-gating is a well known technique to reduce clock power.

Different strategies for optimizing power consumption on ASICs and FPGAs are discussed in Section II. These papers describe the impact of a chosen technology for a given architecture, but do not describe how to reduce power at the design abstraction level. As a consequence, adding power controllers at the behavioral In this CG technique, every actor can concurrently execute processing tasks, executions might be disabled by input blocking reads, and every communications among actors can occur only by means of order preserving lossless queues. As a consequence, an actor may be stopped for a certain period if its processing tasks are idle or its outputs queues (buffers) are full without impacting the overall throughput and semantical behavior of the design.

In a sequential circuit individual blocks usage depends on application, not all the blocks are used simultaneously, giving rise to dynamic power reduction opportunity. By clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit. In clock gating clock is selectively stopped for a portion of circuit which is not performing any active computation [5]

This paper is organized as follows. In Section 2, previous works and literature work on CG are briefly introduced. Section 3 describes in detail the CG strategy and how it is applied on a dataflow design. In Section 4, implementation of clock gating technique on deblocking filter has been shown. In section 5 experimental results are presented and finally the conclusions are drawn in Section 6.

2. RELATED WORK

Dushyant Kumar Sharma has described in detail regarding the Effects of Different Clock Gating Techniques on Design[6]. JiteshShinde and Dr.S.S. Salankar have discussed about Clock Gating –A Power Optimizing Technique for VLSI Circuits [7]. Wuu and Vrudhula [8] and Ghavami and Pedram [9] proposed a method for automatic synthesis of asynchronous digital systems. These two approaches were developed for fine-grained dataflow graphs, where actors are primitives or combinational functions. Dr. Neelam R and Prakash, Akash proposed Clock Gating for Dynamic Power Reduction in Synchronous Circuits and experimental results show are very encouraging in which power reduction has been resulted without any change in the throughput of the design.[10]. Similarly, Related to this paper, Brunet *et al.* proposed a multiple clock, domain-design methodology for reducing the power consumption of dataflow programs. Their design objective was to optimize the mapping of an application while still meeting design performance requirements. This optimization was achieved by assigning each clock domain an optimized clock frequency to reduce power consumption.

3. CLOCK-GATING TECHNIQUE

Clock-Gating [3] is the most common register transfer level (RTL) optimization for reducing dynamic power. In clock gating method, clock is applied only to those modules that are working at that instant. Clock-gating support adds additional logic to the existing asynchronous circuit to prune the clock tree, thus disabling the portions of the circuitry that are not in use. By adopting the clock-gating approach, power dissipation can be reduced significantly, lowering not only the switching activity at the function unit level, but also the switched capacitive load on the clock distribution network[10].

Coarse-Grained CG technique

When the output buffer of any actor is full, the clock of this actor should be turned off as the actor is idle. This is because switching off its clock will not have an impact on design throughput. The queues should be asynchronous for lossless communication when an actor is clock gated and a design has differing input clock domains.

This strategy consists of adding a *clock enabler* circuit for activating the actors' clock. This circuit contains: a controller for each output port queue of each actor, a combinatorial logic for the configuration of the output ports, and a clock buffer (which enables the clock). A representation of an actor with a single output port being clock gated is illustrated in Fig. 1. As depicted, queues are asynchronous. Queues have two input clocks: one for consuming tokens and one for producing them. Additionally, queues have two output ports: 1) *AF* for almost full and 2) *F* for full. The actors input clock is connected to the output of the *clock enabler* circuit. Finally, the clock buffer *BUFGCE* input clock should be connected with a flip-flop for glitch-free CG [13].

The double edge triggered flip-flop will introduce a one-clock latency when the clock is switched off, but this additional clock cycle will not have an impact on actors that are on the critical path. We propose to use the following technique[14] (first time in the data center literature): double edge clock triggering where both the positive and negative clock edges are used to process data. The clock frequency, f, can drop to half which will save processor energy significantly due to equation

P=$\Sigma\ \alpha*C*V2f$.

The key to implement the above methodology is to employ double edge triggered flip flop (DET FF) that can work on both edges of clock instead of using the conventional single edge triggered flip-flop (SET FF). DET flip-flop have not been reported to be used in any processors in servers in data center so far.[14]

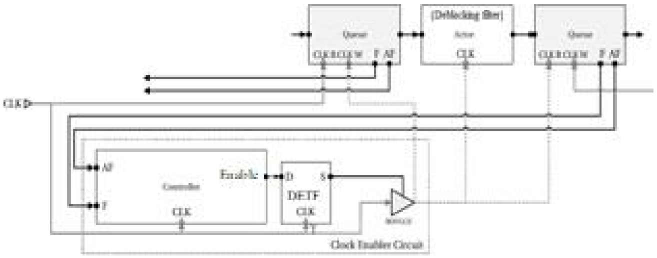


Figure 1.CG technique applied for (deblocking filter) actor.

The actor has two outputs one of those have a fanout of two. The clock enabling circuit takes the *Almost Full* and *Full* signal of each queue and a clock from a clock domain and as a result it is going to activate or deactivate the clock of actor A.

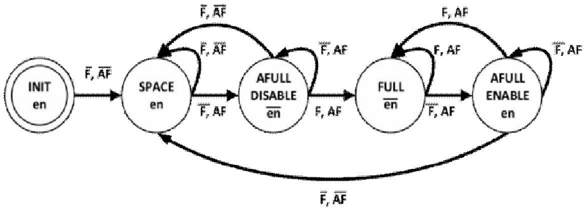


Figure 2: State machine of the clock enabling controller.

The controller has two inputs, *F* for full, *AF* for almost full and an output *en* for enable signal.

1) *Clock Enabling Controller:* The clock enabling controller is represented in Fig. 2. It is implemented as a finite state machine having a clock; a reset; input *F*, for full; input *AF*, for almost full; and output *EN*, for enable. The *AF* input becomes active high when there is only one space left on its FIFO Queue. Its FSM has five states *S* = {*INIT*, *SPACE*,*AFULL_DISABLE*,*FULL*, *AFULL_ENABLE*}. The controller starts with the *INIT* state and maintains the *EN* output port at active high until *F* and *AF* become active low.

Algorithm for clock enabling circuit.

***Step1*:** Initialize en=1. when F=0,AF=0;
***Step2**:* Now queue has empty space. Wait with en=1 until AF=1.If AF=1 go to next state.
Step3: Now CG-circuit ready to give en=0.
If AF=0 again go to step2.
Else if AF=1,F=0 be in the same state.
Else F=1, AF=1 go to next state.
Step4: Now queue is in full state so, disable clk input to actor by asserting en=0;

Step5: Wait until F=0;
If AF=1,F=1 be in the same state. Else ***Step5***
F=0,AF=1 go to next state;
Step6 : Now queue is in almost full state en=1;
If F=0, AF=0 queue has empty space then goto step2; Else if F=1,AF=1 goto step5.

2) Strategy: The user can make a choice of mapping configuration that shows which actor should be clock gated. If an actor has been selected for CG, all of its Outputs queues, F and AF, are connected to a clock enabler controller. Output can be connected through a fanout or directly to a queue. In the first case, the controller outputs are connected to an AND logic port. This is a safe approach in the case where if any one of the queues in the fanout is full it should command the actor not to produce a token. For the latter case, if an actor's output is connected directly to a queue without a fanout, the result should be any one of the queues in the fanout is full it should command the actor not to produce a token. For the any one of the queues in the fanout is full it should command the actor not to produce a token.

For the latter case, if an actor's output is connected directly to a queue without a fanout, the result should be connected to an OR logic port as the next actor may need to consume a certain number of data to output a data. This may lead the system to lock due to the unavailability of data. In the third case, if there is a combination of outputs with or without a fanout, then an *n*-input OR logic port is inserted. Fig. 3 depicts these configurations.

A DETFF is connected between the *BUFGCE* and the final OR or AND port. Thus, clock glitches are eliminated and the clock enabling is run free. The last output of the CG is a new clock that is connected to the actors, its fanouts, and its queues' write and read clocks (CLK W and CLK R, respectively) as visualized in Fig1.

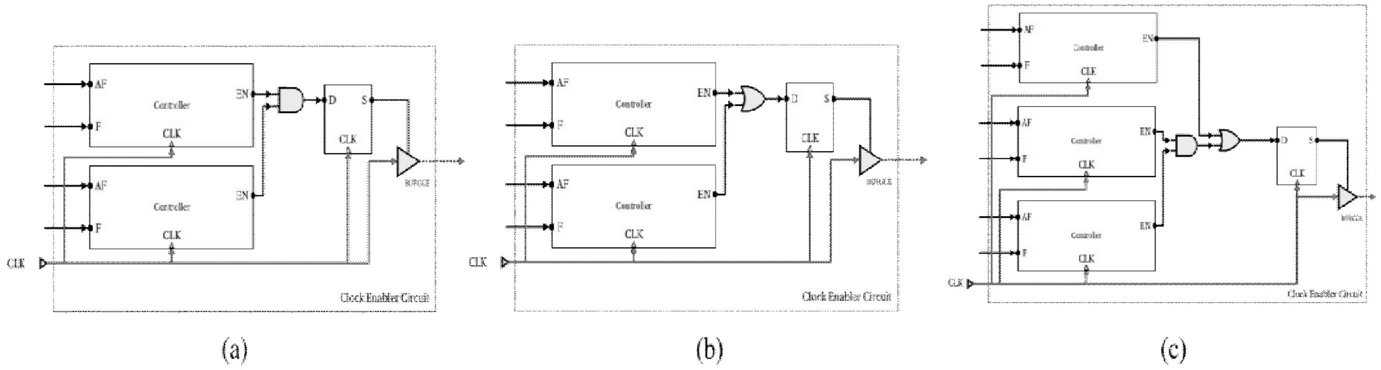


Figure 3: Clock enabler circuit in different configurations. (a) Single output port with a fanout. (b) Two different output ports. (c) Single output port with a fanout and another output port.

4. IMPLEMENTATION OF CLOCK GATING TECHNIQUE ON DEBLOCKING FILTER

Deblocking filter is the heart of MPEG Simple profile decoder and one of the major components of it. Deblocking filter is a video filter applied to the decoded compressed video to improve the visual quality edges and smoothen the blocking artifacts which tend to occur at the block boundaries because of lossy compression introduced by quantization [15]. The block diagram of deblocking filter is shown in Fig.4.

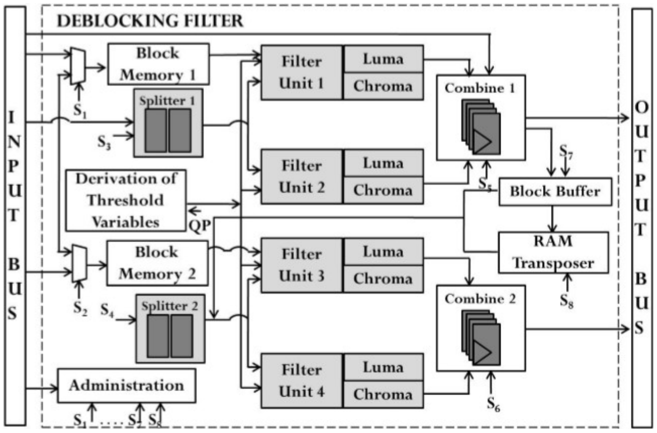


Figure 4: Block diagram of Deblocking filter.

There are five main components in this architecture[15].

1. *Block memories*: to store the data received from an external memory
   a. Block memory 1- stores the left neighbor block (E1-E8)
   b. Block memory 2- stores the top neighbor block (F1-F8)
2. *Filter unit:* includes two horizontal filters and two vertical filters
   a. Filter unit 1 and filter unit 2- two horizontal filter modules (HF1 and HF2)
   b. Filter unit 3 and filter unit 4- two vertical filter modules (VF3 and VF4)
3. *Derivation of threshold variables*: generates the threshold variables β and tc.
4. *Splitter*: divides the coding block into two parts to be transferred to filter modules.
5. *Combine*: merge into original coding block and transferred to block buffer.

Clock gating technique on deblocking filter

In this paper the clock gating technique is used to achieve low power dissipation. The deblocking filter is implemented using this technique.

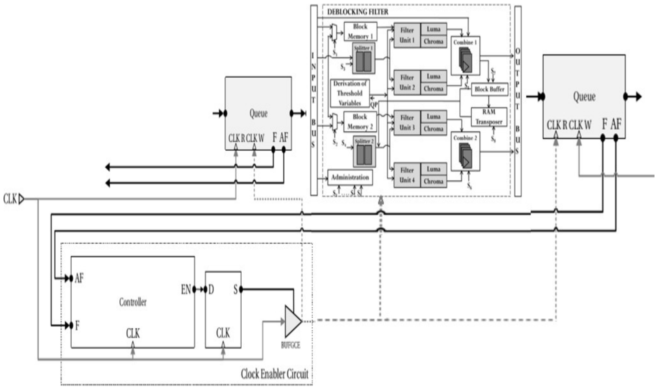


Figure 5: Clock gating technique applied to deblocking filter

When the output buffer of deblocking filter is full, the clock of this filter should be turned off as the actor is idle. This is because switching off its clock will not have an impact on design throughput. Queues have two input clocks: one for consuming data and one for producing them and two output ports: 1) *AF* for almost full and 2) *F* for full. The deblocking filter indicates AF when there is one space left in the queue. In the absence of clock gating technique when the actor won’t be able to indicate that the buffer is full, over writing of data might also take place.

The filter’s input clock is connected to the output of the *clock enabler* circuit. Finally, the clock buffer *BUFGCE* input clock should be connected with a double edge triggered flip-flop for glitch-free clock gating.

The double edge triggered flip-flop[14] will help in high data rate transmission and also reduces the frequency to half thereby reducing the power dissipation of the circuit.

There are three different configuration by which the actor can be clock gated and it is depicted in figure 3.

5.EXPERIMENTAL RESULTS

In this section, the power reduction gain, area utilization and frequency reduction of the aforementioned methodology is evaluated by applying it to a deblocking filter.

A. Experimental Flow

The HDL code of the decoder was generated and synthesized with the Xilinx XST synthesizer. Following synthesis, placings applied to produce a final netlist.

TABLE I
Logic utilsation of deblocking filter with and without clock gating

Logic utilization	Non clock gating	Clock gating	Available
No. of slices	274	35	4656
No. of slice flip flop	463	56	9312
No. of LUT's	242	24	9312
No. of bonded IOB's	125	50	232
No. of GCLK's	1	1	24

This netlist was then simulated with Modelsim to extract the switching activity information (SAIF file) of the design. The Xilinx XPower analyser was then used to determine power consumption, using the design netlist, the design constraints, and the simulation activity SAIF as inputs. Also, all of the results given have a high confidence level meaning that at least 97% of the design nets are found within the SAIF file. Table I shows the logic utilization of deblocking filter with and without CG. This example demonstrates that the clock gated decoder uses more slices than the nonclock gated one. The number of slices, sliced flipflops,LUT, bonded IOB's and gated clocks have been reduced significantly in clock gating when compared to non clock gating circuit. A 120 MHz clock has been given as a synthesis constraint.

Table II depicts the parameter comparison of deblocking filter using clock gating technique and clock gating using double edge triggered flipflop technique. Dealy, area and frequency are compared and resulted in a tremendous decrease in frequency which proves that the power dissipation has been decreased.

TABLE II
Parameter comparison of the deblocking filter
Representing delay area and frequency

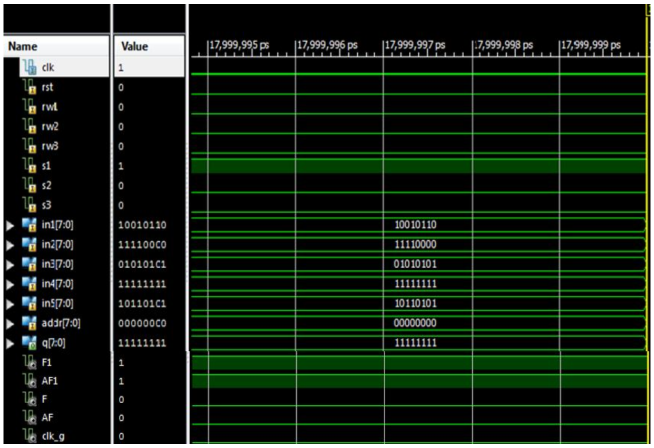
Parameters	Using clock gating technique	Clock gating technique using double edge triggered flip flop
Delay	6.20 ns	8.73 ns
Frequency	161.29 MHz	119.43 MHz
Area (LUT's)	56/9312	73/9312

TABLE III
Power consumption of the deblocking filter when the CG is disabled/enabled

Clock Gating	Disabled (mW)	Enabled (mW)
Actors clocks	59	40
Clocks	90	78
Logic	28	25
Signals	45	42
Leakage	242	242
Total	464	427

Table III depicts the power consumption of the deblocking filter when the clock gating technique is disabled or enabled. The difference of 37mw has been observed.

B. Simulation Results



Name	Value
clk	1
rst	0
rw1	0
rw2	0
rw3	0
s1	1
s2	0
s3	0
in1[7:0]	10010110
in2[7:0]	111100C0
in3[7:0]	010101C1
in4[7:0]	11111111
in5[7:0]	101101C1
addr[7:0]	000000C0
q[7:0]	11111111
F1	1
AF1	1
F	0
AF	0
clk_g	0

The simulation result for the deblocking filter to which clock gating has been applied states that when F (Full) and AF(almost full) signal of the queue is 0 i.e when the queue is empty andalso when the F1 and AF1 of the next queue is 1 i.e when the next queue is completely full then there is no need to clock the actor (Deblocking filter) to avoid the unnecessary switching of flipflops and thus the gated clock is disabled i.e clk_g is 0. Hence this shows that when the buffer is empty or completely filled then clock is not given and this stops the circuit from switching and avoids the dissipation of power.

6. CONCLUSION

This paper presents a CG methodology applied to dataflow designs that can be automatically included in the synthesis stage of an HLS design flow. In clock gating method, clock is applied only to those modules that are working at that instant. Clock-gating support adds additional logic to the existing synchronous circuit to prune the clock tree, thus disabling the portions of the circuitry that are not in use. By adopting the clock-gating approach, power dissipation can be reduced significantly, lowering not only the switching activity at the function unit level, but also the switched capacitive load on the clock distribution network. The application of the clock gating technique is independent from the sematic of application and does not need any additional step or effort during the “design” of the application. The CG logic is generated during the synthesis stage together with the synthesis of the computational kernels connected via FIFO queues constituting the dataflow network.

Experimental results show savings in power dissipation with a slight increase in control logic without any reduction in throughput have been achieved. The overall frequency has been decreased thereby reducing the power dissipation of the circuit. Clock gating technique is helpful in situations where the design is not used to its full capacity. In these circumstances Clock gating is a simple and effective technique to recover power otherwise lost in “idle” cycles. As a result, this technique is particularly interesting in applications with dynamically varying performance requirements and when power consumption is deemed costly.

It will be necessary to develop tools that partition complex applications onto the limited number of clock domains for more efficient implementations. Lastly, additional considerations could be given to controlling clock speed and, possibly, voltage transitions. Further investigations into CG should consider more aggressive control logic, whereby control is given to each individual actor, allowing greater flexibility to actor inactivity.

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