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# Use of Open Source CAD Tools in VLSI Design Curriculum for Developing Countries

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***Abstract*— VLSI design education has a critical role in producing a skilled manpower required for semiconductor industry especially in developing nations. The disparity between the education provided in developing nations and developed nations is due to lack of basic infrastructure which includes hardware equipment and computer aided design tools. These tools are vital in VLSI design cycle at every step from design specifications to the tape out. This paper envisages a framework for imparting VLSI education using open source VLSI CAD tools. The framework includes the hardware requirement, description of courses and sample project. The universities in developing nations can follow this framework for transforming students into skilled manpower.**

**Keywords— VLSI, education, EDA, CAD tool**

## I. INTRODUCTION

In the past decade, semiconductor industry is progressing tremendously. Consumer electronics market is growing day by day with innovation in products offering huge range to consumers. New products with better performance and lower cost are flooding the market due to microelectronics revolution. The size of transistors is constantly shrinking so as to integrate more number of transistors into same chip area with more functionality. To cope up with the demand, semiconductor industry is becoming increasingly specialized where an ecosystem of companies with competitive niche capabilities are responsible for the development and delivery of product. A large number of skilled VLSI engineers are required at every phase of product cycle. Developing nations can grab this opportunity by creating a skilled manpower equipped with new technologies. To achieve this target, well established academia is required. Educational institutions must train them with fundamentals along with the exposure to CAD tools [1-4] so that fit along the industry standards well. As this industry is fast changing to accomplish this is a huge task as faced by academicians to keep pace along with industry.

CAD tools offered by vendors are enormously expensive. Most of the universities in developing countries don't have such funding to purchase such tools. A costly dedicated hardware along with various OS platforms is required to keep running these tools. The hardware needs to be updated after few months as these tools are evolving rapidly. Dedicated manpower is required to handle the administration of such facility which too doesn't come cheaply. This escalates not only purchasing cost but also the running cost for these CAD tools. Moreover, legal agreements between the CAD tool vendor and academic institution makes the whole process complex and lengthy (Elias) [5-6]. It may take several months to furnish the legal formalities to acquire the CAD tools. Annual renewal of licenses of CAD tools along with the license of OS in which these tools are stationed ads to the cost. Some of the companies don't offer support in their offer to academic institutions. Students suffer mostly due to lack of support and discerning distribution policies. Specialized nature of tools provided by commercial CAD vendors are primarily for industry use. However, some tools offers a lot more than needed for basics in academics due to complex nature [7-10].

These problems stated above can be resolved if students are equipped with CAD tools in their personal computers without the hassle of purchasing or renewing license. The free open source tools can be used for academic purpose owing to their usability. Open source tools are available on the web where students can download and install them as per their requirement.

In this paper, an alternative approach VLSI design education is presented as a solution for developing countries.

## II. HARDWARE REQUIREMENTS

CAD vendors have economic concerns as their priority and may not be able to support students with integrated design flows [11-15]. There is gap that exists between course and implementation with EDA tools within academic research because of ever increasing advancements in VLSI technology. The parameters kept evolving in sub-nanometer regime. This variation within a VLSI design complicates traditional approaches teaching and researching designs targeted at the nanometer level. The required to equip themselves with the knowledge above and beyond design for nanometer regime. Special emphasis is required for the designs at nanometer regime. In other words, because nanometer VLSI design flows require an extensive amount of knowledge to create and maintain [16-17] , they become an impediment to properly researching cutting-edge designs. More importantly, it allows teachers and students the valuable specifics related to the theory of nanometer design and allow them to integrate them into an actual design.

A dedicated VLSI lab requires expensive hardware including workstations which stations various CAD tools. However, with the cost of PCs decreasing nowadays computing power more accessible to students. The students can install and simulate the free CAD tools in their low priced PCs. Dual boot mode provides freedom to install OS simultaneously in a single PC.

## III. COURSEWORK REQUIREMENTS

The students after completion of courses shall be able to design and analyze both digital and analog CMOS circuits. They must be able to make and analyze layout of digital and analog designs and show proficiency in writing and synthesizing code. The designs should be extracted in global format to be able to send to foundry/fabrication.

The term design flow refers to set of operations sequentially implemented while designing a circuit. The design flow starts with design specifications and transistor level description of design. The designer should be able to identify characteristics and working of circuit. The analog circuit simulation is done afterwards for functionality verification.

Not much infrastructure is required for implementing this course. Just few personal computers would be sufficient for installing the CAD software [12]. Mutual benefits to faculty and students as a whole upon developing sustainable infrastructure like VLSI department will be as follows:

1) Students shall be able to conduct research with higher impact.

2) Due to higher level of industry interaction, upliftment of research, development, training and review is expected.

3) Pool of skilled manpower will be generated in the area of VLSI.

4) With the generation of skilled manpower, industry will be able to produce low cost consumer electronics products for the nation to strengthen its economy.

By developing the appropriate workforce of the 21st century for the semiconductor industry, detailed knowledge must be acquired by students not only in design, but also in mask fabrication and wafer processing technologies.

## IV. TOOL REQUIREMENTS

Many free CAD tools are available online for academic use. Tools choice is critical for the design flow. While some tools are readily integrated in design flow, other tools output format may not match with others. Should be able to deliver understanding of design and concepts in VLSI. Basic features needed in VLSI design tool are logical design, circuit schematic design, layout generation, and design check.

Major motivation for EDA tools in semiconductor industry is cost effective and efficient development of IC fabrication technology using device CAD to analyze the device performance and process CAD to input realistic structural information from process flow to device. It offers to analyze how structural factors such as geometry and process conditions influence the electrical behavior of device and circuits. Simulation data helps in quantifying the details physical limitations.

### *A. Electric tool*

An Electric tool [3] was developed by Steven Rubin with the support of Sun Microsystem Laboratories. It is developed in Java language with latest version 9.05. This tool is based on connectivity of circuit design as compared to other tools which are both geometry and connectivity based. It considers the electric elements as nodes and the connecting wires as arcs. This offers several advantages. There is no need for node extraction therefore simulation is more speedy, no geometry errors as geometry method is not used and LVS on layouts can be performed prior to DRC. Also, layout and schematic can be finished in one interface. However the user must be good in connectivity while designing. Any wrongly connected circuit is hard to find on screen.

### *B. Alliance tool*

Alliance [2] is a bundle of tools written in C language developed by MASI laboratory of the Pierre Marie Curie University for design, layout and validation of digital circuits. Its tools are command line based and can be run independently unlike Electric which has integrated interface. It supports various formats e.g. SPICE, VHDL, CIF, EDIF and GDS2.It also have a large set of own cell libraries at layout level which makes it process independent. The Alliance's design flow follows top-down Mead-Conway model which includes behavioral view simulation, structural view validation, and physical design, verification, and test coverage evaluation. The tools can be easily installed on Unix OS. With the documentation available on-line, these tools can be easily used.

### *C. SUPREM tool*

SUPREM is developed by Stanford university in 1977 as 1D process simulator [4]. Latest SUPREM IV supports 2D process simulation. SUPREM allows designer to simulate a full technology process sequence. The program inputs specifies the temperature, ambients, implants and other process specifications. We can get the impurity distribution in each layer and other electrical data as an output from the simulator. It provides semiconductor devices cross section based on physical models [TCAD SUPREM]. It has inbuilt dopant models for Si, Se, Ge and Sn, Be, Mg, Zn and C which supports GaAs process along with Si process technology also. Oxidation, diffusion, ion implantation, epitaxy, diffusion, predeposition, etching, CVD processes are supported.

Beside the CAD tools mentioned above, there are many other CAD tools that can be found, though they are not as popular as the three former ones. Some of them are still in development and cannot be used as tools for the whole work flow. These tools have their own features and some of them really worth mentioning here.

## V. RESULTS

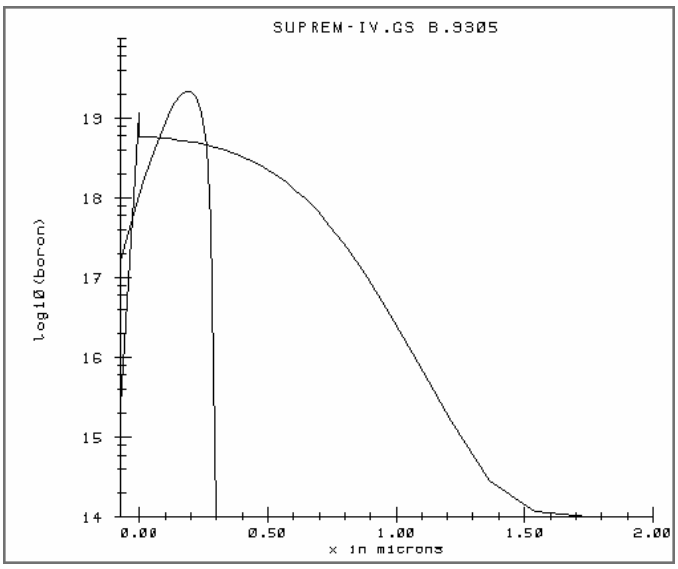


Fig. 1. SUPREM simulation example

The students should be skillful at basic theory, principles and knowledge of IC design and application with integrated circuit design tools. The students can engage in research, design, and application of IC chips and electronic information systems with some innovation ability of engineering and technique. It is expected that this will help the students in gaining a better understanding of both the constituent processes and the global picture of VLSI manufacturing.

### *A. Integrated Circuit fabrication course*

This course stresses manufacturing aspect in the area of electronic and photonic materials and devices. The idea is to introduce students at an early stage to the complexities and challenges associated with VLSI chip fabrication. This course introduces to the manufacturing aspect of semiconductor devices in electronics industry. Complementary Metal Oxide Silicon (CMOS) process technology concentrating on the various processes used to fabricate semiconductor devices. As the CMOS technology is predominantly used in semiconductor industry, this course emphasizes the study of theory and physical design of devices. The basic knowledge about the physics of semiconductors is a prerequisite to this course. This course also exposes fairly students to CMOS and bipolar technologies. The level of depth helps the students understand the limitations of the technology. The course starts with the basics of semiconductor ICs and microelectronic technology. This is followed by introduction to silicon wafers and the clean room environment for their fabrication. Basic CMOS processes (oxidation, diffusion, photolithography, etching, ion implantation and film deposition) are illustrated followed by description of each process in larger detail. Other advanced processes are also introduced which are necessary to make integration of devices more effective. Physics and chemistry involved in each process is studied in detail. Various packaging types are illustrated. SUPREM is used along the course for the demonstration of different process.

This sample project discusses the annealing of boron implant. To run a simulation in SUPREM, the input file should contain initialize statements, materials statements, process statements and output statements. The input file defines the mesh area to be simulated. The starting material (Si in our case) is described by using "region" statement. The "bound" statement defines the surface of wafer which is exposed to gas. Next, pad oxide is added to wafer followed by the implantation of boron. The implant is modeled with distribution type and is then plotted. Then "diffuse" command simulates the anneal according to given environment. The output is read by "structure" command.

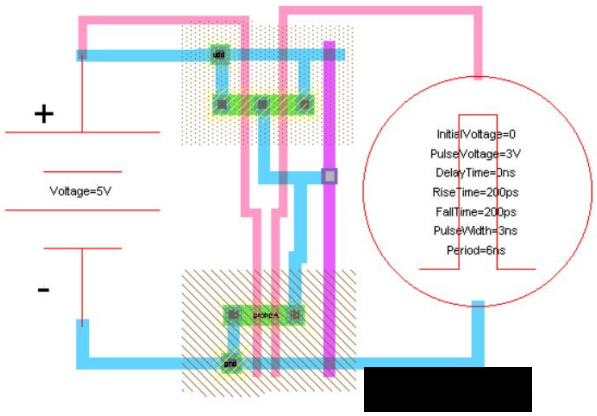


Fig 2. Electric tool simulation example

Figure 2 shows the spice simulation example from the electric tool. Figure 3 describes the output of the circuit simulated in the tool with the help of waveform.

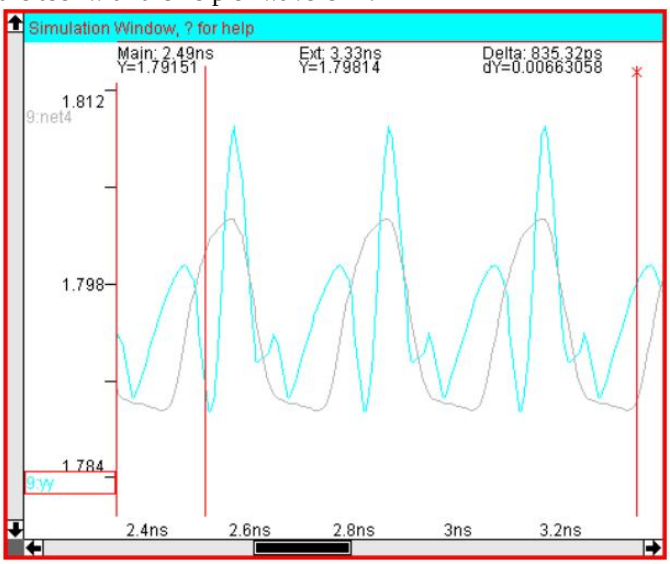


Fig 3. Waveform of the simulated layout in Electric tool.

Students often use Microwind layout editor more than LTSpice schematic editor. Great emphasis is given on layout drawing techniques, which are essential in minimizing the area of circuit, thus, reducing parasitic resistance and capacitance. Design rule check (DRC) is then performed to ensure that the layout is free layout violations. In the assignment, students were instructed to draw layout of various

designs from several circuit families, ranging from static CMOS to domino logic. Even the group project requires the student to master the art of drawing layout of a medium-scaled design.

Students are expected to spend considerable non-scheduled lecture time in this project. At the end of the Project, students need to present a report which contains design methodologies, schematics, simulation results and discussions. The successful resolution of a problem is a good exercise of knowledge, astuteness and intuition and gives the students useful information and skill to understand and to estimate the size of future designs. Solid foundation in VLSI design with an amount of detail and practice that will enable students to productively do design, and a breath of the subject matter that spans silicon process technology, digital and analog design, as well as system issues. The goal is to provide student with powerful learning experiences that they can easily transfer to a future workplace.

## VI. CONCLUSION

A framework is demonstrated for implementing VLSI design curriculum using free open CAD tools. A sample project based on “IC fabrication” course is discussed using SUPREM tool. . This shall help the student to learn different operations involved in transforming silicon wafer into an integrated circuit. Also, the students shall gain experience in the modeling and simulation of semiconductor manufacturing processes. Other courses can also be taught along with the use of open source CAD tools. Our overall objective is to demonstrate that high quality undergraduate education in VLSI is possible with open source free tools and should be encouraged as part of the training that is expected of modern engineering curricula.

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