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AC–DC Converter with High Power Factor and High Efficiency

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***Abstract*—This paper proposes a single power-conversion ac–dc converter with high power factor and high efficiency. The proposed converter is derived by integrating a full-bridge diode rectifier and a series-resonant active-clamp dc–dc converter. To obtain a high power factor without a power factor correction circuit, this pa-per proposes a novel control algorithm. The proposed converter provides single power-conversion by using the novel control algo-rithm for both power factor correction and output control. Also, the active-clamp circuit clamps the surge voltage of switches and recycles the energy stored in the leakage inductance of the trans-former. Moreover, it provides zero-voltage turn-on switching of the switches. Also, a series-resonant circuit of the output-voltage dou-bler removes the reverse-recovery problem of the output diodes. The proposed converter provides maximum power factor 0.995 and maximum efficiency of 95.1% at the full load. The operation principle of the converter is analyzed and verified. Experimental results for a 400 W ac–dc converter at a constant switching fre-quency of 50 kHz are obtained to show the performance of the proposed converter.**

***Index Terms*—Active-clamp circuit, series-resonant circuit, sin-gle power-conversion.**

I. INTRODUCTION

The PFC ac–dc converter can be implemented by using two power-processing stages. The PFC input stage is used to obtain high power factor while maintaining a constant dc-link voltage. Most PFC circuits employ the boost converter [9]–[15]. The output stage, which is a high frequency dc–dc converter, gives a desired output. Two power-processing stages require each control circuit consisting of gate drivers and those controllers.

In general, the PFC ac–dc converter can be categorized into two types: two-stage ac–dc converters [16], [17] and single-stage ac–dc converters [18]–[27]. Two-stage ac–dc convert-ers consist of two power-processing stages with their respec-tive control circuits. However, two-stage ac–dc converters raise power losses and the manufacturing cost, eventually reducing the system efficiency and the price competitiveness. In efforts to reduce the component count, the size, and the cost, a num-ber of single-stage ac–dc converters have been proposed and developed. The main idea is that a PFC input stage and a high frequency dc–dc converter are simplified by sharing common switches so that the PFC controller, the PFC switch, and its gate driver can be eliminated. Most single-stage ac–dc converters in low-power application employ single-switch dc–dc converters such as flyback or forward converters [20]–[23]. These con-verters are simple and cost-effective. However, they have high switching power losses because of the hard-switching operation of the power switch. Thus, to overcome the drawback, single-stage ac–dc converters based on the asymmetrical pulsewidth modulation (APWM) half-bridge converter have been proposed in [24]–[27]. They have low switching losses because of the zero-voltage switching (ZVS) operation of the power switches. However, the conventional single-stage ac–dc converters have high voltage stresses or a low power factor in comparison with the two-stage ac–dc converter. Also, the PFC circuit used in the single-stage ac–dc converter requires the dc-link electrolytic ca-pacitor and the inductor. The dc-link electrolytic capacitor and the inductor raise the size and the cost of the converter.

To solve these problems, the dc-link electrolytic capacitor should be removed from the circuits. The approach of achieving this is through the alleviation of the pulsating component of the input power by sacrificing the input power factor [28], [29]. The main idea is to intentionally distort the input current such that there is little low-frequency power-ripple component being generated at the input. Consequently, nonelectrolytic capacitors such as film capacitors or ceramic capacitors can be used in-stead of electrolytic capacitors. This approach is mostly applied to single-switch PFC ac–dc converters. Compared to the con-ventional single-stage ac–dc converters with the dc-link elec-trolytic capacitor, the converters using this approach are small and cost-effective; on the other hand, they have drawbacks such as low power factor and low efficiency because of the discon-tinuous current mode (DCM) operation and the hard-switching operation. Therefore, these converters are attractive in low-cost and low-power application such as a light-emitting diode (LED) power supply.

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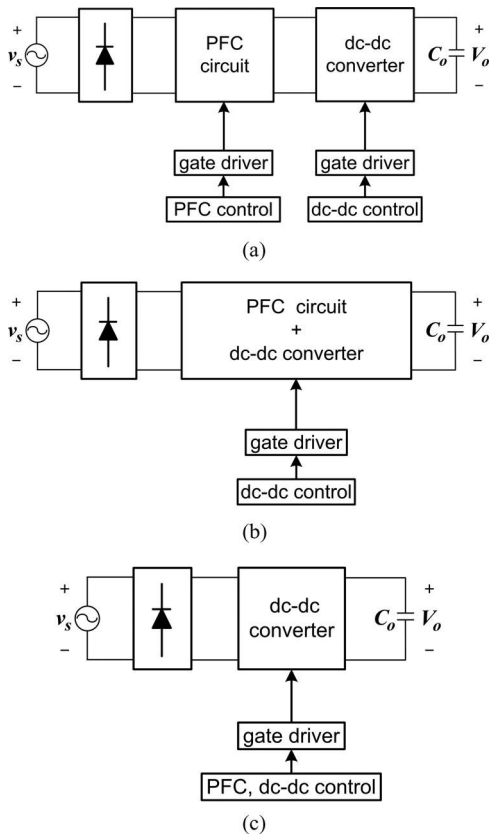

Fig. 1. Block diagrams of the conventional PFC converters and the proposed converter. (a) Two-stage converter. (b) Single-stage converter. (c) Single power-conversion converter.

In view of this, the objective of this paper is to propose the single power-conversion ac–dc converter with the high power factor and the high power efficiency. The proposed converter is composed of a full-bridge diode rectifier and a series-resonant active-clamp dc–dc converter. The proposed converter provides a simple structure, a low cost, and low voltage stresses because it has only high frequency dc–dc converter. To obtain high power factor without a PFC stage, a novel control algorithm is proposed. The proposed converter provides high power factor and single power-conversion by using the novel control algorithm instead of the PFC circuit. Also, the active-clamp circuit clamps the surge voltage of switches and recycles the energy stored in the leakage inductance of the transformer. Moreover, it provides ZVS operation of the switches. Also, a series-resonant circuit of the output-voltage doubler removes the reverse-recovery problem of the output diodes by zero-current switching (ZCS) operation. The design guidelines for the proposed converter are discussed and experimental results are obtained to show the performance of the proposed converter.

II. Characteristics and Operation Principle of the Proposed AC–DC Converter

A. Concept of the Single Power-Conversion AC–DC Converter

Fig. 1(a) shows the schematic diagram of the conventional two-stage ac–dc converter. It comprises a full-bridge diode rectifier, a PFC circuit, a control circuit for the PFC circuit, a high frequency dc–dc converter, and a control circuit for output control. The control circuit is composed of gate-drivers and a controller. Namely, two-stage ac–dc converters have two power-processing stages with their respective control circuits. Also, the boost type PFC converter used in most PFC input stages requires the dc-link electrolytic capacitor and the inductor. Two control circuits, the dc-link capacitor and the inductor raise the size, weight and the cost of the converter and reduce the price competitiveness. On the other hand, the advantage is to decouple control of the dc-link capacitor voltage from that of the output voltage and realize much tighter output control. Therefore, two-stage ac–dc converters are preferred option when reliability is more important concerns than cost per unit. Fig. 1(b) shows the schematic diagram of the conventional single-stage ac–dc converter. It comprises a full-bridge diode rectifier, a PFC circuit, a high frequency dc–dc converter, and a control circuit for output control. The PFC circuit and the high frequency dc–dc converter are simplified by sharing common switches for eliminating the PFC switch and the control circuit for the PFC circuit as shown in Fig. 1(b). That is, single-stage ac–dc converters have only one control circuit. Thus, the output voltage is easily regulated by a controller and the power factor is strongly influenced by the design of the PFC circuit. However, single-stage ac–dc converters have several disadvantages. First, the power factor is also related to the controller, indicating that the variation of the load or the input voltage will change the power factor. Second, the output voltage control bandwidth is limited to a few hertz not to excessively distort the input current. Third, single-stage ac– dc converters require the dc-link electrolytic capacitor and the inductor for the PFC circuit, just like two-stage converters. Finally, the conventional single-stage ac–dc converters have high voltage stresses or low power factor in comparison with two-stage ac–dc converters. Fig. 1(c) shows the schematic diagram of the single power-conversion ac–dc converter. It consists of a full-bridge diode rectifier, a high frequency dc–dc converter, and a control circuit. That is, the single power-conversion ac–dc converter has also one control circuit because it has no PFC circuit. However, it requires the control algorithm for both PFC and output control, unlike single-stage ac–dc converters. Also, it has a large ac second-harmonic ripple component reflected at the output voltage in comparison with two-stage and single-stage converters because it has no dc-link electrolytic capacitor. However, the single power-conversion ac–dc converter provides a simple structure, a low cost, and low voltage stresses because it has no PFC circuit composed of the inductor, power switching devices and the dc-link electrolytic capacitor. Therefore, the single power-conversion ac–dc converter is preferred option when the cost per unit is more important concerns than reliability.

B. Operation Principle of the Proposed Circuit

Fig. 2 shows the proposed single power-conversion ac–dc converter and the control block diagram. The high frequency dc–dc converter [30], [31] used in the proposed converter com-bines an active-clamp circuit and a series-resonant circuit across the power transformer T . The active-clamp circuit is composed

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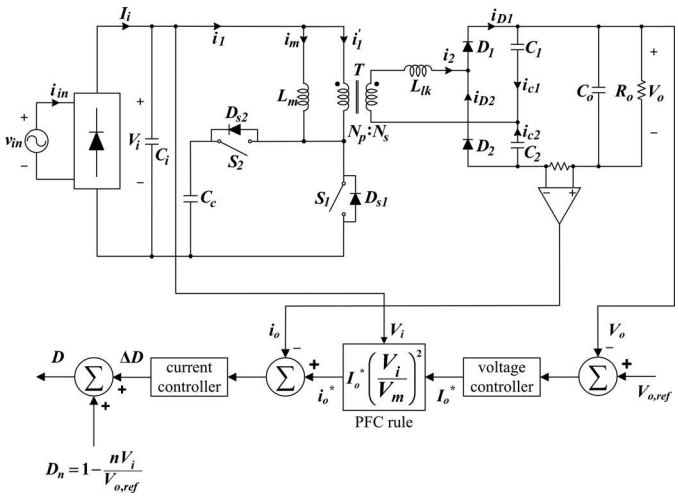

Fig. 2. Proposed single power-conversion ac–dc converter and the control block diagram.

of a main switch S_1 , an auxiliary switch S_2 , and a clamp capacitor C_c . The switch S_1 is modulated with a duty ratio D and the switch S_2 is complementary to S_1 with a short dead time. The active-clamp circuit serves to clamp the voltage spike across S_1 and to recycle the energy stored in the leakage inductance of the transformer T . Also, it provides ZVS turn-on of S_1 and S_2 . The series-resonant circuit is composed of the transformer leakage inductance L_{lk} , the resonant capacitors C_1 , C_2 , and the output diodes D_1 , D_2 and provides ZCS turn-off of the D_1 and D_2 .

In order to analyze the operation principle, several assumptions are made during one switching period T_S :

1) the switches S_1 and S_2 are ideal except for their body diodes D_1 , D_2 and capacitances C_1 , C_2 ;
2) the input voltage v_{in} is considered to be constant because one switching period T_s is much shorter than the period of v_{in} ;
3) the output voltage V_o is constant because the capacitance of the output capacitor C_o is sufficiently large, similarly, C_c is sufficiently large that is voltage ripple is negligible. Thus, the clamp capacitor voltage V_c is constant;
4) the power transformer T is modeled by an ideal trans-former with the magnetizing inductance L_m connected in parallel with the primary winding N_p , and the leakage inductance L_{lk} connected in series with the secondary winding N_s .

The steady-state operation of the proposed converter includes six modes in one switching period T_s . The operating modes and theoretical waveforms of the input side and the output side are shown in Figs. 3 and 4, respectively. The rectified input voltage V_i is $|v_{in}| = |V_m \sin\omega t|$, where V_m is the amplitude of the input voltage and ω is the angular frequency of the input voltage. Prior to Mode 1, the primary current i_1 is a negative direction and the secondary current i_2 is zero.

Mode 1 [t_0 , t_1]: At the time t_0 , the voltage v_{s1} across S_1 becomes zero and D_{s1} begins to conduct power. After the time t_0 , S_1 is turned on. Since i_1 started flowing through D_{s1} before S_1 was turned on, S_1 achieves the ZVS turn-on. As shown in Fig. 4(a), since V_i is approximately constant for a switching period T_s , the magnetizing current i_m increases linearly with the following slope:

$$\frac{di_m}{dt} = \frac{V_i}{L_m} . \quad (1)$$

During this interval, the input power is directly transferred to the output stage of the transformer. The difference between i_1 and i_m is reflected to the secondary current i_2 . The secondary winding voltage v_2 is

$$v_2 = nV_i \quad (2)$$

where the turns ratio n of the transformer is given by N_s / N_p . Since C_o is sufficiently large, the resonant equivalent capaci-tance C_r is $(C_1 + C_2)$. Thus, D_1 is conducting and L_{lk} res-onates with C_r while the secondary current i_2 flows. The state equations of the series-resonant circuit can be written as follows:

$$L_{lk}\frac{di_2}{dt} = nV_i - v_{C1} \quad (3)$$

$$i_2 = C_r \frac{dv_{C1}(t)}{dt} . \quad (4)$$

Here, i_2 is obtained as follows:

$$i(t) = \frac{1}{Z_r}\sin\omega_r(t - t_0) \quad (5)$$

where V_{C1} is the average voltage of C_1 . Also, the angular res-onant frequency ω_r and the resonant impedance Z_r are given by

$$\omega_r = \frac{1}{\sqrt{L_{lk}C_r}} \qquad Z_r = \sqrt{\frac{L_{lk}}{C_r}}$$

As can be seen in Fig. 4(a), i_1 increased by the first series resonance is calculated as follows:

$$i_1(t) = i_m(t_0) + \frac{V_i}{L_m}(t - t_0) + \frac{n^2V_i - nV_{C1}}{Z_r}\sin\omega_r(t - t_0). \quad (7)$$

As shown in Fig. 4(b), the output current i_o becomes half of the output diode current i_{D1} by the resonant capacitors C_1 and C_2 as follows:

$$i_o(t) = i_2(t) - i_{C1}(t) = \frac{1}{2}i_{D1}(t). \quad (8)$$

Mode 2 [t_1 , t_2]: At the time t_1 , i_1 changes its direction to positive. L_{lk} and C_r still resonate similar to Mode1.

Mode 3 [t_2 , t_3]: At the time t_2 , i_2 becomes zero and D_1 is maintained in the on-state with the zero current. I_1 and i_m are equal during this interval. Therefore, i_1 terminates the first resonance and increases linearly as (1).

Mode 4 [t_3 , t_4]: At the time t_3 , S_1 is turned off and D_1 is turned off with the zero current. The ZCS turn-off of D_1 removes its reverse-recovery problem. The voltage v_{s2} across S_2 becomes zero and the body diode D_{s2} begins to conduct power. After the time t_3 , the ZVS turn-on of the auxiliary switch S_2 is achieved. Since the clamp voltages V_c is approximately constant during a switching period T_s , i_m decreases linearly

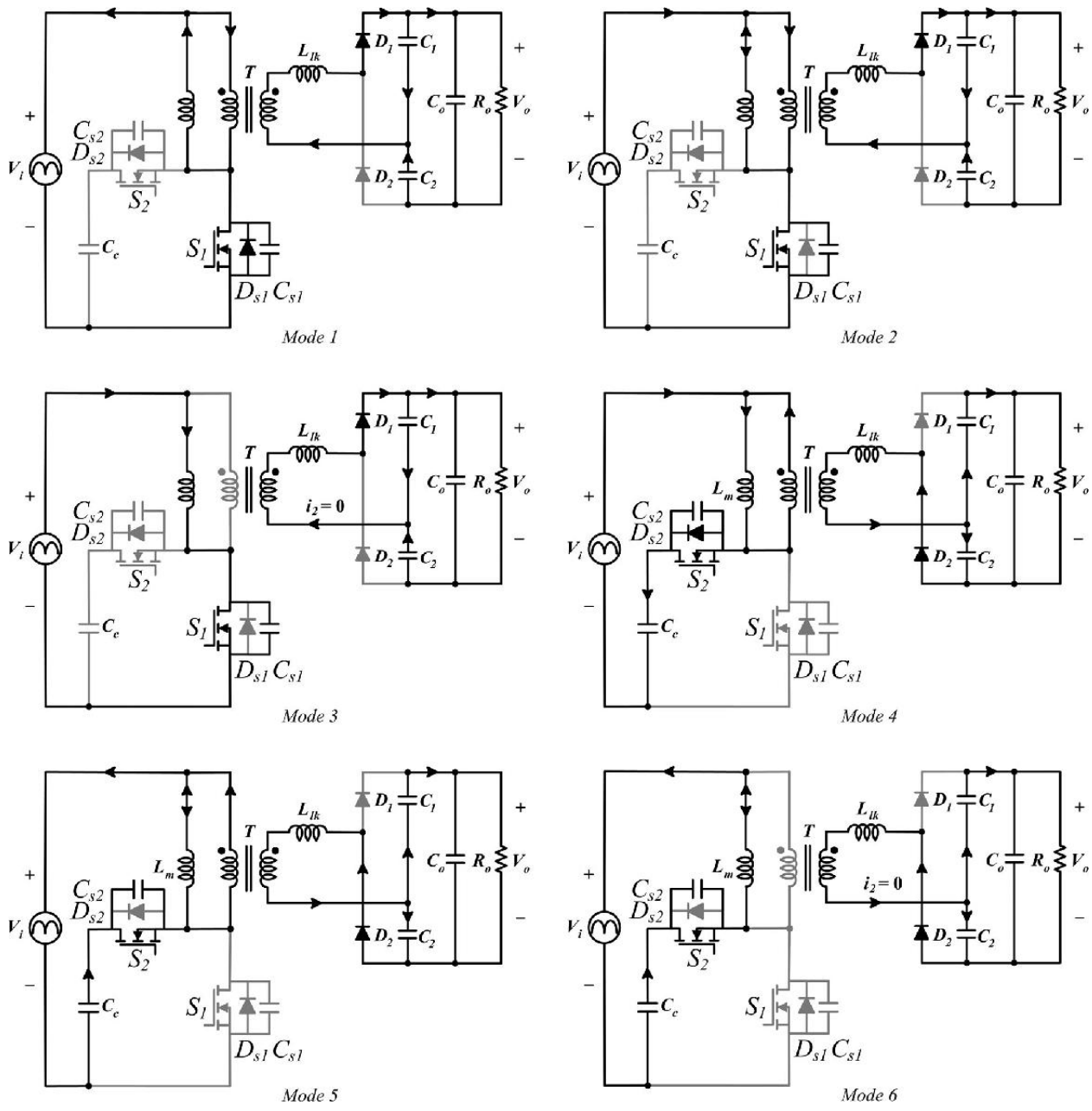

Fig. 3. Operating modes of the proposed ac–dc converter.

with the flowing slope

$$\frac{di_m}{dt} = \frac{V_i - V_c}{L_m} = \frac{D}{1 - D}\frac{V_i}{L_m}. \quad (9)$$

During this mode, the input power is transferred to the output stage like in Mode 1. The voltage across L_{lk} is the difference between the secondary winding voltage v_2 and the resonant ca-pacitor voltage v_{c2}. Since the equivalent clamp capacitor C_c/n^2 is much larger than C_r, the resonant effect of C_c is negligible in the series-resonant network that is composed of C_c/n^2, C_r, and L_{lk}. Therefore, i_2 begins to resonate again by L_{lk} and C_r sim-ilar to the first series resonance in Mode 1. The state equations of the series-resonant circuit can be written as follows:

$$L_{lk}\frac{di_2}{dt} = n(V_c - V_i) - v_{c2} \quad (10)$$

$$i_2 = -C_r \frac{dv_{c2}(t)}{dt}. \quad (11)$$

Here, i_2 is obtained as follows:

$$i(t) = \frac{nV_c - nV_i - V_c}{Z_r}\sin\omega_r(t - t_3) \quad (12)$$

where V_{c2} is the average voltage of C_2. The angular resonant frequency ω_r and the impedance Z_r are equal to (6). From (9) and (12), i_1 decreased by the second series resonance can be

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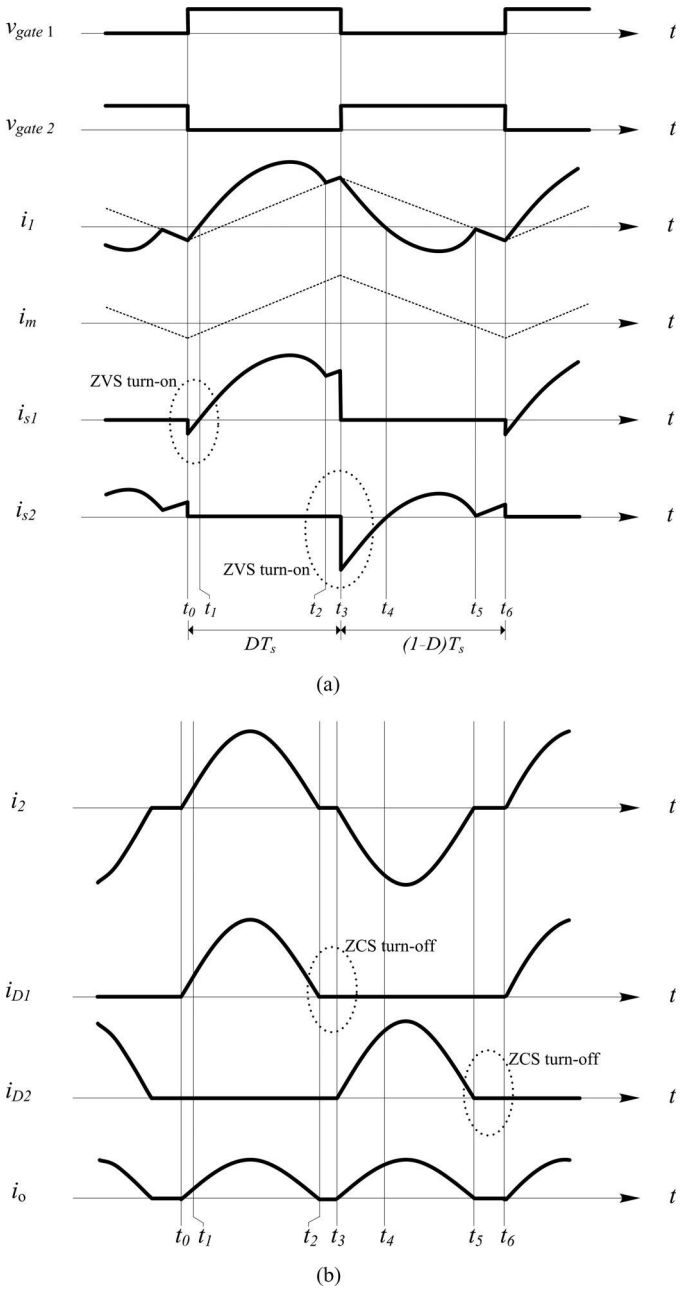

Fig. 4. Theoretical waveforms of the proposed converter. (a) Input side waveforms. (b) Output side waveforms.

obtained as

$$i_1(t) = i_m(t_3) - \frac{DV_i}{1-D}\frac{}{L_m}(t - t_3) \qquad n^2 V_c - n^2 V_i - nV_{c2} \sin\omega(t \quad t \quad).(13)$$

$$- \qquad Z_r \qquad r \quad - 3$$

As shown in Fig. 4(b), the output current i_o becomes half of the output diode current i_{D2} like in Mode 1.

Mode 5 *[t_4 , t_5]:* At the time t_4 , L_{lk} and C_r still resonate similar to Mode 4. In addition, i_1 may change its direction during this interval based on the designed resonant frequency f_r .

Mode 6 *[t_5 , t_6]:* At the time t_5 , i_2 becomes zero and D_2 is maintained to the on-state with the zero current. i_1 and i_m are equal during this mode. Therefore, i_1 terminates the series resonance and decreases linearly as (9). At the end of this mode, D_2 is turned off with the zero current. The ZCS turn-off of D_2 removes its reverse-recovery problem.

With the average voltage across the primary winding N_p dur-ing S_2 turn-on, $V_1 = DV_i/(1-D)$, from the volt–second balance law of the magnetizing inductance L_m , the average voltages across the resonant capacitors C_1 and C_2 are as follows:

$$V_{c1} = \frac{n^2 L_m + L_{lk}}{nL_m} V_i = (1-D)V_o \qquad (14)$$

$$V_{c2} = \frac{n^2 L_m + L_{lk}}{nL_m} \frac{D}{1-D} V_i = DV_o \qquad (15)$$

where the output voltage of the converter V_o is $V_{c1} + V_{c2}$. From (14) and (15), the relationship between the input voltage and the output voltage can be obtained as

$$\frac{V_o}{V_i} = \frac{n^2 L_m + L_{lk}}{nL_m} \frac{1}{1-D} . \qquad (16)$$

If L_{lk} is a very small value compared to L_m , from (16), the voltage transfer function of the proposed converter becomes that of an isolated boost converter.

III. Control Algorithm

The proposed converter has no PFC circuit. Therefore, to obtain a high power factor, it requires the control algorithm for both PFC and output control. The duty ratio D according to the input current i_{in} is hard to control because the relation of D and i_{in} is nonlinear. To achieve good controllability, the nonlinear system needs to be transformed into the linear system by the feedback linearization.

During the on-state and the off-state of S_1 , from Kirchhoff's voltage law, each equation can be obtained as follows:

$$\begin{aligned} &|v_{in}| - L_m \frac{di_m}{dt} = 0, && \text{on-state of } S_1 \\ &|v_{in}| - V_c - L_m \frac{di_m}{dt} = 0, && \text{off-state of } S_1 . \end{aligned} \qquad (17)$$

From (17), the average magnetizing inductance voltage of the transformer for one switching period T_s is expressed as

$$|V_{in}| D + (|V_{in}| - V_c)(1-D) = L_m \frac{i_m}{T_s} \qquad (18)$$

where i_m is current variations of i_m for one switching period T_s . The ripple component of V_c can be neglected by the large clamp capacitor value. Therefore, from the volt–second balance law of L_m , V_c is as follows:

$$V_c = \frac{|v_{in}|}{1-D} . \qquad (19)$$

If L_{lk} is a very small value compared to L_m , from (16), the voltage transfer function of the proposed converter is expressed as

$$\frac{V_{o,ref}}{|v_{in}|} \approx \frac{n}{1-D} \qquad (20)$$

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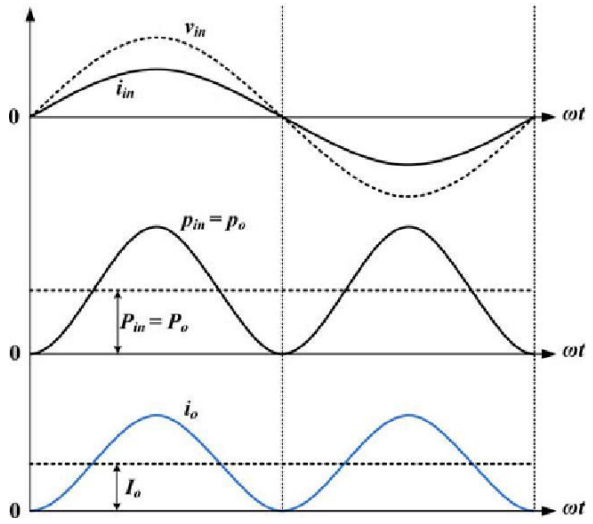


Fig. 5. Key waveforms of the ideal single power-conversion ac–dc converter.

where $V_{o,\mathrm{ref}}$ is the reference output voltage. From (18), (19), and (20), the duty ratio D can be expressed as follows:

$$D = 1 - \frac{nV_i}{V_{o,\mathrm{ref}}} + L_m \frac{n}{V_{o,\mathrm{ref}} T_s} i_m = D_n + \Delta D \quad (21)$$

where the nominal duty ratio D_n and the duty ratio variations ΔD are expressed as follows:

$$D_n = 1 - \frac{nV_i}{V_{o,\mathrm{ref}}}, \quad \Delta D = L_m \frac{n}{V_{o,\mathrm{ref}} T_s} i_m. \quad (22)$$

As shown in (22), D_n is decoupled from (21) and the relation of ΔD and i_m is linear. Also, the rectified input current variation I_i is equal to the primary current variation $i_1 = i_m$ because $i_1 = i_2/n$ is zero. Thus, the relation of I_i and ΔD is linear. In conclusion, the nonlinear system becomes the first-order linear system by controlling ΔD.

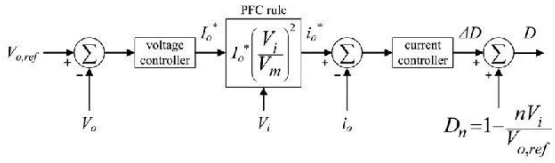
Fig. 5 shows the input voltage, the input current, the input power, the output power, and the output current when the input power factor is unity. When unity power factor is achieved, the input current i_{in} is a sinusoidal waveform in phase with v_{in} as

$$i_{\mathrm{in}} = I_m \sin \omega t \quad (23)$$

where I_m is the amplitude of the input current. Assuming that the converter is ideal with no power loss, the instantaneous input power p_{in} and the desired instantaneous output power p^*_o can be derived as

where $V_{o,\mathrm{ref}}$ is the reference output voltage and i^*_o is the desired output current. As shown in Fig. 5, when the constant output voltage is achieved, i^*_o is expressed as

$$P_{\mathrm{in}} = v_{\mathrm{in}} i_{\mathrm{in}} = V_{o,\mathrm{ref}} i_o^* = p_o^* \quad (24)$$



As shown in (25), i_o^* is proportional to $\sin^2 \omega t$. Therefore, i_o^* for PFC and power control can be expressed as

$$i_o^* = I_o^* \left(\frac{V_m}{V_i}\right)^2 \quad (26)$$

where i_o^* is the amplitude of the desired output current.

Fig. 6 shows the control block diagram of the proposed converter. The voltage controller attempts to minimize the error value as the difference between $V_{o,\mathrm{ref}}$ and the measured output voltage by adjusting i_o^*, that is, i_o^* is calculated by the voltage controller, and then i_o^* is calculated by the PFC rule in Fig. 6. In order to realize the PFC rule, synchronization with input voltage v_{in} is necessary. Since V_i includes the information about the amplitude and the phase of v_{in}, the synchronization with v_{in} is implemented by using V_i as shown in Fig. 2. The current controller attempts to minimize the error value as the difference between i_o^* and the measured output current i_o by adjusting D. Finally, D is obtained by adding ΔD to D_n.

The proposed control system consists of the inner loop and the outer loop. The inner loop is the current control loop and the outer loop is the output voltage control loop. The proposed control system is analyzed by using a small signal model. The crossover frequency of the open-loop transfer function $T_v(s)$ for the voltage controller is chosen much smaller than the open-loop transfer function $T_i(s)$ for the inner current loop. The open-loop transfer functions $T_i(s)$ and $T_v(s)$ are expressed as

$$T_i(s) = H_i \cdot C_{ic}(s) \cdot G_{id}(s) \quad (27)$$

$$T_v(s) = H_v \cdot C_{vc}(s) \cdot G_{vi}(s) \quad (28)$$

where $H_i(s)$ and $H_v(s)$ are current sensor gain and voltage

Fig. 6. Control block diagram of the proposed converter.

sensor gain, respectively. The small signal transfer functions of the duty ratio-to-output current and the output current-to-voltage, respectively, can be obtained as follows:

$$G_{id}(s) = \frac{\hat{i}_o(s)}{\hat{d}(s)}, \quad G_{vi}(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} \quad (29)$$

where the variables $\hat{i}_o(s)$, $\hat{v}_o(s)$, and $\hat{d}(s)$ are the small signals of i_o, V_o, and D, respectively. The PI compensator for the outer voltage loop $C_{vc}(s)$ and the P compensator for the inner current loop $C_{ic}(s)$ are expressed as

$$C_{vc}(s) = K_{pv} + \frac{K_{iv}}{s}, C_{ic}(s) = K_{pc}. \quad (30)$$

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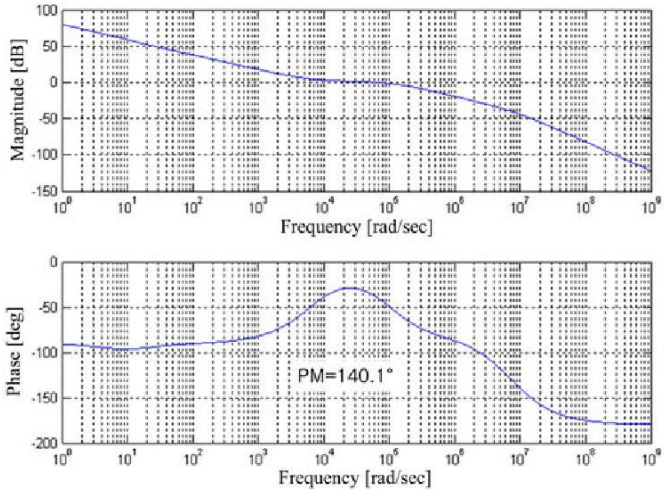

Fig. 7. Bode plot of overall open-loop transfer function $T_{o\,p}(s)$.

to have large time constant. The transfer function of the overall open-loop transfer function $T_{o\,p}(s)$ can be obtained as follows:

$$T_{o\,p}(s) = H_v(s) \cdot C_{v\,c}(s) \cdot G_{v\,i}(s) \cdot 1 + \underbrace{H_i(s) \cdot C_{ic}(s) \cdot G_{id}(s)}_{C_{ic}(s) \cdot G_{id}(s)} \quad (31)$$

From Fig. 7 and (31), the stability and dynamics of the proposed converter can be analyzed. Fig. 7 shows the bode plot of $T_{o\,p}(s)$ with designed parameters. The gain and phase margins are infinite and 140.1°, respectively. The proposed converter is a highly stable system whose stability is not affected by its gain. It also possesses considerable phase margin. Hence, it is theoreti-cally acceptable for the controller's gain to tend to infinity since overshoots or oscillations will be damped by the high phase margin.

IV. Design Guidelines

In this section, the design guidelines of the proposed converter are introduced. These guidelines help to define the ac–dc converter with the input voltage v_{in}. From (19), the voltages across the switches S_1 and S_2 are

$$v_{s1} = v_{s2} = v_c = \frac{V_i}{1-D}. \quad (32)$$

Thus, if V_i, V_o, and D are selected, the voltage margin of the switches S_1 and S_2 can be calculated from (32).

The soft switching of S_2 is naturally achieved by the stored energy in L_{lk} and L_m. However, the ZVS design of S_1 is determined by L_m and p_o. The relationship between I_i and i_o has an inverse proportion with the relationship (16). Also, since the average of the secondary current is zero, the average of the magnetizing current $i_{m,avg}$ is equals to I_i and can be obtained from the relationship between I_i and i_o as follows:

$$I_{m,avg} = I_i = \frac{n^2 L_m + L_{lk}}{nL_m} \frac{1}{1-D} i_o. \quad (33)$$

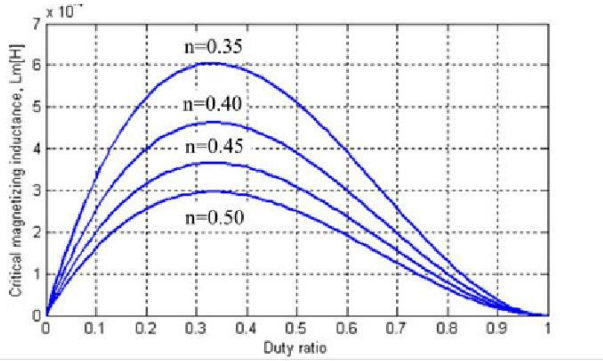

Fig. 8. Critical magnetizing inductance for turn-on ZVS of the switches.

TABLE I
Parameters and Components of the Prototype

Parameters	Symbols	Value
Input voltage	v_{in}	$90\sim265V_{rms}$
Output voltage	V_o	200V
Switching frequency	f_s	50kHz
Input capacitor	C_i	2.2μF
Clamp capacitor	C_c	2.2μF
Magnetizing inductance	L_m	435μH
Secondary leakage inductance	L_{lk}	1μH
Primary winding turns	N_p	45turns
Secondary winding turns	N_s	18turns
Resonant capacitors	C_1, C_2	2.2μF
Output capacitor	C_o	330μF
Components	**Symbols**	**Part number**
Switches	S_1, S_2	W26NM60
Transformer core	T	PQ3535
Output diodes	D_1, D_2	15ETH03
Full-bridge diode rectifier		RBV-1506

From i_m and i_1 in Fig. 4(a), $i_{m,avg}$ can be calculated as follows:

$$i_{m,avg} = \frac{i_1(t_0) + i_1(t_3)}{2} = \frac{i_m(t_0) + i_m(t_3)}{2}. \quad (34)$$

From (9), (16), (33), and (34), if L_{lk} is negligible, i_1 at the time t_0 can be derived as

$$i_1(t_0) \approx \frac{n}{L_m} i_{D=nL_m} - \frac{1}{2} \frac{D(1-D)T_s}{L_m} V_o. \quad (35)$$

For ZVS of the main switch S_1, i_1 at the time t_0 should be negative. L_m is then designed to satisfy the following relation:

$$L_m < \frac{D(1-D)^2 v_o^2}{2n^2 f_s p_{o,peak}} \quad (36)$$

where f_s is the switching frequency. From Fig. 5, $p_{o,peak}$ is twice the rated output power P_o because the average value of the instantaneous output power p_o is the rated output power P_o. According to the variation of the duty ratio D, the critical magnetizing inductance value to satisfy the turn-on ZVS condition of the switches can be seen from Fig. 8.

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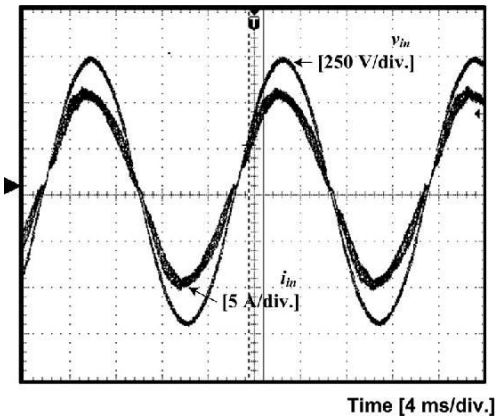


Fig. 9. Experimental waveforms of the input voltage v_{in} and current i_{in}.

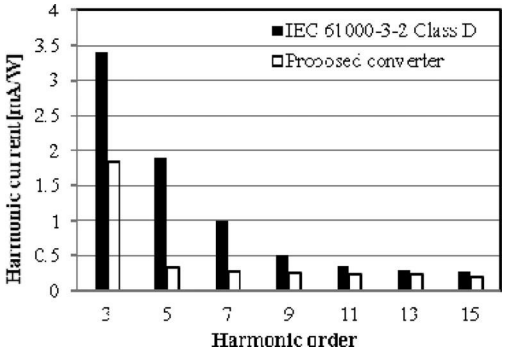


Fig. 10. Harmonic content of the input current i_{in}.

For the ZCS turn-off of D_1 and D_2, the following critical conditions must be satisfied:

$$C_r < \frac{1}{\omega_r^2 L_l} = (1-D)^2 T_s^2 \quad \text{for } D > 0.5$$

$$\frac{k}{\omega_r^2 L_l} \quad \frac{\pi^2 L_l k}{D^2 T_s^2} \qquad (37)$$

$$C_r < \frac{k}{} = \pi^2 L_l k \quad \text{for } D < 0.5$$

where the critical angular resonant frequency ω_{rc} is $\pi f_s / D$.

V. Experimental Results

An experimental prototype was implemented to verify the theoretical analysis. It was designed for the following specifications: input voltage v_{in} = 90–265 Vrms, output voltage V_o = 200 V, rated output power P_o = 400 W, and switching frequency f_s = 50 kHz. The major components and parameters of the prototype used for experiments were presented in Table I. The turns ratio n of the transformer was selected as n = 0.4. Then, the turn-on ZVS condition (36) of S_1 and S_2 resulted in $L_m < 460\ \mu$H and the magnetizing inductance L_m was selected as 435 μH, Also, the resonant capacitors, $C_1 = C_2 = 6.6\ \mu$F, were selected from the turn-off ZCS condition (37) of the out-put diodes D_1 and D_2. The control algorithm was implemented fully in software using a single-chip microcontroller, Microchip dsPIC30F3011.

Fig. 9 shows the waveforms of the input voltage and the input current. The input current is sinusoidal and in phase with the input voltage. The measured power factor is greater than 0.99.

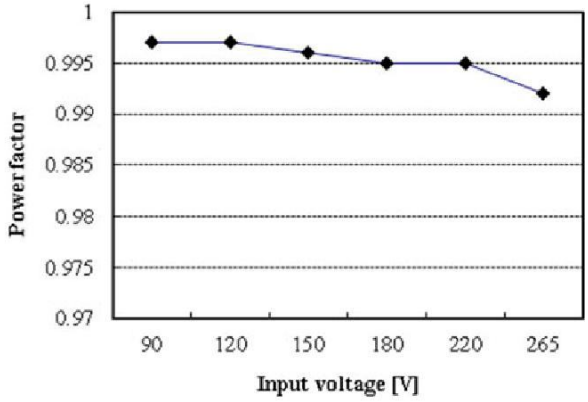
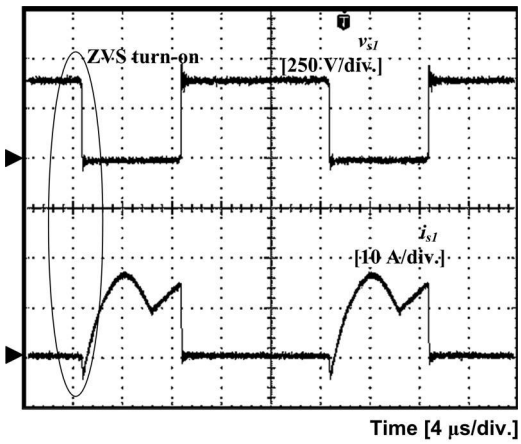
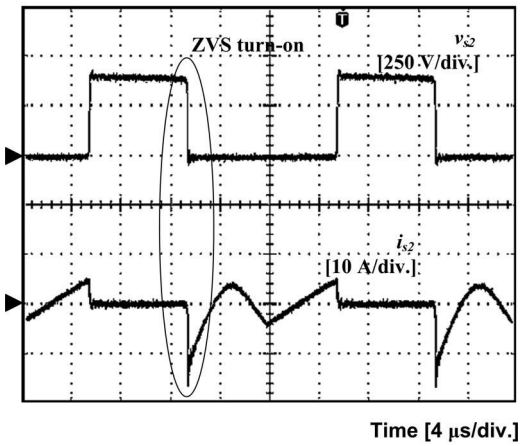


Fig. 11. Power factor under the universal input voltage v_{in}.



(a)



(b)

Fig. 12. Experimental waveforms of the ZVS turn-on of the switches. (a) v_{S1} and i_{S1}. (b) v_{S2} and i_{S2}.

Fig. 10 shows the harmonic spectrum of the input line current i_{in} when v_{in} = 220 V and P_o = 400 W. It can be seen that all harmonics are in compliance with the IEC 61000-3-2 Class D. Fig. 11 shows the variation of PF in the v_{in} range from 90 to 265 Vrms. It can be observed that the high PF (above 0.99) over the universal line voltage is achieved.

Fig. 12(a) shows the experimental waveforms of v_{s1} and i_{s1} flowing through S_1 at the full load. Also, the experimental

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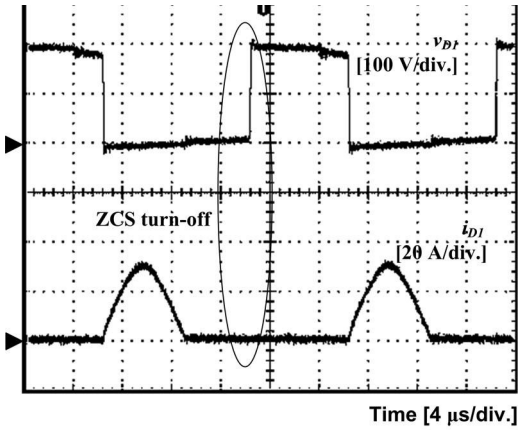
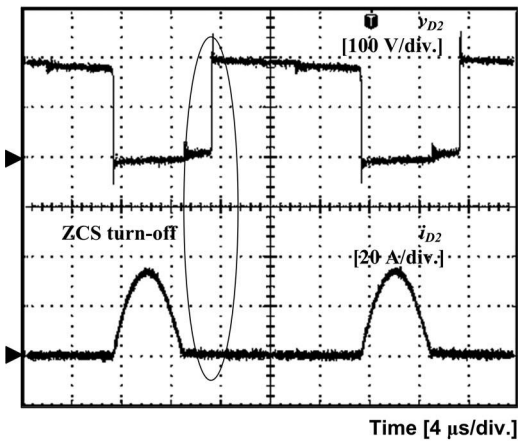


(a)



(b)

Fig. 13. Experimental waveforms of the ZCS turn-off of the output diodes. (a) v_{D1} and i_{D1}. (b) v_{D2} and i_{D2}.

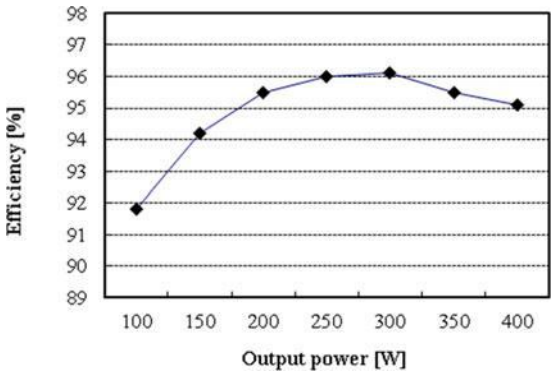


Fig. 14. Power efficiency under different loads.

waveforms of v_{s2} and i_{s2} flowing through the switch S_2 in the full load are shown in Fig. 12(b). These waveforms show that S_1 and S_2 achieve the ZVS at the moment of the turn-on. Fig. 13shows the experimental waveforms of the output diodes D_1 and D_2. From these waveforms, it can be seen that v_{D1} and v_{D2} are clamped to the output voltage V_o and the output diode current i_{D1} and i_{D2} reach zero before D_1 and D_2 are reversely biased, which guaranteed the ZCS turn-off of the diodes. There-fore, the switching losses of S_1 and S_2 and the losses caused by the reverse-recovery problem are reduced. Fig. 14 shows the power efficiency under different loads. The measured power ef-ficiency is over 95% at full load. The efficiency is measured by the digital power meter Yokogawa WT130. The measured maximum efficiency is about 95.1% at the full load.

VI. Conclusion

This paper has proposed a single power-processing ac–dc converter with a high power factor and high power efficiency. Also, analysis, design, and experimental results for the pro-posed converter have been presented. The proposed converter combines the full-bridge diode rectifier and the series-resonant active-clamp dc–dc converter. The series-resonant active-clamp dc–dc converter is based on a flyback converter that employs the active-clamp at the transformer primary side and the voltage doubler at the transformer secondary side to reduce the switch-ing losses and the voltage stress of the main switch suffered from the transformer leakage inductance. Also, the proposed converter provides a simple structure, a low cost, and low volt-age stresses by the single power-conversion without a PFC cir-cuit. Therefore, the proposed converter is suitable for low-power applications. The proposed converter has low line current har-monics to comply with the IEC 61000-3-2 Class D limits and the high power factor of 0.995 by using the proposed control al-gorithm for both PFC and power control. The proposed control algorithm can be used to the boost type PFC ac–dc convert-ers since it is based on the control algorithm of the PFC boost converter in the continuous conduction mode. The proposed converter provides the high efficiency of 95.1% at the full load by the single power-processing, the turn-on ZVS mechanism of the switches by the active-clamp circuit, and the turn-off ZCS mechanism of the output diodes by the series resonance.

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