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A Dual Full-Bridge DC–DC Converter with Reduced Circulating Current, Output Filter, of Rectifier Stage for RF Power Generator Applications

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Abstract- In this paper, a hybrid dual full-bridge dc–dc converter for radio frequency (RF) power engenderer application is proposed to overcome the drawbacks of a conventional phase-shift full-bridge (PSFB) converter such as the large circulating current of the primary side and large output filter size. The proposed converter adopts a dual full-bridge hybrid structure with a small series capacitor in the primary side and a full-bridge rectifier with two additional low-voltage-rated diodes in the secondary side. With this structure, the proposed converter has advantages of reduction of circulating current, zero-voltage switching (ZVS) operation of all primary switches, size reduction of the output inductor, and low conduction loss of the rectifier stage. Additionally, the proposed converter can regulate the output voltage very wide by changing the operational mode according to the output voltage. These advantages result in the improvement of whole load efficiency. The operational principle and analysis of the proposed converter are presented and analyzed.
KEY WORDS- Circulating current, hybrid dual full-bridge, output filter, wide output voltage applications, zero-voltage switching (ZVS).

1. INTRODUCTION

In the semiconductor fabrication process, plasma is commonly used to process silicon wafers in the manufacturing of integrated circuits and other semiconductor devices. For producing this plasma, a radio frequency (RF) power generator is widely utilized.

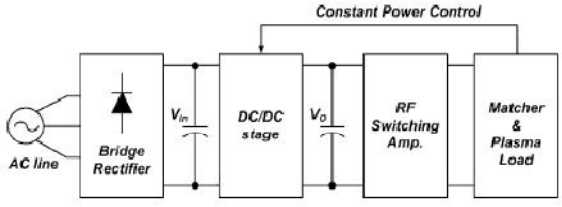

Figure 1. Structure of an RF power generator.

Since the plasma produced by an RF power generator is mainly allied with the quality of semiconductor device, the RF power generator requires stable power conversion processing, high efficiency, and high output power [1].Figure 1 shows the typical structure of the RF power generator. As shown in Figure 1, the RF power generator is composed of three components: front-end dc/dc converter, RF switching amplifier, and matcher and plasma load. The front-end dc/dc converter converts the ac line input voltage to variable dc output voltage according to the required output power of system and it additionally provides electrical isolation of system. The RF switching amplifier receives the dc output voltage and engenders RF power signal whose frequency can be anywhere between 9 kHz and 300 GHz. The matcher is utilized to match the generator to the load to ascertain maximum power transfer. Among these components, as pre regulator of the RF generator, the front-end dc/dc converter should provide wide and variable output power regulation capability.

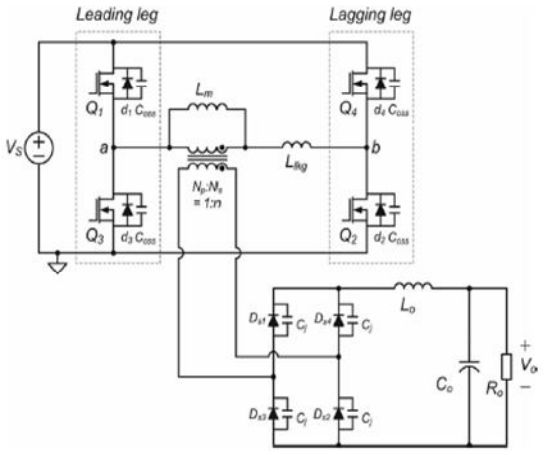

Figure 2. Circuit diagram of the conventional PSFB converter.

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The conventional phase-shift full bridge converter is an attractive topology for high power and wide output voltage applications, since it has some desirable features such as low current/voltage stress, the ZVS operation of all primary switches, and variable output regulation capability by the phase shifted control signal [2]. Figure 2 shows the circuit diagram of the conventional PSFB converter. However, the conventional PSFB converter has several problems for wide-output-voltage applications such as the RF power generator. Since the operating duty cycle of the conventional PSFB converter prodigiously varies with the output voltage variation, large circulating current exists on the primary side during the freewheeling period [3]–[6]. Besides, the size of the output filter is highly incremented due to the small duty operation and it results in low power density and high cost [7]–[10]. To reduce the filter size and to achieve the ZVS operation of all switches for wide-output-voltage applications, several converters with hybrid structure such as full–full bridges or full–half bridges are proposed [10]–[15]. The common characteristic of the hybrid structure is that the input energy is transferred to the output stage even during the freewheeling period. Hence, the waveform of the output filter is ameliorated and the reduction of the filter size becomes possible.

A hybrid dual full-bridge converter with reduced circulating current, small output filter, and low conduction loss of the rectifier stage for RF power generator applications is proposed in this paper. The proposed converter adopts two full-bridge inverters that share the lagging leg for the primary side and employs full-bridge rectifier with two additional diodes that have low voltage stress for the secondary side. This structure allows the proposed converter to have following advantages: 1) reduced filter size because input energy is perpetually transferred to the output over the whole switching period; 2) reduced circulating current by employing a minuscule capacitor connected in series with one transformer; 3) the ZVS operation of all switches is well achieved in spite of eliminated circulating current; 4) in the

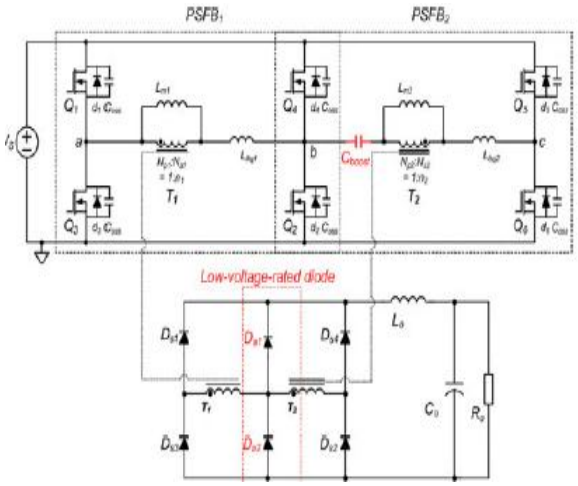

Figure 3. Circuit diagram of the proposed converter.

rectifier stage, since the load current is distributed to two additional low-voltage-rated diodes that have good performance such as lower forward voltage and reverse recovery characteristic, secondary conduction loss is greatly reduced; and 5) the proposed converter has higher conversion ratio than the conventional PSFB converter. As a result, the conduction loss of the primary side is also significantly reduced due to the reduction of circulating current and primary current.

2. DESCRIPTION OF THE PROPOSED CIRCUIT

Figure 3 shows the circuit diagram of the proposed converter .As shown in Figure 3, the proposed converter is composed of two PSFB converters PSFB1 and PSFB2 that are placed in parallel on the primary side. One of PSFB converters PSFB1 consists of switches Q1, Q2, Q3 and Q4 and a transformer T1. The other converter PSFB2 consists of switches Q2, Q4, Q5 and Q6, a small capacitor C_{boost}, and a transformer T2. Both PSFB converters share switches Q2 and Q4. In order to eliminate the circulating current of T2, C boost is connected in series with T2 as shown in Figure 3. Due to the voltage across this capacitor, which is called the boost capacitor, the circulating current of T2 is reset during the freewheeling period. In the secondary side, both main transformers T1 and T2 are connected in series and a full-bridge rectifier consisting of Ds1, Ds2, Ds3 and Ds4 is employed. The midpoint of both transformers is connected with a additional diode leg having low-voltage-rated diodes Da1 and Da2. Since

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the voltage stress of Da1 and Da2 is much lower than that of outer diodes Ds1, Ds2, Ds3 and Ds4, diodes that have low forward voltage can be employed for Da1 and Da2. The proposed converter has two operational modes: dual full bridge mode and single full-bridge mode.

1) Dual Full-Bridge Mode: At dual full-bridge operational mode, the first full-bridge section has full duty operation which designates that the diagonal pair of switches Q1 andQ2, Q3 and Q4 conduct together, and the output power is controlled by varying the phase shift among Q2, Q4 andQ5,Q6 as shown in Figures. 4 and 5. Since the circulating current of switches Q2, Q4, Q5 and Q6 is eliminated by the voltage of C_{boost}, conduction loss of the primary side is greatly reduced during the dual full-bridge operation .In spite of reduced circulating current of T2, since the ZVS operation of lagging-leg switches Q1, Q2, Q3, and Q4 is assisted by the primary current $i_{pri1}(t)$ of T1, the ZVS operation of all six switches can be easily achieved.

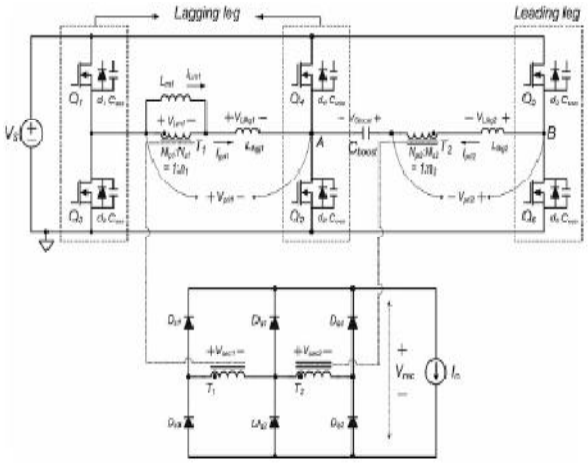

Figure4. Circuit diagram of the proposed PSFB converter at dual full-bridge mode.

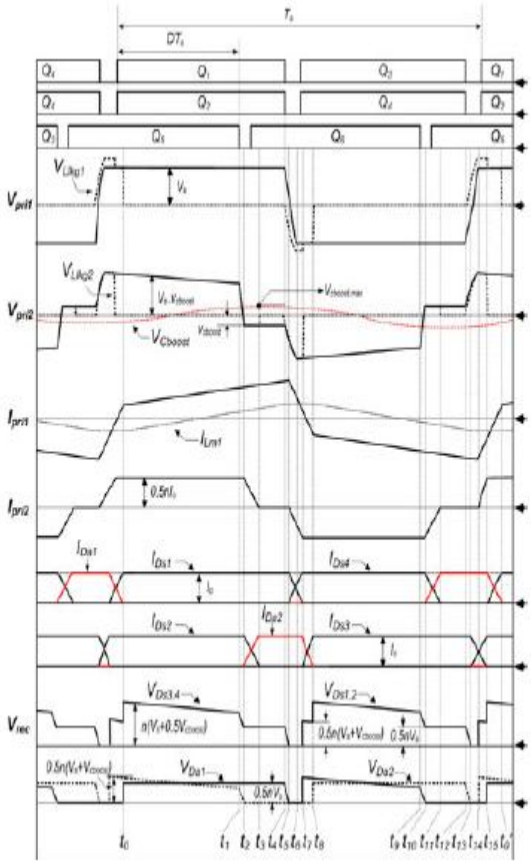

Figure 5. Key waveform at dual-full bridge operation.

2) Single Full-Bridge Mode: At single full-bridge operational mode, a phase-shifted gate signal is applied to switches Q1, Q2, Q3 and Q4, and switches Q5and Q6 are disenabled as shown in Figures. 6 and 7. Hence, power is mainly delivered to the output stage throughQ1, Q2, Q3, Q4, T_1, D_{s1}, D_{s3}, D_{a1}, and D_{a2}. Since T_1 of the proposed converter has lower turns ratio than that of the conventional PSFB converter, a full-bridge stage can be operated with large duty ratio and it results in reduction of the conduction loss of the primary side. Furthermore, since the main power is delivered through D_{a1} and D_{a2}, which have low forward voltage, secondary conduction loss is also reduced during the single full-bridge operation.

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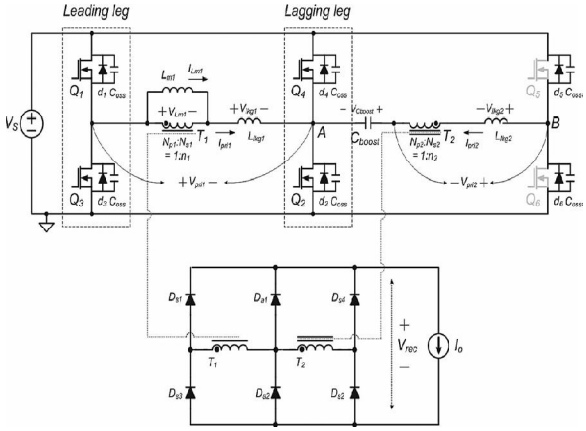


Figure 6. Circuit diagram of the proposed PSFB converter at single full-bridge mode.

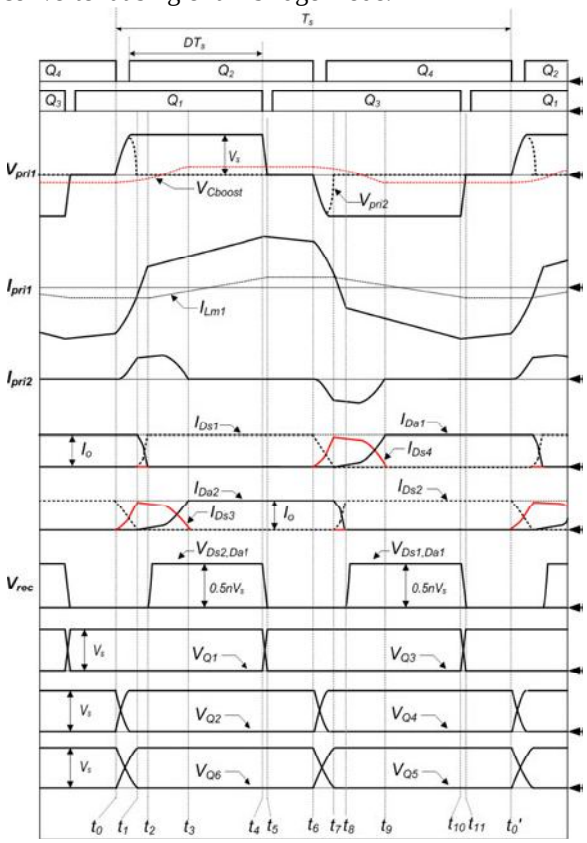


Figure 7. Key waveform at single full-bridge operation.

3. OPERATIONAL PRINCIPLE

3.1. Dual Full-Bridge Operation

Mode 1 [t_0–t_1]: Mode 1 commences when the commutation of D_{s1} and Da1 is culminated. Q1, Q2, and Q5 are conducting and input power is transferred to the secondary side. During mode1, positive input voltage Vs is applied to the primary voltage $v_{pri1}(t)$ of T1 and Vs − $v_{Cb}(t)$ is applied to the primary voltage $v_{pri2}(t)$ of T2 , respectively. Therefore, primary current ipri1 (t) is linearly incremented. However, the magnetizing inductance Lm2 of T2 is prodigiously and sizably voluminous so that the effect of magnetizing inductor current iLm2 (t) can be ignored. Then, i_{pri2} (t) virtually has the same value with reflected load current. Since i_{pri2} (t) charges the boost capacitor C $_{boost}$, the voltage v_{cboost} (t) of C boost is linearly incremented in this mode. The energy stored in transformers T1and T2 is transferred to the output through Ds1 and Ds2. The output voltage of rectifier stage v_{rec} (t) is the sum of reflected voltage v_{sec1} (t) of T1 and reflected voltage v_{sec2} (t) of T2. The currents and the voltages are represented as follows:

$$i_{pri1(t)} = 0.5nI_0 + \frac{v_s}{L_{m1}+L_{lkg1}}(t - t_0) + i_{pri1}t_o \quad (1)$$

$$i_{pri2}(t) = 0.5nI_0 + \frac{Vs - VC_{boost}(t)}{L_{m2}+L_{1kg2}}(t\text{-}t_o)$$

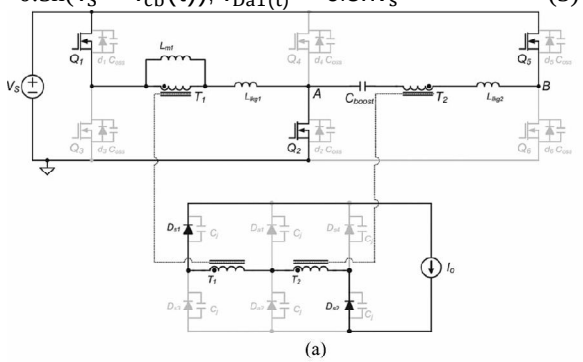
$$=0.5nI_0+i_{pri2}(t_0) \quad (2)$$

$$VC_{boost}(t) = VC_{boost}(to) + 0.5nI_0/VC_{boost}(t\text{-}t_o) \quad (3)$$

$$v_{rec}(t) = n(v_s - 0.5v_{cb}(t)) \quad (4)$$

$$v_{DS1.3(t)} = n(v_s - 0.5v_{cb}(t)), v_{Da2}(t)$$

$$=0.5n(V_S - V_{cb}(t)), V_{Da1(t)} = 0.5nv_s \quad (5)$$



(a)

Figure 8(a). Mode 1

Mode 2 [t1 –t2]: At time t1, Q5 is turned OFF and mode2 commences. The output capacitors C_{oss} of switches Q5 and Q6 are linearly charged and

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discharged, respectively, by the energy stored in the output inductor Lo. vpri2(t) is linearly decremented to zero and the primary vpri1(t) is perpetually maintained at Vs . Hence, vsec2 (t) is decremented from n(Vs – V_C boost (t)) to zero voltage. Then, v_{rec}(t) falls from n(Vs − 0.5v_{Cboost}(t)) to0.5nVs .

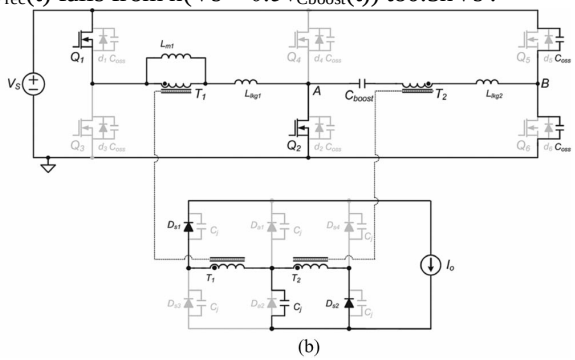

Figure 8(b). Mode 2

Mode 3 [t2 –t3]: After v_{pri2}(t) reaches zero, anti parallel diode D6 of Q6 commences to conduct. When Q6 is turned ON at this time, the ZVS operation of Q6 is achieved. During mode 3, since the commutation between Ds2 and Da2 is progressed, total v_{Cboost}(t) is applied to L_{lkg2} and i_{pri2}(t) commences to decrement rapidly. v_{pri1}(t) is still maintained at Vs during this mode. Hence, v_{rec}(t) is maintained at 0.5nVs and i_{pri1}(t) is perpetually incremented. The currents and secondary voltages are represented as follows:

$$i_{pri1}(t) = 0.5nI_0 + \frac{V_S}{L_{m1}+L_{1Kg1}}(t\text{-}t_2) + i_{pri1}(t_2) \quad (6)$$

$$i_{pri2}(t) = i_{pri2(t_2)}\text{-}\frac{1}{L_{1kg2}}\int vc_{boost}(t)dt \quad (7)$$

$$VC_{boost}(t) = VC_{boost}(t_2) + \frac{1}{C_{boost}}\int i_{pri2}(t) \quad (8)$$

$$V_{rec}(t) = 0.5nV_s \quad (9)$$

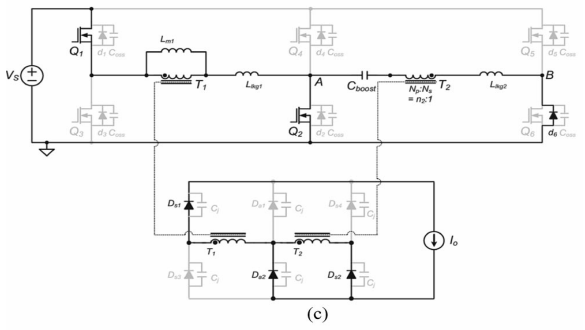

Figure 8(c). Mode 3

Mode 4 [t3 –t4]: When the commutation between Ds2 andDa2 is consummated, mode 4 commences. Since ipri2(t) is in the zero state, the input power is transferred to the output stage through only T1, Ds1, and Da2 . The voltage of boost capacitor v_{cboost} (t) remains its maximum value $V_{cboost,\ max}$ and the secondary voltage v_{sec2} (t) of T2 is decremented to $0.5nV_{Cboost,\ max}$.

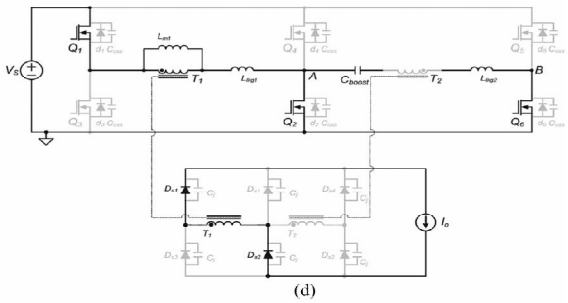

Figure 8(d). Mode 4

Mode 5 [t4 –t5]: At time t4, Q1 and Q2 are turned OFF and mode 6 commences. Since v_{sec1} (t) remains in the positive side, output current still permeates T1, Ds1, and Da2 during this mode .Hence, C_{oss} of Q1, Q2, Q3, and Q4 are linearly charged and discharged, respectively, by the reflected load current of T1and the current of magnetizing inductor L_{m1}. The voltages and currents are represented as follows:

$$i_{pri1}(t) = 0.5nI_0 + I_{Lm1}(t_4), where I_{Lm1}(t_4) = \frac{V_S T_s}{4L_{m1}} \quad (10)$$

$$V_{Q3}(t) = V_{Q4}(t) = V_S - \frac{0.5I_0+I_{Lm1}(t_4}{4c_{oss}}(t\text{-}t_4) \quad (11)$$

$$V_{pri1}(t) = V_S - \frac{0.5nI_0+I_{Lm1}(t_4}{2C_{OSS}}(t\text{-}t_4) \quad (12)$$

$$V_{pri2}(t) = -V_{Cboostmax} - \frac{0.5nI_O+ILm_1(t_4)}{4c_{oss}}(t\text{-}t_4) \quad (13)$$

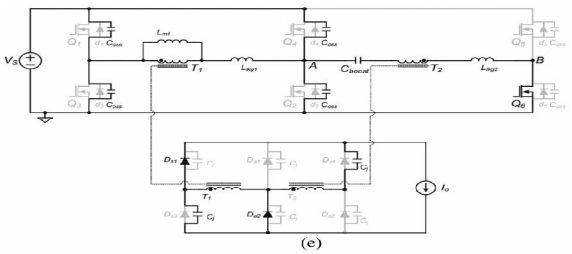

Figure 8(e). Mode 5

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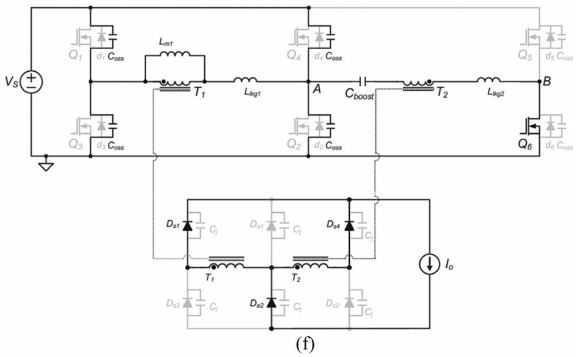
Mode 6 [t5 –t6]: When the sum of v_{sec1} (t) and v_{sec2} (t) reaches at zero voltage, mode 6 starts. At time t5, Ds4 starts to conduct and the commutation between Ds1 and Ds4 is progressed. The C_{oss} of Q1, Q2, Q3, and Q4 is charged and discharged, respectively, in a resonance manner with $L_{lkg1} + L_{lkg2}$. The voltages and currents are represented as follows:

$$V_{pri1}(t) = V_{pri1}(t_5) - 2i_{pri1}(t_5)Z_o \sin(w_0(t - t_5)) \quad (14)$$

$$V_{pri2}(t) = V_{pri2}(t_5) - 2i_{pri1}(t_5)Z_o \sin(w_0(t - t_5)) \quad (15)$$

$$i_{pri1}(t) = i_{pri1}(t_5)(1 - Z_O \cos(W_0(t - t_5)) \quad (16)$$

$$i_{pri2}(t) = -i_{pri1}(t_5)(1 - Z_O \cos(W_0(t - t_5)) \quad (17)$$



(f)

Figure 8(f). Mode 6

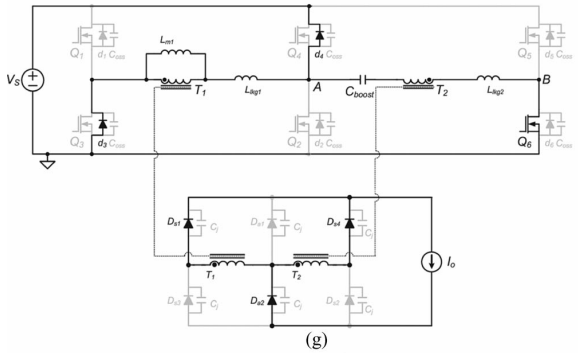
Mode 7 [t6 –t7]: After vpri1(t) and vpri2(t) reach −Vs, the anti parallel diode D3 of Q3 and anti parallel diode D4 of Q4 start to conduct. When Q3 and Q4 are turned ON at this time, the ZVS operation of Q3 and Q4 is achieved. During this mode, the commutation between Ds1 and Ds4 is still progressed. The sum of the input voltage Vs and divided voltage of $V_{cboost,\ max}$ is applied to both leakage inductor L_{lkg1} of T1 and leakage inductor L_{lkg2} of T2 so that $i_{pri1}(t)$ and $i_{pri2}(t)$ are rapidly decreased to the negative side. The voltages and currents are represented as follows:

$$V_{l1kg1} = V_S + VC_{boost.max}\frac{L_{1kg1}}{L_{1Kg1}+L_{1Kg2}} \quad (18)$$

$$V_{l1kg2} = V_S + VC_{boost.max}\frac{L_{1kg2}}{L_{1Kg1}+L_{1Kg2}} \quad (19)$$

$$i_{pri1}(t) = i_{pri1}(t_6) - \frac{V_{l1Kg1}}{L1_{Kg1}}(t\text{-}t_6) \quad (20)$$

$$i_{pri2}(t) = -\frac{V_{L1kg2}}{L1Kg_2}(t\text{-}t_2) \quad (21)$$



(g)

Figure 8(g). Mode 7

Mode 8 [t7 –t8]: When the commutation between Ds1 and Ds4 is finished, mode 8 begins. At this time, since the commutation between Ds3 and Da2 is progressed, Vs is applied to the $L_{lkg1}$and $i_{pri1}(t)$ is continuously decreased to the negative side. The negative voltage −Vs + v_{cboost}(t) is applied to v_{pri2}(t); then ,v_{rec}(t) is increased to 0.5n(Vs + v_{cboost} (t)) and input energy is transferred to the output through T2,Q4,Q6,Da2 , and Ds4 .

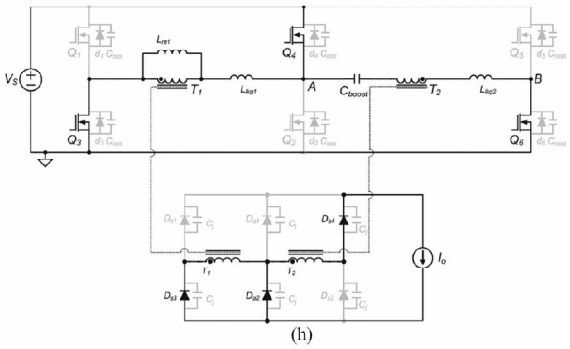
The voltages and currents are represented as follows:

$$i_{pri1}(t) = i_{pri1}(t_7) - \frac{V_S}{L_{1Kg1}}((t - t_7) \quad (22)$$

$$i_{pri2}(t) = -0.5nI_0 \quad (23)$$

$$V_{pri2(t)} = -V_S + V_{Cboost}(t) \quad (24)$$

$$VC_{boost}(t) = VC_{boost.max} - \frac{1}{C_{boost}}\int i_{pri2}(t) \quad (25)$$



(h)

Figure 8(h). Mode 8

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3.2. SINGLE FULL BRIDGE OPERATION

The operation of the proposed converter at single full-bridge operation is almost the same as the conventional PSFB converter except modes 1–3. Hence, only modes 1–3 are explained and the explanation of other modes is omitted.

Mode 1 [t0 –t1]: At t0, after Q4 is turned OFF mode 1 begins. The output capacitors C_{oss} of Q2 and Q4 are charged and discharged, respectively, in a resonance manner with equivalent leakage inductor (L_{lkg1} //L_{lkg2}) and the voltage of Q2 starts to decrease. Hence, the difference between VQ2 and

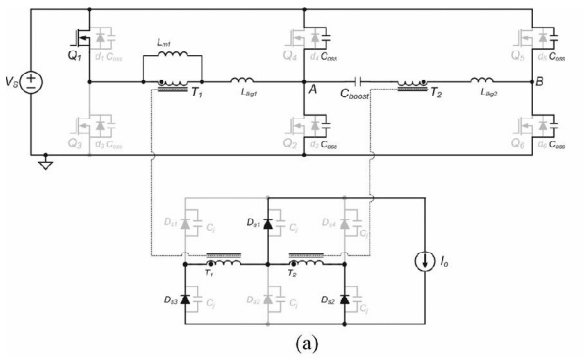
VQ5 + $v_{cboost}(t)$ is applied to $v_{pri2}(t)$ and $i_{pri2}(t)$ starts to increase. From this operation, the voltage transition between Q5 and Q6 occurs and the commutation between Ds2 and Ds3 is progressed. C_{boost} is charged by $i_{pri2}(t)$. The voltages and current are represented as follows:

$$v_{Q2}(t) = i_{pri1}(t_0)Z_L \sin(w_L(t - t_0)) \quad (26)$$

$$v_{Q5}(t) = V_s - i_{pri1}(t_0)Z_L \sin(w_L(t - t_0)) \quad (27)$$

$$i_{pri1}(t) = i_{pri1}(t_0)(1 + Z_O \cos(W_L(t - t_0)) \quad (28)$$

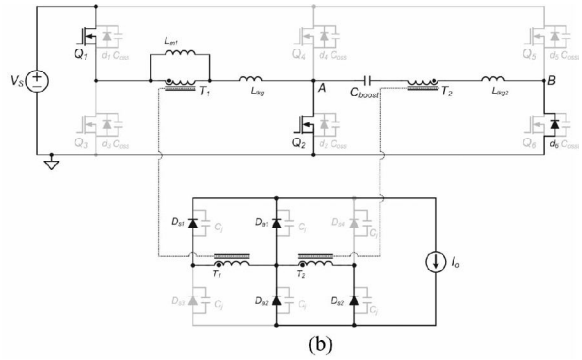
$$i_{pri2}(t) = i_{pri1}(t_0)Z_L \cos(W_L(t - t_0)) \quad (29)$$



(a)

Figure 9(a). Mode 1

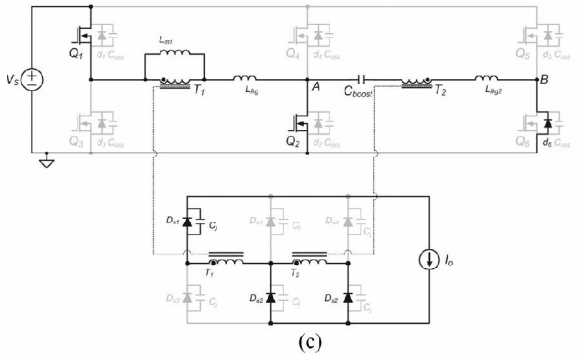
Mode 2 [t_1 –t_2]: After the commutation betweenD_{s2} andD_{s3} is finished, mode 2 begins. The antiparallel diode d_6 of Q_6 and Q_2 is conducted. The commutation between D_{s2} and D_{a2}, D_{a1} and D_{s1} is progressed and V_s is applied to L_{lkg1} and $v_{cboost}(t)$ is applied to l_{lkg2} . Therefore, $i_{pri1}(t)$ and $i_{pri2}(t)$ are increased.



(b)

Figure 9(b). Mode 2

Mode 3 [t_2 –t_3]: At t_2, the commutation betweenD_{s1} andD_{a1} is finished and mode 3 begins. During this mode, the commutation between D_{s2} and D_{a2} is still progressed and input energy is mainly transferred to the secondary side through T_1, D_{s1}, and D_{a2}. When $v_{cboost}(t)$ is increased to the positive side, $i_{pri2}(t)$ starts to decrease. When $i_{pri2}(t)$ reaches zero current, mode 3ends.



(c)

Figure 9(c). Mode 3

4. RESUTS

4.1. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed converter, a 3-kWlaboratory prototype converter has been built with following specifications: input voltage: Vs = 280 V, output voltage variation: Vo = 40–200 V, switching frequency: fs = 100 kHz, and maximum output power: Po = 3 kW. Components of prototype are shown in Table 1. Figure 10 shows the designed output voltage profile of the prototype as output power variation. As shown in Figure 10, the operational mode of the proposed converter is changed from single full-bridge mode to dual full-bridge mode at 30% load condition and 110-V output voltage.

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TABLE 1
COMPONENT LIST

Components list	Proposed Converter		Conventional PSFB converter
Primary switches	IPP60R045 (600V/60A)		IPP60R045 (600V/60A)
Transformer	EI5040 x 1		EI5040x2 L_m: 330μH L_{lkg}:2.2uH N_p:N_s=9:8
	T_1 L_m: 302μH L_{lkg}:4.3uH N_p:N_s=18:8	T_2 L_m: 647μH L_{lkg}:2.25uH N_p:N_s=18:7	
Rectifier diode (D_{s1}~D_{s4})	APT75DQ60 (600V/75A/2V)		APT75DQ60 (600V/75A/2V)
Additional diode (D_{a1},D_{a2})	30EPH03 (300V/60A/1.25V)		N/A
Output Inductor (L_o)	CM3580060 x 2 (Φ: 35mm, H: 10.46mm) 28uH		CM400060 x 2 (Φ: 40mm, H: 14.48mm) 58μH
Boost capacitor (C_{boost})	500nF		N/A
Output capacitor (C_o)	750uF/350V		750uF/350V

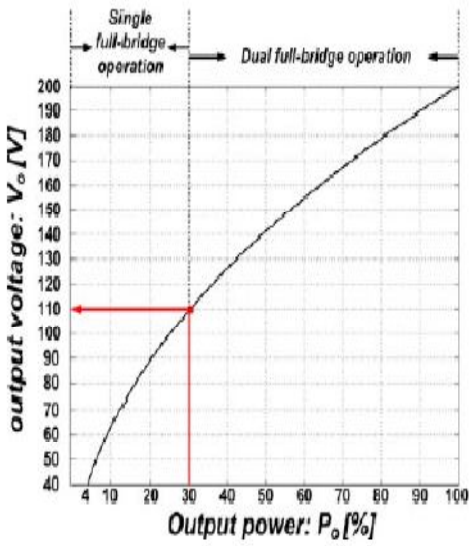

Figure 10. Output voltage profile versus output power.

Figure 11 show experimental results of primary voltage and primary current for both the conventional PSFB converter and the dual full-bridge operation of the proposed PSFB converter at full-load condition. As shown in Figure 11, the proposed converter has reduced circulating current and smaller RMS current as discussed in the previous section, while the conventional converter has large circulating current due to the small duty operation.

Figure 12 shows experimental results of primary voltage and primary current for both the conventional PSFB converter and single full-bridge operation of the proposed PSFB converter at 20% load condition. As shown in Figure 19, the proposed converter has smaller RMS current despite the existence of circulating current because the proposed converter has smaller turns ratio (n_1 = 0.44) than that in the conventional PSFB converter (n =0.88). Therefore, it is noted that the proposed converter has lower conduction loss of the primary side over whole load condition compared to the conventional PSFB converter.

Figure 13 shows the gate signal and drain-to-source voltage of lagging-leg switch at dual full-bridge operation. As shown in Figure 13, the drain-to-source voltage reaches zero before the gate signal reaches its threshold voltage. Therefore, the ZVS operation of lagging-leg switches is well achieved.

Figure 14 shows size comparison of the designed output inductor between the conventional PSFB converter and the proposed converter. As shown in Figure 14, the proposed converter has smaller inductor size than the conventional PSFB converter.

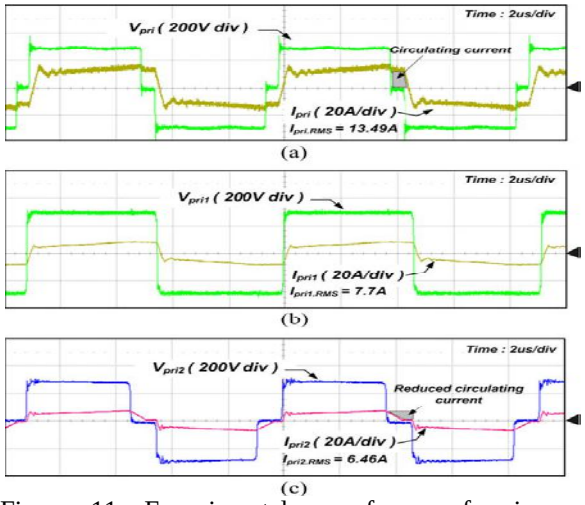

Figure 11. Experimental waveforms of primary voltage and primary current at full load condition. (a) Vpri and Ipri of the conventional PSFB converter. (b) Vpri1 and Ipri1 of the proposed converter. (c) Vpri2 and Ipri2 of the proposed converter.

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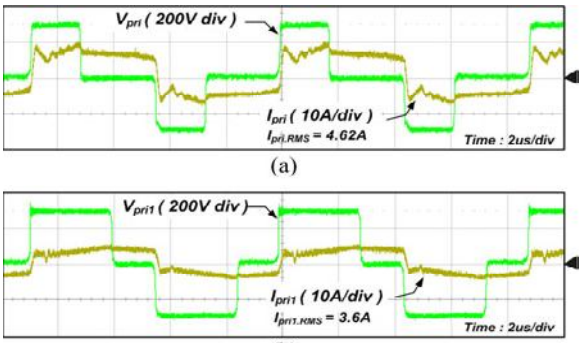


Figure 12. Experimental waveforms of primary voltage and primary current at 20% load condition. (a) Vpri and Ipri of the conventional PSFB converter. (b) Vpri1 and Ipri1 of the proposed converter.

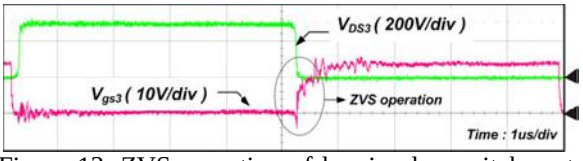


Figure 13. ZVS operation of lagging-leg switches at dual full-bridge mode

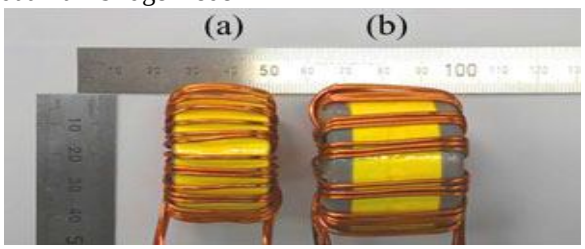
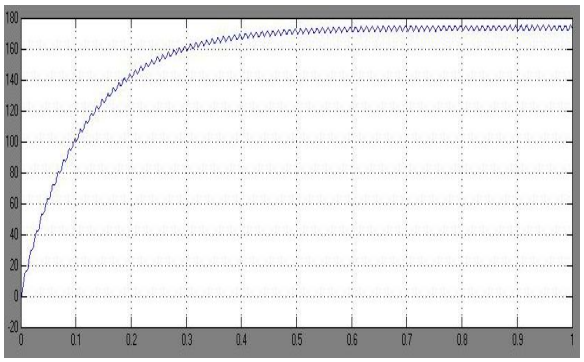


Figure 14. Size comparison of the output inductor. (a) Output inductor of the proposed converter. (b) Output inductor of the conventional PSFB converter.

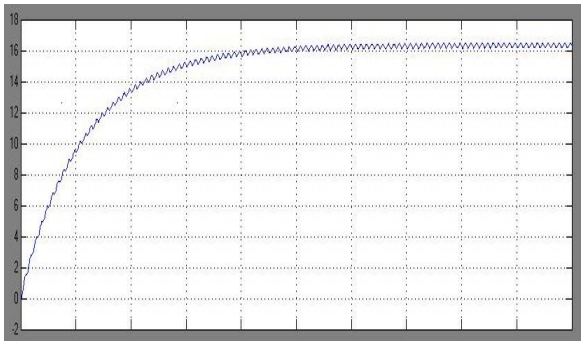
4.2. SIMULATION RESULTS

The Proposed dual full-bridge dc-dc converter is designed using MATLAB SIMULINK. The input voltage is Vs = 280 V, output voltage variation is Vo = 40–200 V, and maximum output power: Po = 3 kW.

The output voltage and current waveforms of the proposed converter are shown in Figure 15.



(a)



(b)

Figure 15. (a) Voltage and (b) Current Waveforms

The output power of the converter is shown in Figure 16.

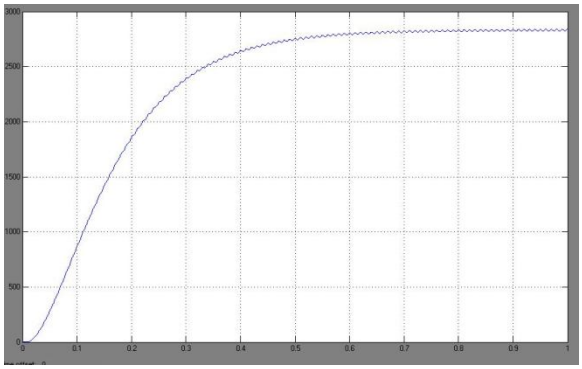


Figure 16. Waveform of output power.

VI. CONCLUSION

A new hybrid dual full-bridge converter with reduced circulating current, small output filter, and low conduction loss of the rectifier diode for RF power generator application is proposed in this paper. By adopting a small capacitor connected in series with one transformer, the circulating current is greatly

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reduced .In spite of reduced circulating current, the ZVS operation of all switches is well achieved. Furthermore, the energy is transferred to the output stage during the freewheeling period so that the waveform of the rectifier output voltage is ameliorated and it results in the size reduction of the output inductor compared to the conventional PSFB converter. In addition, since the load current is distributed to the additional low-voltage-rated diode, the secondary conduction loss is also reduced in the proposed converter. These advantages result in an improvement in efficiency over wide output voltage and power ranges. Therefore, it can be verbally expressed that the proposed converter is very desirable and opportune for a high-power and high-efficiency front-end dc/dc converter for wide-output-voltage applications such as the RF power generator.

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