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A NEW SINGLE-PHASE CASCADED MULTILEVEL INVERTER BASED ON NOVEL H-BRIDGE UNITS

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Abstract—In this paper, a new single-phase cascaded multilevel inverter based on novel H-bridge units is proposed. In order to generate all voltage levels (even and odd) at the output, nine different algorithms are proposed to determine the magnitudes of dc voltage sources. Then, the proposed algorithms are compared to investigate their advantages and disadvantages. This topology is able to increase the number of output voltage levels by using a lower number of power electronic devices such as switches, power diodes, driver circuits, and dc voltage sources that lead to reduction in installation space and cost of the inverter. In addition, in the proposed cascaded multilevel inverter, not only the number of required power electronic devices is reduced, but also the amount of the blocked voltage by switches, and the number of different voltage amplitudes of the used sources is decreased .These features are some of the most important advantages of the proposed topology. These features are obtained via the comparison of the proposed topology and its proposed algorithms with the conventional cascaded multilevel inverters that have been presented in the literatures. The operation and performances of the proposed topology with its presented algorithms in generating all voltage levels have been verified by using the experimental results of a49-level single-phase inverter.

Index Terms—Cascaded multilevel inverter, developed H-bridge, multilevel inverter.

I. INTRODUCTION

NOWADAYS, the multilevel inverters have received much attention because of their considerable advantages such as high power quality, lower harmonic components, better electromagnetic consistence, lower dv/dt, and lower switching losses [1]–[6]. There are three main types of multilevel inverters: diode clamp multilevel inverter, flying capacitor multilevel inverter, and cascaded multilevel inverter [2]–[4], [7], [8]. The cascaded multilevel inverters have received special attention due to the modularity and simplicity of control. The cascaded multilevel inverters are mainly classified into two groups:1) symmetric, with equal magnitude for the dc voltage sources; and 2) asymmetric, with different values of the dc voltage sources. By increasing the magnitude of dc voltage sources, the higher number of output levels will be generated. Therefore, the asymmetric cascaded multilevel inverters increase the number of output levels by using power semiconductor devices that are the same as the symmetric ones [4], [6], [9]–[13]. Up to now, different topologies with several algorithms to determine the magnitude of their dc voltage sources have been presented in the literatures. In [14], the H-bridge cascaded multilevel inverter with two different algorithms as symmetric and asymmetric inverters has been presented. Two other symmetric cascaded multilevel inverters have been also presented in [15] and [16]. The main advantage of these inverters is the low number of different voltage amplitudes of the used dc sources. However, the higher number of required insulated gate bipolar transistor (IGBTs), power diodes, and driver circuits in generating a specific output level are their remarkable disadvantages. In order to increase the number of output levels with a lower number of power semiconductor devices, different asymmetric cascaded multilevel inverters have been presented in [17]–[19].The bidirectional power switches have been used in these topologies. Each bidirectional power switch includes two IGBTs, two power diodes, and one driver circuit if the common emitter configuration is used. Therefore, in these topologies,

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the installation space and total cost of the inverter increase. As a result, several asymmetric cascaded multilevel inverters have been presented in which the unidirectional switches from the voltage point of view and the bidirectional switches from the current point of view are used in them. Each unidirectional switch consists of an IGBT with an anti parallel diode. Two of these topologies have been presented in [20] and [21]. Two other algorithms for the H-bridge cascaded multilevel inverter have been also presented in [9] and [10]. Because of the asymmetric topology and used unidirectional switches, it seems that the lower number of power electronic devices is the main advantage of these inverters. However, the main disadvantage of the asymmetric topologies is the lost of modularity, which means the use of a high variety of semiconductor devices and dc voltage sources. In this paper, a new single-phase cascaded multilevel inverter with series connection of the novel H-bridge basic units is proposed. Moreover, nine different algorithms to determine the magnitude of dc voltage sources are proposed to generate all output voltage levels. These algorithms are compared to each other from the number of required IGBTs, dc voltage sources, and different voltage amplitudes of the used source points of view. These investigations are done to determine the best proposed algorithm. Then, the proposed topology with its best proposed algorithm is compared to the conventional topologies. These comparisons consist of the amount of the blocked voltage by switches and the number of used power electronic devices. Finally, in order to reconfirm the correct performance of the proposed cascaded multilevel inverter and its algorithms in generating all voltage levels, the experimental

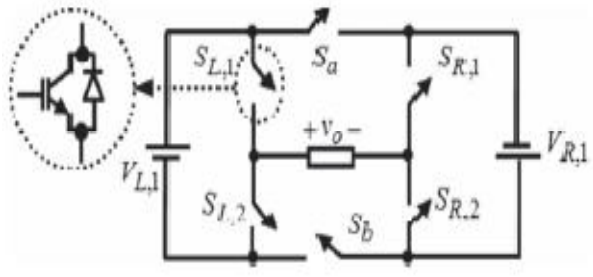

Fig. 1. Basic unit based on developed H-bridge.

TABLE I
OUTPUT VOLTAGE OF THE DEVELOPED H-BRIDGE TOPOLOGY BASED ONDIFFERENT SWITCHING PATTERNS

State	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	v_o
1	1	0	0	1	0	1	$V_{L,1}$
2	0	1	1	0	0	1	$V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1}+V_{R,1}$
4	1	0	1	0	1	0	0
	0	1	0	1	0	1	
5	0	1	1	0	1	0	$-V_{L,1}$
6	1	0	0	1	1	0	$-V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1}+V_{R,1})$

results of a single-phase 49-level inverter based on the proposed topology are used.

II. PROPOSED TOPOLOGY

The topology of the novel H-bridge basic unit is shown in Fig. 1. This unit consists of six unidirectional power switches from the voltage point of view (*SL*,1, *SL*,2, *SR*,1, *SR*,2, *Sa*, and *Sb*) and two insulated dc voltage sources (*VL*,1 and *VR*,1),which is called the developed H-bridge unit [22]. The main disadvantage of the proposed basic unit over the H-bridge is its higher number of required dc voltage sources and power switches; however, this basic unit is able to generate seven different levels at the output, whereas three output levels are only generated in the H-bridge. Table I shows the generated output voltage levels based on the different switching patterns in the proposed basic unit. In this table, 1 and 0 indicate the on and off states of the switches, respectively. As shown in Table I , this basic unit is able to generate seven levels (three positive levels, three negative levels, and one zero level) at the output. In addition, in each switching pattern, one power switches from each leg (*SL*,1 or *SL*,2), (*SR*,1 or *SR*,2), and *Sa* or are turned on simultaneously. If the magnitudes of the dc voltage sources are equally considered, the proposed inverter can generate five levels at the output. Therefore, in order to generate more numbers of output levels at the output, the magnitude of dc voltage sources have to be selected differently. Therefore, the magnitude of the dc voltage sources is considered as follows:

$V_{R,1}=V_{DC}$ (1)

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$V_{L,1}=2V_{DC}$ (2)

A new cascaded multilevel inverter can be made by series connection of *n* number of the H-bridge basic units. This

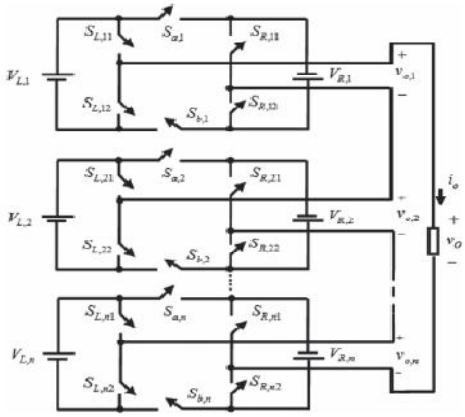

Fig. 2. Proposed cascaded multilevel inverter.

Inverter is shown in Fig. 2. According to Fig. 2, the output voltage of the proposed cascaded multilevel inverter is equal to adding the output levels of different units and is given by

$V_0(t)=V_{0,1}(t)+ V_{0,2}(t)+……..+ V_{0,n}(t)$ (3)

The generated output voltage levels based on the different switching patterns are shown in Table II. In this table, 1 and0 indicate the on and off states of the switches, respectively. In the proposed cascaded multilevel inverter, the number of switches (*N*switch), IGBTs (*N*IGBT), driver circuits (*N*driver), and dc voltage sources (*N*source) are calculated as follows:

$N_{switch}=N_{IGBT}=N_{driver}=6n$(4)

$N_{source}=2n$(5)

The other main parameter in calculating the total cost of the inverter is the maximum amount of the blocked voltage by switches. If the values of the blocked voltage by switches are reduced, the total cost of the inverter decreases [9]. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig. 2, the values of the blocked voltage by switches *SR*,1 and *SR*,2 are equal to

$V_{SR,1}=V_{SR,2}=V_{R,1}$ (6) In (6), *VSR*,1 and *VSR*,2 indicate the values of the blocked voltage by switches *SR*,1 and *SR*,2, respectively. The value of the blocked voltage by switches *SL*,1 and *SL*,2 is equal to

$V_{SL,1}=V_{SL,2}=V_{L,1}$(7)

$V_{Sa}=V_{Sb}=V_{R,1}+V_{L,1}$(8)

In (7), *VSL*,1 and *VSL*,2 indicate the values of the blocked voltage by switches *SL*,1 and *SL*,2, respectively. Moreover, the values of the blocked voltage by switches *Sa* and *Sb* are equal to

TABLE II
OUTPUT VOLTAGE OF THE PROPOSED CASCADED MULTILEVEL INVERTER BASED ON DIFFERENT SWITCHING PATTERNS

$S_{L,11}$	$S_{L,12}$	$S_{R,11}$	$S_{R,12}$	$S_{a,1}$	$S_{b,1}$	$S_{L,21}$	$S_{L,22}$	$S_{R,21}$	$S_{R,22}$	$S_{a,2}$	$S_{b,2}$	⋯	$S_{L,n1}$	$S_{L,n2}$	$S_{R,n1}$	$S_{R,n2}$	$S_{a,n}$	$S_{b,n}$	v_o
1	0	0	1	0	1	1	0	1	0	1	0	⋯	1	0	1	0	1	0	$V_{L,1}$
0	1	1	0	0	1	1	0	1	0	1	0	⋯	1	0	1	0	1	0	$V_{R,1}$
1	0	1	0	0	1	1	0	1	0	1	0	⋯	1	0	1	0	1	0	$V_{L,1}+V_{R,1}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋯	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	1	0	0	1	1	0	1	0	0	1	⋯	1	0	1	0	0	1	$\sum_{i=1}^{n}(V_{L,i}+V_{R,i})$
1	0	1	0	1	0	1	0	1	0	1	0	⋯	1	0	1	0	1	0	0
0	1	0	1	0	1	0	1	0	1	0	1	⋯	0	1	0	1	0	1	
0	1	1	0	1	0	0	1	0	1	0	1	⋯	0	1	0	1	0	1	$-V_{L,1}$
1	0	0	1	1	0	0	1	0	1	0	1	⋯	0	1	0	1	0	1	$-V_{R,1}$
0	1	0	1	1	0	0	1	0	1	0	1	⋯	0	1	0	1	0	1	$-(V_{L,1}+V_{R,1})$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋯	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	0	1	1	0	0	1	0	1	1	0	⋯	0	1	0	1	1	0	$-\sum_{i=1}^{n}(V_{L,i}+V_{R,i})$

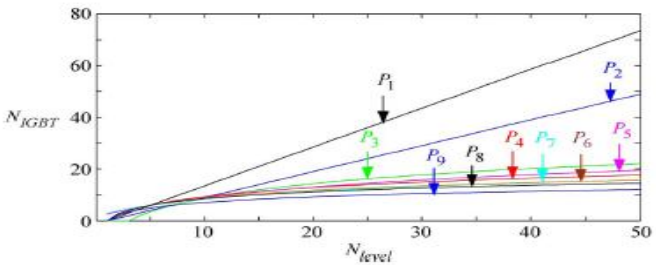

Fig. 3. Variation of *N*IGBT versus *N*level in the proposed algorithms.

where *VSa* and *VSb* indicate the values of the blocked voltage by switches *Sa* and *Sb*, respectively. Therefore, the maximum amount of the blocked voltage by all of the used switches in the first unit, i.e., *V*block,1, is equal to

$V_{block,1}=4(V_{R,1}+V_{L,1})$ (9)

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Similarly, the maximum value of the blocked voltage by the switches in other units is calculated, and thus, the maximum amount of the blocked voltage in the proposed cascaded multilevel inverter, i.e., *V* block, is equal to

$$V_{block=} \quad V_{block,1}+ \quad V_{block,2}+\ldots\ldots..+ V_{block,n}=4(V_{R,1}+V_{L,2}+\ldots..V_{R,n}+V_{L,n}) \quad (10)$$

It is important to note that the existence of all voltage levels at the output is based on suitable selection of the magnitude of dc voltage sources. Thus, in order to generate all voltage levels at the output, nine different algorithms to determine the magnitude of dc voltage sources are proposed. Some of these algorithms had been presented for conventional cascaded inverters in the literature, but they could be also used in the proposed topology or any inverter and are completely based on the topology. According to each of the proposed algorithms, the number of output voltage levels (*N*level), the maximum amplitude of the producible output voltage (*Vo*,max), the number of different voltage amplitudes of the used sources (*N*variety), and the maximum amount of the blocked voltage by switches (*V*block)will be different. These proposed algorithms and all of the aforementioned indexes are calculated and shown in Table III.

III. COMPARING THE PROPOSED ALGORITHMS

Here, the proposed algorithms are compared to each other to investigate their advantages and disadvantages. These investigations are done from several points of view such as the number of different voltage amplitudes of the used sources, the number of IGBTs, and the dc voltage sources. Fig. 3 compares the number of IGBTs in the different proposed algorithms. As it is obvious, the required numbers of IGBTs in the eighth and ninth proposed algorithms are lower than the other algorithms. As mentioned before in unidirectional switches from the voltage point of view, the number of

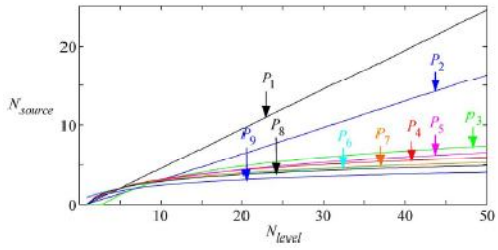

Fig. 4. Variation of *N*source versus *N*level in the proposed algorithms.

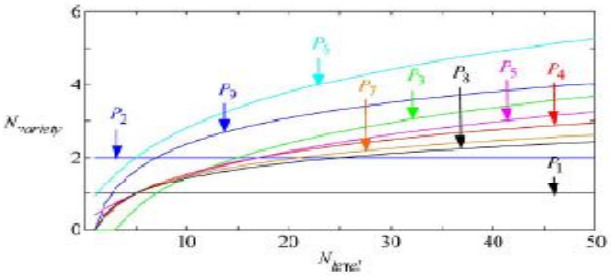

Fig. 5. Variation of *N*variety versus *N*level in the proposed algorithms.

IGBTs is identically tantamount to the number of switches, power diodes, and driver circuits. Therefore, in the eighth and ninth proposed algorithms, the number of switches, power diodes, and driver circuits are less than the other proposed algorithms. Fig. 4 compares the number of required dc voltage sources of the proposed topology predicated on the different proposed algorithms. As shown in Fig. 4, the ninth proposed algorithm needs a lower number of dc voltage sources in engendering particular levels. Moreover, the first proposed algorithm requires more numbers of dc voltage sources. This feature is because of the equal magnitude of the dc voltage sources. Fig. 5 compares the number of different voltage amplitudes of the used sources in the different proposed algorithms. As it is conspicuous, the first proposed algorithm has a lower number of different voltage amplitudes of the used sources. In integration, the ninth proposed algorithm that requires a minimum number of IGBTs and dc voltage sources requires a high number of different voltage amplitudes of the used sources. Never the less, its performance is better than the other presented algorithms, except the first one. From the aforementioned comparisons, it is pellucid that

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the ninth proposed algorithm has a better performance among all the proposed algorithms.

IV. COMPARING THE PROPOSED TOPOLOGY WITH THECONVENTIONAL TOPOLOGIES

The main aim of proposing the new cascaded multilevel inverter is to increase the number of output voltage levels by using a lower number of components. In order to investigate the performance of the proposed topology from the number of different voltage amplitudes of the used sources, the amount

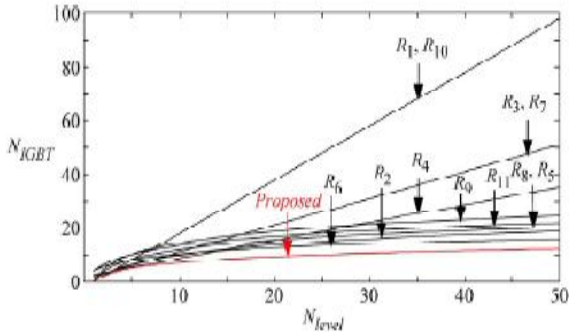

Fig. 7. Variation of *N*IGBT versus *N*level.

IGBTs is identically tantamount to the number of switches, power diodes,and driver circuits. Therefore, in the eighth and ninth proposed algorithms, the number of switches, power diodes, and driver circuits are less than the other proposed algorithms. Fig. 4 compares the number of required dc voltage sources of the proposed topology predicated on the different proposed algorithms. As shown in Fig. 4, the ninth proposed algorithm needs a lower number of dc voltage sources in engendering particular levels. Moreover, the first proposed algorithm requires more numbers of dc voltage sources. This feature is because of the equal magnitude of the dc voltage sources. Fig. 5 compares the number of different voltage amplitudes of the used sources in the different proposed algorithms. As it is conspicuous, the first proposed algorithm has a lower number of different voltage amplitudes of the used sources. In integration, the ninth proposed algorithm that requires a minimum number of IGBTs and dc voltage sources requires a high number of different voltage amplitudes of the used sources. Never the less, its performance is better than the other presented algorithms, except the first one. From the aforementioned comparisons, it is pellucid that the ninth proposed algorithm has a better performance among all the proposed algorithms. cascaded multilevel inverters with bidirectional switches have been presented in [17]–[19] and [21]. These topologies are shown by *R*5−*R*6, *R*11, and *R*8, respectively. Fig. 6 indicates all of the aforementioned structures. Fig. 7 compares the number of the IGBTs in the proposed topology and the conventional cascaded multilevel inverters. As

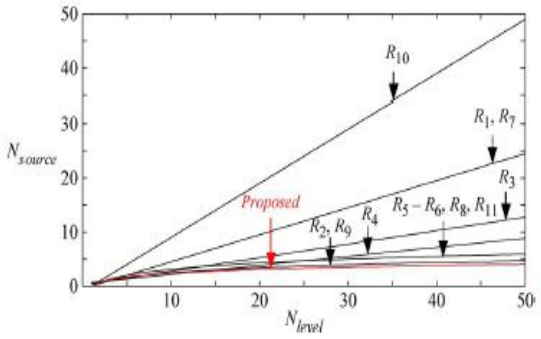

Fig. 8. Variation of *N*source versus *N*level.

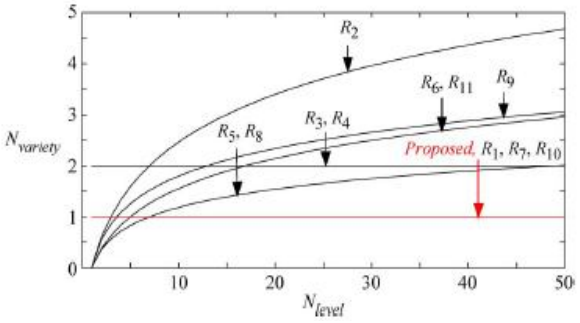

Fig.9. Variation of *N*variety versus *N*level.

it is obvious from Fig. 7, the number of IGBTs in the proposed cascaded multilevel inverter is less than other topologies. As mentioned before, in the proposed topology, the number of switches, power diodes, and driver circuits is the same as the number of IGBTs. This comparison shows that the number of used power switches in the proposed topology is not only lower than the topologies with bidirectional switches but also less than the topologies with unidirectional ones. As a result, the proposed topology has a better feature in this point of view. Fig. 8 shows the comparison of the number of required dc voltage sources. As Fig. 8 indicates, the

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number of required dc voltage sources in the proposed inverter is lower than the other aforementioned topologies instead of the topologies that are indicated by *R*9.Fig. 9 compares the number of different voltage amplitudes of the used sources in the proposed inverter and the conventional cascaded multilevel inverters. In this comparison, the first proposed algorithm is considered. This selection is based on the obtained result from Fig. 5. It is obvious from Fig. 9 that the proposed cascaded multilevel inverter has a lower number of different voltage amplitudes of the used sources. However, this index in the proposed inverter is the same as the topologies that are shown by *R*1, *R*7, and *R*10. It is also important to note that the number of different voltage amplitudes of the used sources is one of the most important features in determining the cost of an inverter. By reducing this amount, the total cost of the inverter decreases. Therefore, this feature is one of the most important advantages of the proposed topology. Fig. 10 compares the magnitude of the blocked voltage by the switches in the proposed inverter and the conventional cascaded multilevel inverters. Fig. 10 shows that the proposed topology consists of the lowest amount of the blocked voltage by switches. This feature in the proposed topology is the same

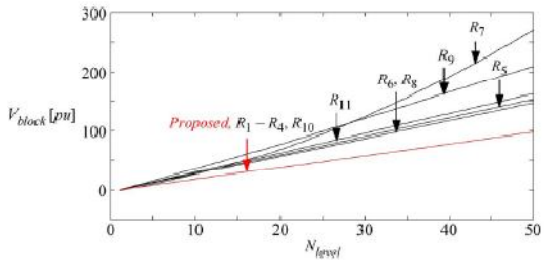

Fig.10. Variation of *V*block versus *N*level.

as the topologies that are shown by *R*1−*R*4 and *R*10. This feature is known as one of the main important indexes in selecting the kinds of power switches and determines the total cost of the inverter. Therefore, if the value of the blocked voltage is reduced, the used switches have lower rating, and thus, the total cost of the inverter decreases. It is point out that all values are considered in per unit. It is clear that the proposed cascaded multilevel inverter requires a minimum number of IGBTs, power diodes, driver circuits, and dc voltage sources. In addition, in this inverter, the different voltage amplitudes of the used sources and the amount of the blocked voltage by switches are also less than the most of the conventional cascaded multilevel inverters that have been presented in the literatures, except the H-bridge cascaded multilevel inverter. These features lead to reduction of the installation space and total cost of the inverter, whereas the number of output voltage levels is increased. As a result, this inverter could be a suitable topology to replace the conventional cascaded inverters in many of applications such as drive and control of electrical machines, connection of renewable sources, flexible alternating current transmission system devices, etc. Although the proposed inverter needs several insulated dc voltage sources, it is important to note that many of the conventional cascaded multilevel inverters, such as the presented topologies in [14], [16], and [20], require a higher number of insulated dc voltage sources. In other words, in the proposed cascaded multilevel inverter, the minimum number of insulted dc voltage sources is used.

V. SIMULATION RESULTS

Here, the correct performance of the proposed cascaded multilevel inverter in generating all voltage levels (even and odd) at the output is verified by using the experimental results of a49-level cascaded inverter. The proposed topology consists of two series-connected developed H-bridges. The magnitude of its dc voltage sources is determined by using the ninth proposed algorithm. Therefore, the values of the used dc voltage sources in the first unit are considered to be *VR*1 = 10 V and*VL*1 = 20 V, and in the second unit, the values will be *VR*2 =70 V and *VL*2 = 140 V. Considering Table III, this inverter is able to generate 49 levels with the maximum amplitude of240 V at the output. The IGBTs used on the prototype areHGTP10N40CID (with an internal anti parallel diode) with the voltage and current rating of 400 V and 10 A, respectively.

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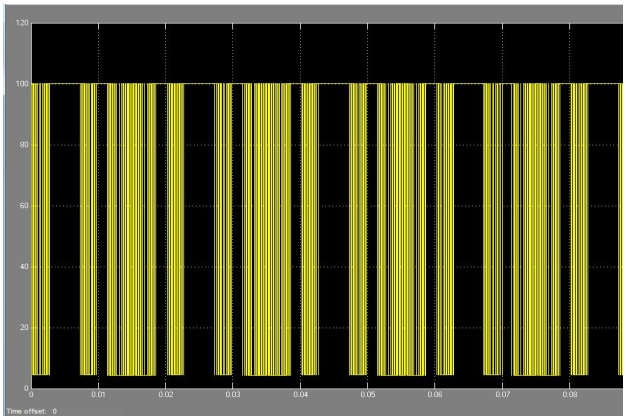
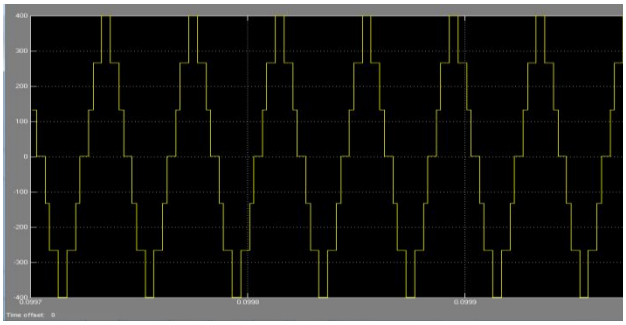


(a)



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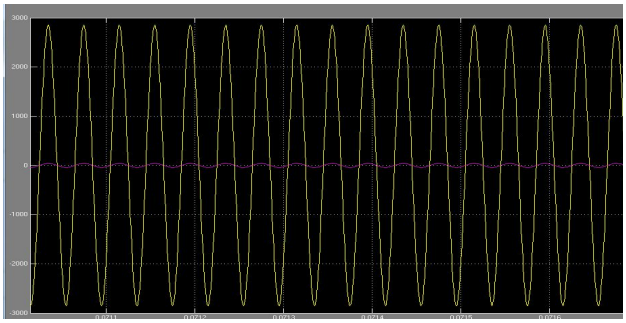

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Fig.11. (a) Output voltage waveforms of the first basic unit. (b) Output voltage waveforms of the second basic unit. (c) Output voltage and current waveforms. The 89C52 microcontroller by ATMEL Company has been used to generate all switching patterns. In all processes of the experimental performance, the load is assumed as R–L with R = 100 Ω and L = 55 mH. The output voltage waveforms of the first and second basic units are shown in Fig. 11(a) and (b),respectively. As shown in Fig. 11(a), the first unit has the ability of generating positive and negative levels with the magnitudes of 0, ±10, ±20, and ±30 V at the output. Moreover, according to Fig. 11(b), the second bridge generates seven levels with the values of 0, ±70, ±140, and ±210 V at the output. The output voltage and current waveforms are shown in Fig. 11(c). It is important to mention that for measuring the output current, a 0.1-Ω resistor has been used. It is obvious from Fig. 11(c) that this inverter is able to produce 49 stepped levels with the maximum output voltage of 240 V. A comparison of the voltage waveform with the current waveform shows that the current waveform is closer to the ideal sinusoidal one. This is due to the resistive–inductive load feature, which behaves as a low-pass filter. Considering the aforementioned comparison, it is obvious that there is a phase different between voltage and current waveforms, which are related to the inductive characteristic of the load. As mentioned, the used power switches on the proposed cascaded multilevel inverter are as unidirectional ones from the voltage point of view; thus, in order to verify this fact, the voltage on switches *SL*,11, *Sa*,1, and *SR*,11 of the first bridge and *SL*,22, *Sb*,2, and *SR*,22 of the second bridge are indicated in Fig. 11(d)–(i). As shown in the figure, the magnitude of the standing voltage on switches are either positive or zero, and there is any negative amount on them. This fact reconfirms the existence of unidirectional power switches in this topology. As can be seen, the maximum blocking voltage by switches *SR*,11,*Sa*,1, *SL*,11, *SR*,22, *Sb*,2, and *SL*,22 are equal to 10, 30, 20,70, 210, and 140 V, respectively. Considering the magnitude of the blocking voltage of the switches, the relations associated to the maximum blocking voltage of the switches are well confirmed.

VI. CONCLUSION

In this paper, a new general topology based on the developed H-bridge has been proposed. Nine different algorithms to determine the magnitude of the dc voltage sources of the proposed inverter are introduced. Then, a comparison between the different proposed algorithms has been done to determine the best algorithm that requires a minimum number of power electronic devices and a lower number of different voltage amplitudes of the used sources. Based on this comparison, the ninth proposed algorithm needs less number of power electronic

devices, but the first proposed algorithm has a lower number of different voltage amplitudes of the used sources. The main advantage of the proposed cascaded multilevel inverter is increasing the number of output voltage levels by decreasing the number of IGBTs, power diodes, driver circuits, and dc voltage sources. In addition, in this inverter, the amount of the blocked voltage by switches is lower than the most of the presented topologies in the literatures, except the H-bridge cascaded multilevel inverter. These results are obtained from the comparison of the proposed inverter with the conventional cascaded multilevel inverters. Finally, the correct performance of the proposed cascaded multilevel inverter with its new algorithm was verified by the experimental results obtained through a 49-level inverter.

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