ISSN 2347 - 3983

International Journal of Emerging Trends in Engineering Research (IJETER), Vol. 3 No.6, Pages : 369 - 372 (2015)
Special Issue of NCTET 2K15 - Held on June 13, 2015 in SV College of Engineering, Tirupati
http://warse.org/IJETER/static/pdf/Issue/NCTET2015sp69.pdf

LOW POWER HIGH SPEED CURRENT COMPARATOR

Raikindi Saidulu[1], J.S.Yadav[2],
[1]MANIT, INDIA,raikindisaidulu@gmil.com
[2]MANIT, INDIA, yadavis@manit.ac.in

ABSTRACT

In this paper a current comparator is proposed which takes low power and has high speed. Simulation has been performed by using 0.18µm CMOS technology. The power consumption of the reference circuit is 0.646mW.This proposed current comparator takes low power of 0.5mw.This power is less compared to the reference circuit.. The propagation delay of the circuit is 0.606 ns at 1µA and for the reference circuit 0.86ns. So speed of the proposed comparator is also increased. Power dissipation is decreased by an amount of 21.36% and propagation delay is decreased by an amount of 29.53% with respect to the reference circuit.

Key words: current mode, front-end signal processing, ADC, delay, power dissipation.

1. INTRODUCTION

Current comparator plays a vital role in analogue circuit design particularly for front-end signal processing applications and increasingly within neuromorphic electronic systems [1],[2]. It is vital to the systems that any decision circuitry such as the comparator is accurate, low power, and high speed. The first comparator which is having high-speed, low input impedance was proposed by Traff in 1992 [6], and for many applications was a significant. Along with traff current comparator various comparators circuits have been proposed. One of them is Chen's current comparator. The traff current comparator is modified by different authors.

In this paper the proposed current comparator is also modified version of Traff current comparator. The proposed current comparator has good characteristics compared to the Traff comparator. Power is one of the important factors in deep submicron technologies. Now a day's most of the devices are portable and to get the maximum battery duration the leakage power dissipation should be as low as possible. There are number of techniques proposed to reduce the power dissipation.They are sleep approach, stacking approach, lector approach, dual vth approach and multi vth approach and so on [7]. So it is a critical component in current mode circuits. Whatever the comparator proposed it needs high speed, low power, high resolution and low supply voltage. Current mode has so many advantageous such as speed, bandwidth and decreased supply voltages. As supply voltage decreases power consumption also decreases. For example current comparator is an important component Analogue to Digital Converter (ADC).The traff comparator and the improved version of the traff comparator proposed in [6], [8] are consuming more power. This is the one of the main limitation of these comparators. The gain of the comparator in [8] is 180V/µA. So it can improve the small difference current applied at the input.

In this paper section 2 explains about the basic characteristics of the current comparator. Section 3 explains about the working of the reference comparator and section 4 presents the different low power techniques available in the literature. Section 5 explains about the proposed circuit followed by the section6 and section 7 in which simulation results and the conclusion are discussed respectively.

II. BASIC CURRENT COMPARATOR

In current comparator two currents are compared. Based on the current values at the input side output voltage is produced. Consider two currents namely I_1 and I_2 then the output of the comparator is as follows

V_0=high for $I_1>I_2$
=Low for $I_1<I_2$

Output voltage is HIGH when I_1 is greater than I_2 and output voltage is LOW when I_1 is less than I_2.A good comparator has low input impedance and quick response time.
The ideal characteristics of current comparator are shown below figure1. V_{OL} and V_{OH} in the above diagram represent the limiting values of logic levels HIGH and LOW.

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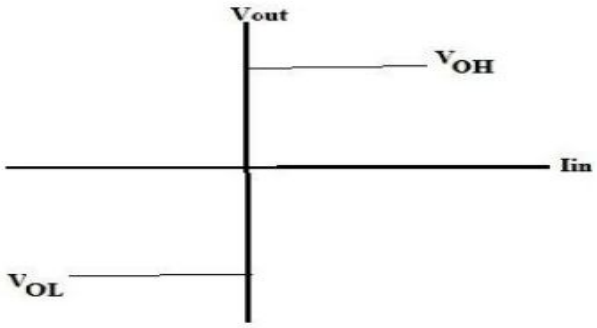

Fig1.transfer characteristics

Ideally the current comparator should detect very small currents. But practically the comparator cannot detect very small currents. The minimum current difference that can be detected by the current comparator is called resolution of that current comparator.

III.REFEENCE CURRENT COMPARATOR

The traff current comparator along current difference circuit stage is shown below. The current difference stage consists of two currents I_1 and I_2.Generally one of the current is taken as reference current. The other current is compared with reference current. We take the difference these two currents from drain terminal of transistor M5 as shown in the above current reference circuit figure2. In the below figure3 is the current compactor which is modified form of the Traff comparator [6].The principle of the operation of the improved Traff current comparator is as follows. The current difference obtained from the current difference circuit is applied at the input of the improved traff current comparator circuit. This improved traff current comparator. Circuit consists of two source followers' stages and one inverter in the feedback loop formed by the transistors M18-M20.The applied current at the input of the first source following stage is converted into its equivalent voltage at the input of the feedback loop.

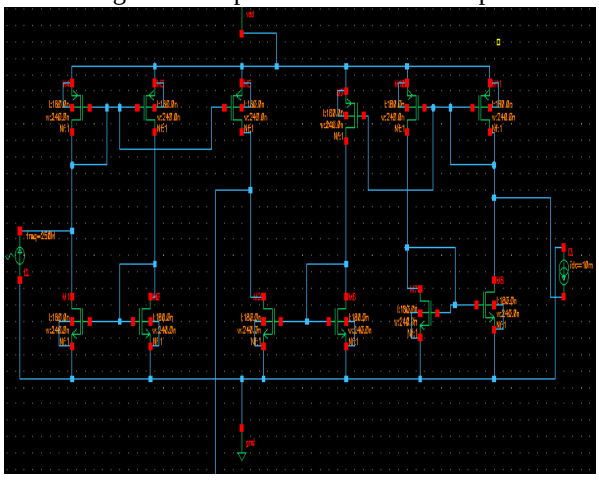

Fig2.The current difference circuit

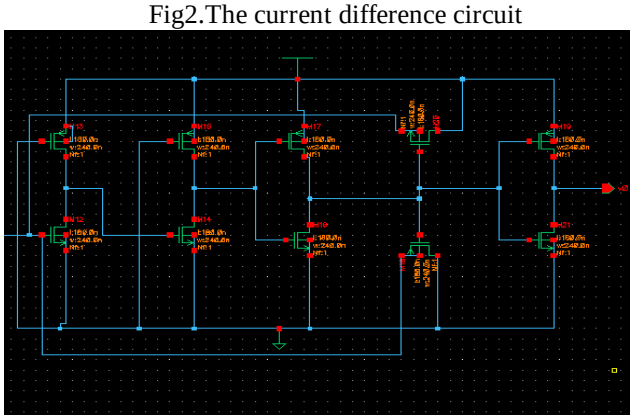

Fig3.Reference current comparator

This feedback loop acts as trans impedance gain stage. Because the applied difference current is converted into its equivalent voltage. This in turn is converted into full swing output voltage by the output inverter. But the power consumed by the improved current compactor is 0.646mW, which is the limitation of the figure3.so in order to reduce the power figure 3 is modified to consume less power. The next section explains the various techniques used for reducing power.

IV.LOW POWER TECHNIQUES:

For the DSM (Deep submicron technology) circuit, the size of CMOS integrated circuits is shrinking day by day. So the power dissipation is a major issue for the short channel devices and the performance of digital integrated circuits is challenged by higher power consumption. On the other side, scaling of the transistor improves the density and functionality of a chip. Scaling also results in higher speed of operation and improves the performance of the device.
So to reduce the power consumption number techniques are available in the CMOS technology. They are sleep transistor approach, LECTOR technique, Stacking technique, dual Vth, multi Vth, optimal stand by input vector selection, body bias.

A. INPUT VECTOR SELECTION

Sub threshold leakage current contributes majorly to leakage power dissipation. The different inputs applied to the gates of the different transistors make the transistor on and off. So by properly selecting input vectors at the input of the different transistors we can reduce the power.

B.DUAL VTH TECHNIQUE

In Dual Vth technique there are two threshold values. They are low vth and low vth. For low vth the speed is more but has sub threshold leakage current. Where as in high vth case sub threshold current is low and thereby reducing the power dissipation. So in this method low vth is used for speed and high vth is used for reducing power dissipation.

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C. MULTI-THRESHOLD-VOLTAGE CMOS

In a Multi-Threshold-Voltage CMOS (MTCMOS) circuit extra transistors are introduce in the transistors are inserted in the circuit. The extra transistors are inserted in between power supply and main transistors. These inserted transistors have high threshold voltage vth.The main transistors have low threshold voltage compared to the extra inserted transistors. When the circuit is in working condition the extra transistor are operated in sleep mode. The main transistors have low threshold voltage which enhances the circuit performance. In the standby mode the extra transistors which have high threshold voltage vth are set to high. The leakage in the original transistors is suppressed by low leakage current of the of the extra transistors. By using the high threshold voltage transistors power can be reduce in this way.

D.SLEEP TRANSISTOR TECHNIQUE

In CMOS we have pull up network and pull down network. This technique is MTCMOS, which adds high-Vth sleep transistors between pull-up networks and Vdd and pull-down networks and gnd while for fast switching speeds, low-Vth transistors are used in logic circuits. Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep.

E. TRANSISTOR STACKING

The leakage current when produce by the two serially connected transistors is less than the leakage current produced by the on off transistor. This is technique is called stacking technique. With this stack of transistors the leakage power can be reduced significantly.

V.PROPOSED CURRENT COMPATOR

The improved current comparator is shown below. The first four stages acts as gain improving stage. In the first four stages the source follower circuit is used to improve the gain. The difference current is applied to the input of the first source follower stage. The feedback loop consists of four source follower stages and inverter followed by the feedback transistors. The operation of the proposed is same as the reference circuit. The current difference is applied at the gate node of the transistor M30 and it is converted into equivalent voltage at the input of the feedback transistors M20-21.This voltage in turn is converted into full output voltage by the output inverter. The first four stages are used for improving the gain. The gain of the proposed current comparator is approximately 180V/µA which is very high compared to the reference circuit.

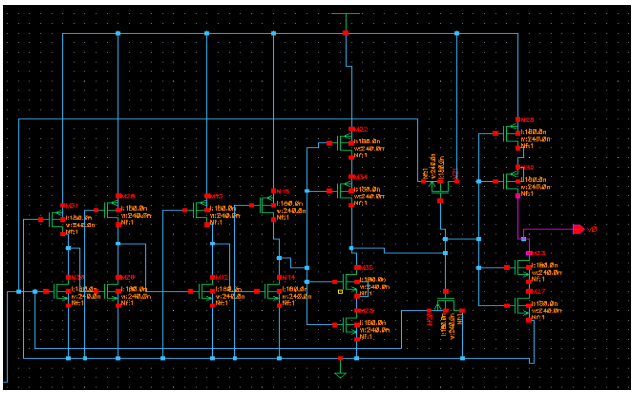

Fig4.Proposed improved circuit

To reduce the power consumed by the circuit, stacking technique is used. The stacking technique is used in the inverter stage. The stacking transistors are those transistors which are added in series in the original transistors to reduce the power. The extra transistors added in series with the main transistors increase the total resistance from the vdd to the ground. Because some transistors are on and off. So this in turn decreases the power consumed by the circuit.

VI.SIMULATION RESULTS

For the verification of the propose circuit 180nm technology is used. The simulation results of the proposed circuit are shown below figure 5.Transient behavior of the proposed circuit is shown in figure5. We have two inputs in the circuit. One is I_1 and other one I_2.By taking I_1 as varying input current and I_2 as reference current transient analysis is performed. So the output of the proposed current comparator is HIGH when I_1 is greater than I_2 and it is LOW when I_1 is less than I_2.For the transient analysis I1 is taken as sinusoidal waveform and I2 is taken as DC current.

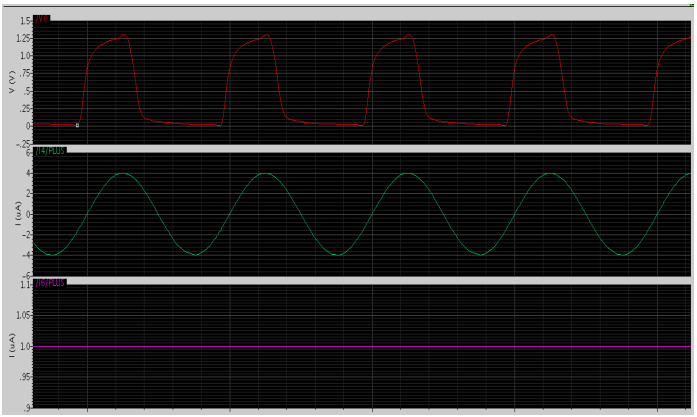

Fig5.Transient waveforms

The gain of the circuit is increased to 180V/µA which the transimpedance of the circuit. The propagation is delay is 0.606ps.Where as for the reference circuit the propagation delay is 0.86ns.

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The variation of output voltage with respect to the current difference is shown in the below figure.

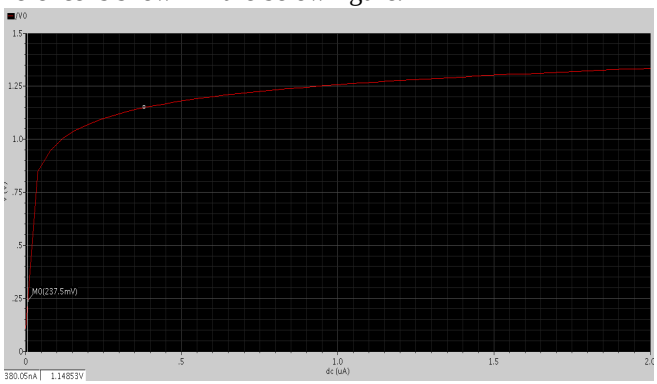

Fig6.difference current vs output voltage

VI. CONCLUSION

A current comparator has been proposed in this paper, which has power consumption of 0.5mw and has a propagation delay of 0.606ns at input current range of 1μA. Our comparator works at 29.53% increase in high speed and 21.36% decrease in power consumption by using the use of STACKING technique.

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