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A Very–High Impedance Current Mirror with High Output Accuracy for Bio-medical Applications Using 65nm technology

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ABSTRACT

Bio-medical applications require very high impedance and a low voltage current mirror. This paper is about a very high impedance current mirror using 65nm technology which operates precisely for a range of output voltages with optimum number of transistors. MOS transistors are used in the circuit which is used to take the sample of the output current and give it to the input side. This negative feedback action makes both the output and input currents equal. The proposed circuit is also insensitive to the biasing current, this yields an increase in output impedance when compared to super Wilson current mirror thus offering a solution to reduce the effect of low output impedance of deep submicron CMOS transistors used in low voltage current sources and current mirrors. A MOS version of the proposed current mirror was implemented using UMC-65nm CMOS process and simulated using Cadence to validate its performance. The output mirror current was inspected for the input voltage range from 30μA to 50μA.

I. INTRODUCTION

With recent advances in CMOS technologies, integration of radio-frequency (RF) circuits, baseband signal processing, and also sensors on a same chip has led to a terrific growth of interest in smart medical implants and their applications. Recently biomedical circuits' demand large-voltage compliance current sources and current mirrors with a high output impedance. Very high output resistance and low input resistance and precise operation for high output voltage range are required for high accuracy. Low-voltage operation requires low output and input voltages also low supply requirements for the control circuitry used to improve the mirror's output and input resistance.

Ultra-low power consumption and low supply voltage of less than 1 V or 1V are critical to make sure that the batteries can run over a long period of time. Recent developments in deep sub-micron CMOS technologies are found to be very apt to reach this goal, since deep sub-micron CMOS transistors can be operated in weak inversion up to the GHz region with a satisfactory gain. Also the low threshold voltage of the CMOS transistors allows designing of the analog circuits which can operate around 1 V. However, reducing the supply voltage and low output resistance of transistors in these deep sub-micron CMOS processes make it very burdensome to implement current mirrors and current sources or sinks that offer very-high output impedance over a large output voltage range.

The basic operation and performance of the proposed current mirror is described in section II. The results of simulation are presented in section III and the conclusions are stated in section IV.

II. Basic operation of the circuit

The basic idea of this circuit is from high-swing super-Wilson, which offers very high output impedance using a negative feedback and shown in Fig. 1. The transistors M1-M4 forms a current mirror which is used to sample the output current I_{out} and compares it with the input current I_{in}. High output impedance in Wilson current mirror is achieved as follows. If there is any increase in the output current due to an increase in the output voltage through output transistor's early effect is sensed by the simple current mirror whose input is in series with the output transistor. The output current is fed back to the input node by the simple mirror, reducing the gate voltage of the output transistor, thus reducing its channel current and compensating the original current increase. Because a transistor's incremental transconductance gain is typically much larger than its incremental output conductance, the input voltage does not normally need to move by very much to compensate such output current variations.

The output impedance of the Wilson current mirror circuit is directly proportional to the loop gain which comprises the combination of current source load and Common Source amplifiers M1. The output impedance r_{out} of the high-swing super-Wilson current mirror can be approximated as:

$$r_{out} = g_{m1} r_{01} r_{05}$$

Where r_{01} and g_{m1} are the output resistance and transconductance of transistors M1 respectively and r_{05} is the output resistance of transistors M5.

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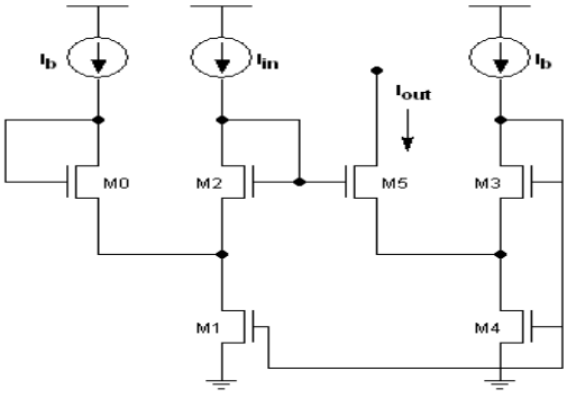

Fig.1. Super Wilson Current Mirror

The improved version of the super Wilson current mirror circuit is shown in fig.2. In this circuit, the drain symmetry for the transistors M2-M4 is obtained without the need of an auxiliary current source. It is achieved by placing Diode-connected PMOS transistors in place of auxiliary current sources. The transistors M2-M4 are formed as current mirror and are used to achieve high output impedance. The diode connected transistor M1 is altered as a cascoded one. The transistors M2-M4 are used to sample the output current I_{out} and compare it with the input current I_{in}, which changes the conduction of the transistor M5. Thus the output current I_{out} is made equal to the input current I_{in}. The transistors M6-M7 which are diode connected acts as an active load and increase the output impedance also increases the output current.

The resistance which has increased is equal to

$$r_{out} = \frac{1}{g_{o2}}\left(\frac{1+\frac{g_{o2}}{(g_{m4}+g_{o4})}+\frac{g_{m2}}{(g_{m4}+g_{o4})}+\frac{g_{m2}}{g_{m4}+g_{o4}}(g_{m1}||g_{m6})g_{m2}+(g_{m1}||g_{m6})g_{o2}+g_{m2}g_{o2}}{g_{o1}g_{o2}}\right)$$

Where g_{o1}, g_{o2}, g_{o4}, g_{o5} are the output conductance and the g_{m1}, g_{m2}, g_{m4}, g_{m5} transconductance of the transistors M1, M2, M4 and M5.

If the transconductance g_m of the transistors is much larger than their output conductance g_0, then the equation is:

$$r_{out}=(g_{m1}//g_{m6})(g_{m2})(r_{01})(r_{02})(r_{05})$$

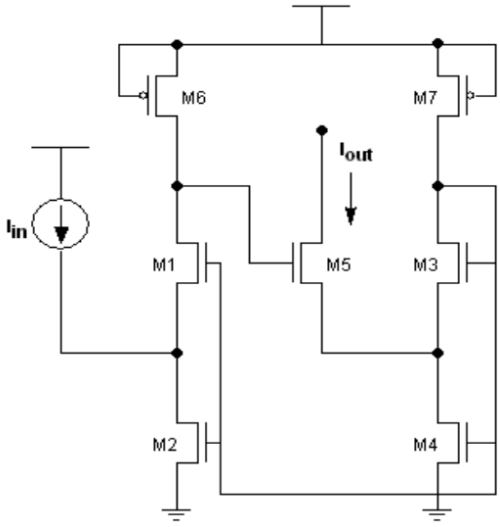

Fig.2. Improved Super Wilson using 180nm FET

Proposed Current mirror using 65nm technology*:*

The circuits implemented previously were based on 180nm technology, but in the proposed circuit 65nm technology is used that is the channel length of the transistor reduces to 65nm also an extra transistor is added to the circuit to improve steady output current for a wide range of output variations of the current mirror. The output resistance of the modified 65nm technology circuit is given as

$$r_{out} = \frac{1}{g_{o2}}\left(\frac{1+\frac{g_{o2}}{(g_{m4}+g_{o4})}+\frac{g_{m2}}{(g_{m4}+g_{o4})}+\frac{g_{m2}}{g_{m4}+g_{o4}}(g_{m1}||g_{m6})g_{m2}+(g_{m1}||g_{m6})g_{o2}+g_{m2}g_{o2}}{g_{o1}g_{o2}}\right)$$

Where g_{mt} is the combined trans conductance of M1 and M0 transistors also g_{0t} is the total output conductance of the transistors M1 and M0.

This output resistance can be approximated when considered that the transconductance gm of the transistors is much larger than their output conductance g0 as:

$$r_{out}=(g_{mt}//g_{m6})(g_{m2})(r_{01})(r_{02})(r_{05})$$

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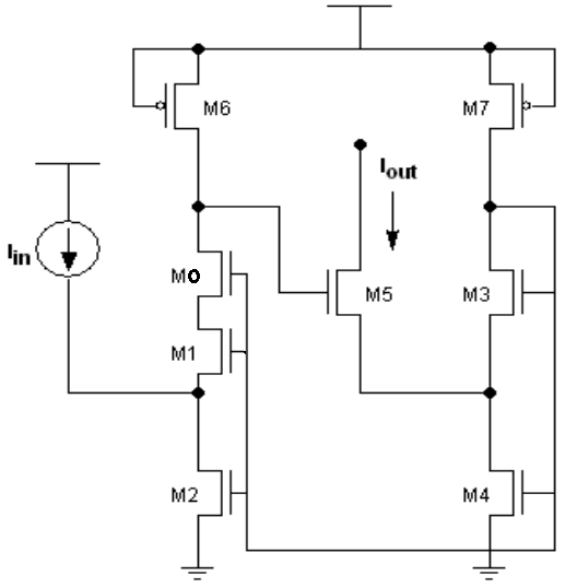

Fig.3. Current Mirror Using 65nm technology with added transistor

If the previous papers circuit is implemented as it is using 65nm technology, the impedance is good enough but the output is not following the input that is the output is less in magnitude when compared with the input (shown in figure 6). The added transistor improves the output current by boosting up the gate voltage of the output transistor (shown in figure 7).

III. Results of Simulation

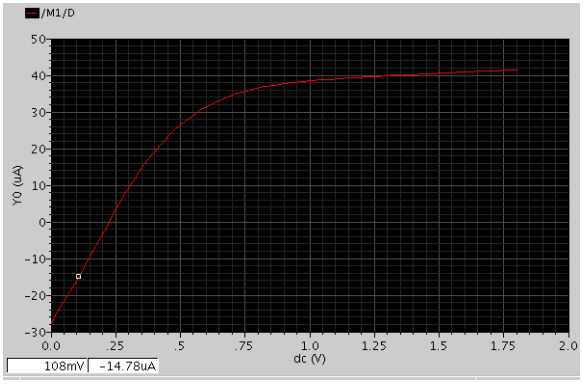

Fig.4. Voltage Vs Current graph of Wilson Current Mirror at 40µA

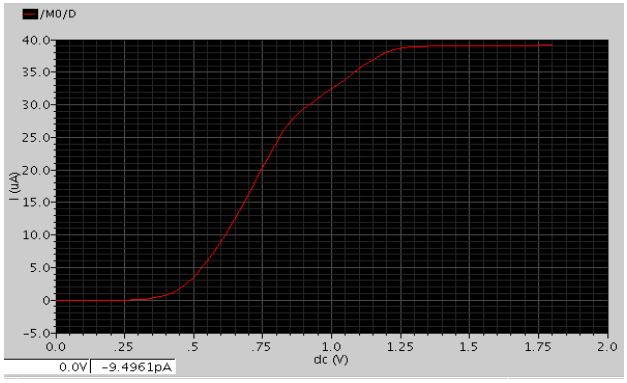

Fig.5. Voltage Vs Current graph of improved Current Mirror using 180nm technology

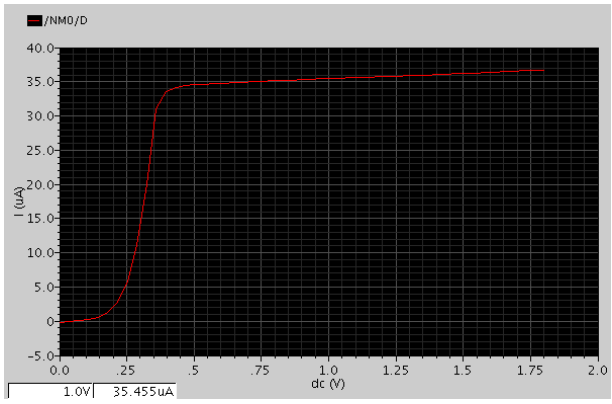

Fig. 6. Voltage Vs Current graph of Current Mirror using 65nm technology

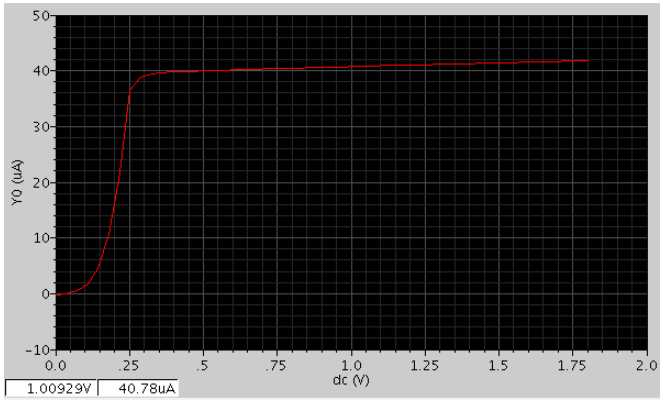

Fig.7. Voltage Vs Current graph of improved Current Mirror using 65nm technology with added transistor

IV.CONCLUSION

The proposed circuit offers very high impedance along with a very high accuracy of output current for a large variation of output voltage. Thus for a large variation in output voltage we can get a steady output current for the input current range from 30µA to 50µA.

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