

# Reversal the Power Flow in the Looped Electrical Network by Using a Cascaded H-bridge D-SSSC



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**Abstract**— In this paper the distributed generation is connected directly to the medium voltage link. The conventional radial electrical distribution system will change to loop or even meshed system due to the deregulation of electrical system and connection of Distributed Generation to Medium and Low voltage in future. Looping the feeders in the conventional distribution system has some benefits which are discussed more precisely in this paper. These benefits will be voltage regulation, increasing reliability, loss reduction, avoiding congestion in cables and facilitating use of distributed generation. Distribution Static Synchronous Series Compensator (D-SSSC) is able to control the power flow between two feeders from different substations can provide controllable compensating voltage over an identical capacitive and inductive range, independently of the magnitude of the line current. Cascaded H-bridge inverter can then be configured with multiple modules. Such a system does not need a transformer to provide isolation, and the system can be constructed in a cost effective manner. This control strategy is fail to operation while the power reference is reversing due to loosing the current phase track at low and zero line current. In this paper the feasibility of a DSSSC for reversing the power flow is discussed and a new control strategy based on voltage phase track is proposed.

*D-SSSC, Cascaded H-bridge inverter, power flow control, Carrier based PWM*

## I. INTRODUCTION

Increased demand of energy sources is to be carried almost in totality by the electrical distribution system. The prime reason is ever increasing demand. Alternative energy sources are not utilized to their potential. Use of solar energy is still in infancy and not very popular. At present, very few houses and public buildings use passive solar energy gain. The conventional radial distribution network is not able to handle these new demands and needs to change. The Radial distribution system is the cheapest to build and simpler also. But For achieving the total generation of DGs the distribution network radial configuration is changed to the loop or meshed configuration by using a power electronic device in the connection point to control the power flow.

Electric power flow though an alternating current transmission line is a function of the line impedance, the magnitudes of the sending-end and receiving-end voltages, and the phase angle between these voltages. The power flow

can be increased by inserting an additional capacitive reactance in series with the transmission line, thereby decreasing the effective reactance of the transmission line between its two ends. A distribution Synchronous Series Compensator (DSSSC), which is a solid-state voltage source inverter, injects an almost sinusoidal voltage, of variable magnitude, in series with a transmission line.

Most of the injected voltage which is in quadrature with the line current emulates an inductive or a capacitive reactance in series with the transmission line. This emulated variable reactance, inserted by the injected voltage source, influences the electric power flow in the transmission line. A DSSSC is operated with an energy storage system. A seven level cascaded H-bridge which is used as a D-SSSC in series to line.

The cascaded multilevel inverter consists of a series of H-bridge inverter. The general purpose of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, like batteries, fuel cells, solar cells, and ultra capacitors. The resulting phase voltage is obtained by the addition of the voltages generated by the different cells by opening and closing the switches of each cells suitably. The most attractive features of multilevel inverters are, they draw input current with very low distortion and they can generate output voltages with extremely low distortion. The harmonics orders and magnitude are depends up on the type of inverter and the control techniques. For example in single phase VSI, the output voltage waveform typically consists only of odd harmonics. The even harmonics are not present due to the half wave symmetry of the output voltage harmonics.

Multilevel inverter structures have the particular advantages of operation at high dc-bus voltages, achieved using series connections of switching devices and a reduction in output voltage harmonics, achieved by switching between multiple voltage levels. Modulation control of any type of multilevel converter is quite challenging, and much of the reported research is based on somewhat heuristic investigations.

Carrier-based PWM forms a common thread in this work, but particular approaches are generally applied only to individual inverter structures. Most carrier-based PWM schemes for diode-clamped inverters derive from the carrier disposition strategy.

The conventional control strategy uses the phase angle of line current by a phase locked loop and injects a voltage in phase to line current to maintain the DC bus voltage and a voltage in quadrature to the line current for control the power flow. But when the power flow is going to reverse the line current PLL is not able to work properly due to the low and zero current at that point. Losing the line current phase track will fail the whole control strategy. In this paper the electrical distribution system modeling for reversing the power flow is discussed and a new control strategy based on tracking the phase of feeder voltage is proposed.

II. DISTRIBUTION STATIC SYNCHRONOUS SERIES COMPENSATOR

Electric power flow through an alternating current transmission line is a function of the line impedance, the magnitudes of the sending-end and receiving-end voltages, and the phase angle between these voltages. The power flow can be decreased by inserting an additional inductive reactance in series with the transmission line, thereby increasing the effective reactance of the transmission line between its two ends. Also, the power flow can be increased by inserting an additional capacitive reactance in series with the transmission line, thereby decreasing the effective reactance of the transmission line between its two ends.

In order to control the power flow of the transmission line, the effective line reactance is controlled by using fixed or thyristor-controlled series capacitors or inductors. With the use of the impedance compensation controller, a *distribution Static Synchronous Series Compensator* (DSSSC), which is a solid-state voltage source inverter injects an almost sinusoidal voltage, of variable magnitude, in series with a transmission line. This injected voltage is almost in quadrature with the line current. A small part of the injected voltage which is in phase with the line current provides the losses in the inverter. Most of the injected voltage which is in quadrature with the line current emulates an inductive or a capacitive reactance in series with the transmission line. This emulated variable reactance, inserted by the injected voltage source, influences the electric power flow in the transmission line. When an SSSC injects an alternating voltage leading the line current, it emulates an inductive reactance in series with the transmission line causing the power flow as well as the line current to decrease as the level of compensation increases and the DSSSC is considered to be operating in an inductive mode. When an DSSSC injects an alternating voltage lagging the line current, it emulates a capacitive reactance in series with the transmission line causing the power flow as well as the line current to increase as the level of compensation increases and the SSSC is considered to be operating in a capacitive mode.

Fig. 1 shows a single line diagram of a simple transmission line with an inductive reactance,  $X_L$ , connecting a sending-end voltage source,  $v_s$ , and a receiving-end voltage source,  $v_r$ , respectively.

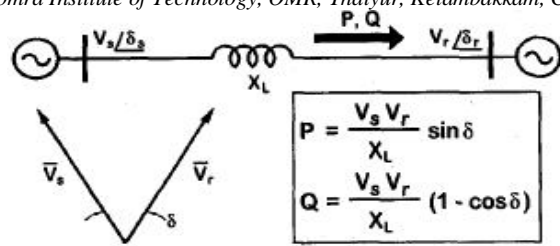


Fig. 1 Power Transmission System

The real and reactive power ( $P$  and  $Q$ ) flow at the receiving-end voltage source are given by the expressions

$$P = \frac{V_s V_r}{X_L} \sin(\delta_s - \delta_r) = \frac{V^2}{X_L} \sin \delta \tag{1a}$$

and

$$Q = \frac{V_s V_r}{X_L} (1 - \cos(\delta_s - \delta_r)) = \frac{V^2}{X_L} (1 - \cos \delta) \tag{1b}$$

where  $V_s$  and  $V_r$  are the magnitudes and  $\delta_s$  and  $\delta_r$  are the phase angles of the voltage sources  $v_s$  and  $v_r$ , respectively. For simplicity, the voltage magnitudes are chosen such that  $V_s = V_r = V$  and the difference between the phase angles is  $\delta = \delta_s - \delta_r$ .

An SSSC, limited by its voltage and current ratings, is capable of emulating a compensating reactance,  $X_q$ , (both inductive and capacitive) in series with the transmission line inductive reactance,  $X_L$ . Therefore, the expressions for power flow given in equation (1) become

$$P_q = \frac{V^2}{X_{eff}} \sin \delta = \frac{V^2}{X_L(1 - X_q / X_L)} \sin \delta \tag{2a}$$

and

$$Q_q = \frac{V^2}{X_{eff}} (1 - \cos \delta) = \frac{V^2}{X_L(1 - X_q / X_L)} (1 - \cos \delta) \tag{2b}$$

where  $X_{eff}$  is the effective reactance of the transmission line between its two ends, including the emulated variable reactance inserted by the injected voltage source of the SSSC. The compensating reactance,  $X_q$ , is defined to be negative when the SSSC is operated in an inductive mode and positive when the is operated in a capacitive mode.

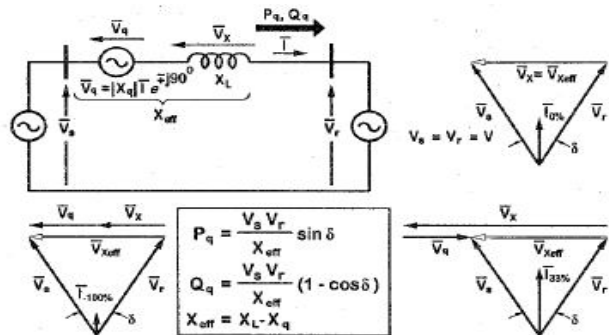


Fig.2. A phaser diagram static synchronous series compensator operated in inductive and capacitive modes

Fig. 2 shows an example of a simple power transmission system with an SSSC operated both in inductive and in capacitive modes and the related phasor diagrams. The line current decreases from  $I_0\%$  to  $I_{100}\%$ , when the inductive reactance compensation,  $-X_q/X_L$ , increases from 0% to 100%. The line current increases from  $I_0\%$  to  $I_{33}\%$ , when the capacitive reactance compensation,  $X_q/X_L$ , increases from 0% to 3%.

generated by the different cells. To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded inverter is defined by

$$m = 2s + 1 \tag{3}$$

III.CASCADED H-BRIDGE INVERTER

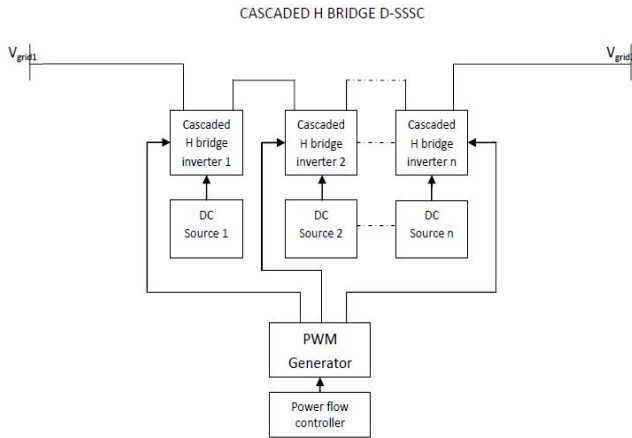


Fig. 3 Cascaded H bridge D-SSSC

Fig. 3 shows a cascaded H-bridge inverter which is used as a D-SSSC in series to line. The cascaded multilevel inverter consists of a series of H-bridge inverter. The general purpose of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, like batteries, fuel cells, solar cells, and ultra capacitors.

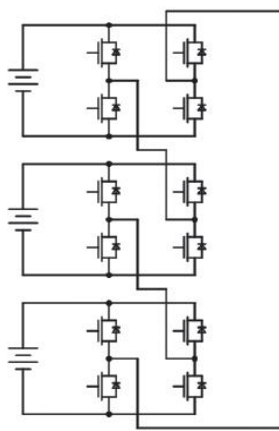


Fig.4 Seven-level cascaded H bridge inverter

Fig.4 shows the power circuit for one phase leg of a three-level inverter with four cells in each phase. The resulting phase voltage is synthesized by the addition of the voltages

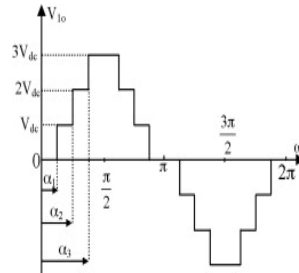


Fig 5 Waveform showing a seven-level output phase voltage

Each single-phase full-bridge inverter generates three voltages at the output:  $+V_{dc}$ , 0, and  $-V_{dc}$ . The resulting output ac voltage swings from  $-3V_{dc}$  to  $+3V_{dc}$  with seven levels, and the staircase waveform is nearly sinusoidal, even without filtering. The switching strategy of the circuit will be explained in the next chapter. The output waveform is shown in the Fig.5. Obviously no even harmonic components are available in such a waveform. To minimize THD, all switching angles will be numerically calculated.

IV. MULTI LEVEL INVERTER MODULATION CONTROL SCHEMES

Too many modulation strategies can be used for switching modulation like Phase Shift Carrier PWM, Phase Disposition Carrier PWM, Phase Opposition Disposition Carrier PWM and etc. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the conventional SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. By generalizing, for an 'n' level multilevel inverter, (n-1) carriers are needed. The implementation of the various carrier PWM techniques that is possible for multi-level inverters. Level Shifted PWM (LSPWM) leads to less distorted line voltages. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topology. Alternative phase opposition disposition (APOD) is used to generate switching signals to inverter switching devices. In APOD, each carrier is phase shifted by 180 from its adjacent carrier. APOD only generates carrier sideband harmonics in the phase-leg voltage. While triplen multiples of these harmonics cancel in the line-to-line voltage.

As a result of not including any auxiliary source power this strategy can control only the active or reactive parts of power flow. This control strategy uses two control loop, one for maintaining the DC bus voltage at its reference value which produces the in phase part of injected voltage with the line current and the second loop, control the amount of power flow in the connected line which makes the quadratic part of injected voltage with current. The reference current, active or reactive power is compared with the actual value and passing through a PI controller generates the quadratic part amplitude. The power flow can be increased by acting DSSSC as additional capacitive impedance in series with the transmission line, and decreased by acting it as additional inductive impedance in series with the transmission line. In this control technique two PI controllers are used. One of the PI output controllers is used to identify the mode of operation. The reference DC bus voltage is compared with actual DC bus voltage using another PI controller the amplitude of in phase part of injected voltage is as shown in fig 6. But in crossing from the zero current for reversing the power flow the PLL is not able to produce the well results and lose the current phase track which causes the mal function of whole control system.

So for solving this problem another control strategy is proposed which uses the phase of feeder voltage instead of current phase. As a result of not having the current phase, it is not possible to maintain the DC bus voltage by controlling the in phase part of injected voltage directly. So the new control strategy which is showed in Fig. 7 uses the variable DC bus voltage. The active power or current is compared to the actual value and passing a PI controller the voltage reference is produced. In this control strategy, the DC bus voltage is not fixed and varies by the changing in power flow while the modulation index is fixed at (0.9). This reference is compared with the actual DC bus voltage value and using another PI controller, a phase displacement  $\gamma$  is obtained. As a result of having one of feeder voltages close to the injected voltage, it is easy to use it as a reference for phase synchronization. Note that the feeder voltage unlike the feeder current has no changes during reversal of power flow and becomes a good choice for synchronization. The same control strategy like Fig. 7 with current PLL is achievable while it is suitable for one direction power flow demanding. In this strategy the DC bus voltage is more than the difference voltages between feeders at connection point when the power flow is reversed. Also using the voltage phase, there is no need to change the control strategy while power flow is reversed.

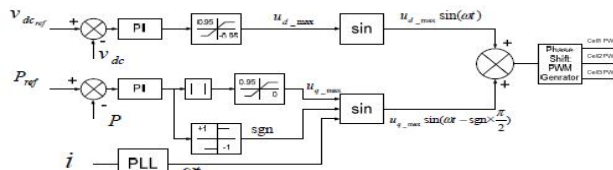


Fig 6. Power flow control with current phase locked loop

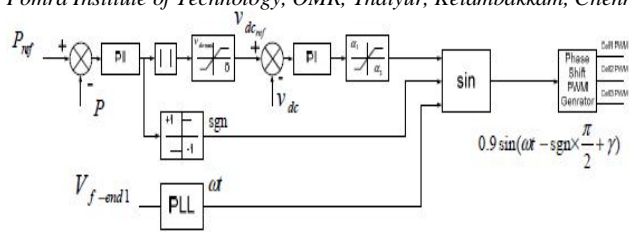
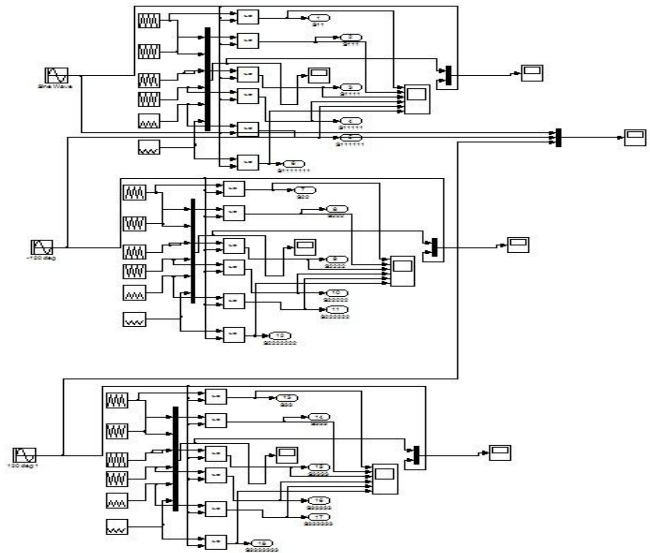


Fig.7 Power flow control with voltage phase locked loop

VI. SIMULATION RESULTS



[1] Fig.8 Simulink diagram of APODPWM Generator

The simulink diagram of alternative phase opposition disposition PWM (APODPWM) Generator is as shown in Fig.8. In this PWM generator, pulses to the cascaded H bridge inverters are generated by the alternative phase opposition disposition PWM method. For seven level cascaded H bridge inverter, this strategy arranges six triangular carriers with same frequency and amplitude in repeating sequence. So they occupy contiguous bands over the range +150Vdc to -150Vdc. A single sinusoidal reference is then compared with each triangular carriers and the switched output voltage for the converter is obtained. This switched output voltage is generated for the three phases and given to the gate terminal of the each MOSFET (Metal Oxide Semi Conductor Field Effect Transistor) device in seven level cascaded H bridge inverter. Triangular carriers and sinusoidal reference wave forms are shown in the fig.9.

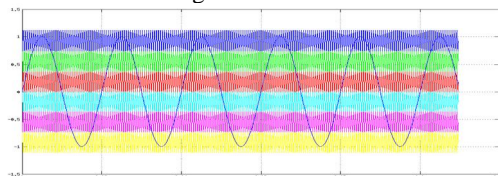


Fig.9 Output wave form of APODPWM Generator

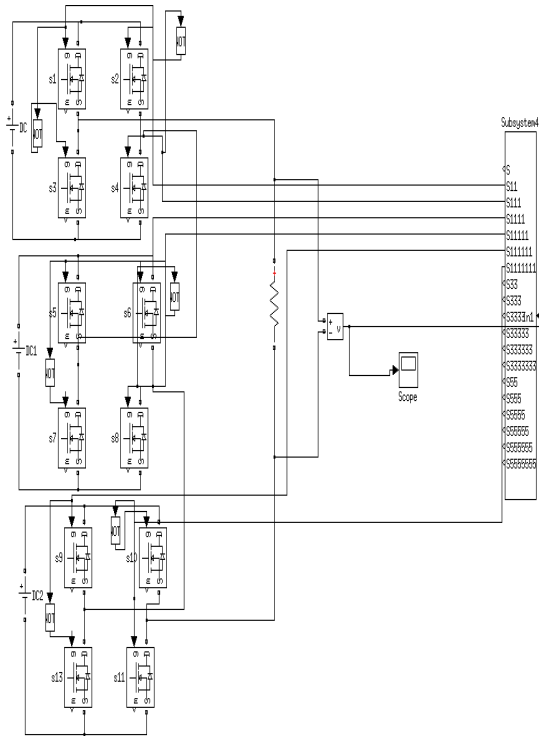


Fig. 10 simulink diagram of cascaded H bridge inverter

Fig.10 shows the power circuit for single phase leg of a seven level inverter with four MOSFETs in each phase, which is based on the series connection of single-phase inverters with separate dc sources. The resulting phase voltage is synthesized by the addition of the voltages generated by the each switching device.

Each single phase full bridge inverter generates three voltages at the output +50Vdc, 0 and -50Vdc. The single phase voltage of this inverter is swings from -150Vdc to +150Vdc with seven levels and the staircase waveform in nearly sinusoidal. The single phase and three phase output voltage waveform is shown in as shown in fig.11 and fig.12. The cascaded multilevel inverter is best suited for harmonic and reactive compensation and other utility applications.

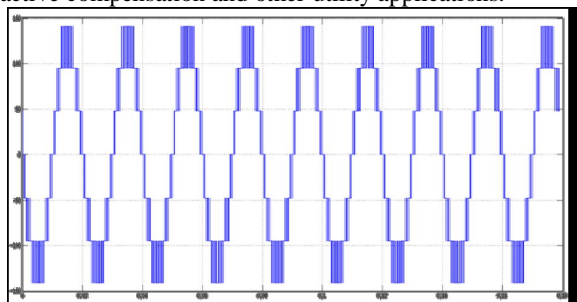


Fig.11 Three phase output of seven levels H bridge inverter

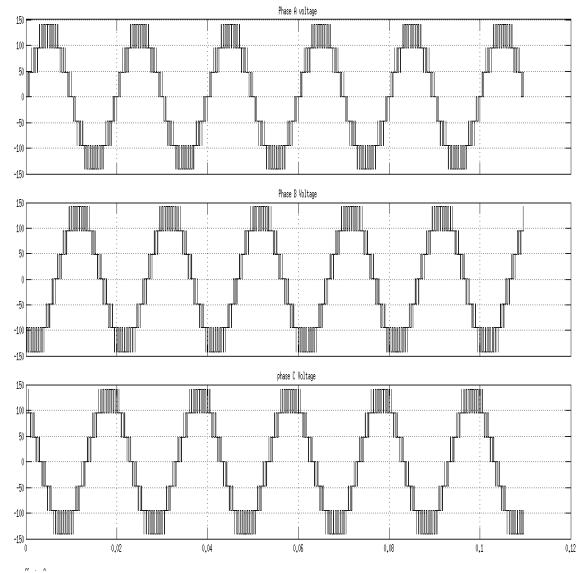


Fig: 12. Three phase output of seven levels H bridge inverter

VII.CONCLUSION

In this paper power flow control of a DSSSC in the electrical distribution system is described. The DSSSC is used to control the power flow between two feeders from different substations. The conventional control strategy is fail to operation while the power reference is reversing due to loosing the current phase track at low and zero line current. The new control strategy is discussed to reverse the power flow properly. This strategy uses one of the feeders' voltages to obtain the synchronization phase by a PLL unlike the strategies which use the line current for phase synchronization. In this phase I, seven level cascaded H-bridge inverter with carrier based PWM is simulated and the output is shown.

REFERENCES

- [1] L. Tolbert, F.-Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 36–44, Jan./Feb.1999.
- [2] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Applicat.*, vol. 37, pp. 611–618, Mar./Apr.2001.
- [3] L. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 1098–1107, Sept./Oct. 1999.



- [4] Y. Liang and C. O. Nwankpa, "A new type of STATCOM Based on cascading voltage-source inverters with phase-shifted unipolar SPWM," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 1118–1123, Sept./Oct. 1999.
- [5] B. P. McGrath, D. G. Holmes, M. Manjrekar, and T. A. Lipo, "Improved modulation strategy for a hybrid multilevel inverter," in *Conf.Rec. IEEE-IAS Annu. Meeting*, 2000, pp. 2086–2093.
- [6] J. M. Gonzalez, C. A. Canizares, J. M. Ramirez, "Stability Modeling and Comparative Study of Series Vectorial Compensators," *IEEE Trans.Power Del.*, vol. 25, no. 2, pp. 1093--1103, April 2010.
- [7] L. Gyugyi, C. D. Schauder, and K. K. Sen, "Static synchronous series compensator: A solid-state approach to the series compensation of transmission lines," *IEEE Trans. Power Del.*, vol. 12, no. 1, pp. 406–417, Jan. 1997.417, Jan. 1997. J
- [8] K. K. Sen, "Static synchronous series compensator: Theory modeling and applications," *IEEE Trans. Power Del.*, vol. 13, no. 1, pp. 241--246,Jan. 1998.
- [9] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.