International Journal of Advanced Trends in Computer Science and Engineering, Vol.2, No.2, Pages : 203-208 (2013) Special Issue of NCRTECE 2013 - Held during 8-9 February, 2013 in SMK Fomra Institute of Technology, OMR, Thaiyur, Kelambakkam, Chennai

Modeling and Simulation of PFC SEPIC Converter fed PMBLDC Drive for Mining Application



C.Umayal Assistant Professor, Department of EEE, Easwari Engineering College, Chennai, India Chennai, India cumayal@yahoo.com

Abstract— Digital Simulation of a bridgeless Power Factor Correction (PFC) SEPIC converter based adjustable speed controlled VSI fed PMBLDC motor for mining applications is presented in this paper. The proposed topologies are designed to achieve near unity power factor in a simple and effective manner. The proposed speed control scheme has the concept of DC link voltage control proportional to the desired speed of the PMBLDC motor. The speed is regulated by a PI controller. The proposed converter combines the PFC and DC link voltage control in single stage and uses a single controller. This is designed for continuous conduction mode (CCM) of operation. Detailed analysis, modeling and performance evaluation is done for a 0.5kW, 1800 rpm PMBLDC Drive. The proposed PFC converter provides less than 5% total harmonic distortion (THD) in current at AC mains with near unity power factor.

Keywords- PFC; Converters; SEPIC; Power factor; total harmonic distortion; PMBLDC Drive

I. INTRODUCTION

Permanent Magnet Brushless DC (PMBLDC) motors are preferred motors for mining applications since they do not produce sparking, due to the absence of brushes. They also have better speed versus torque characteristics, high dynamic response, and high efficiency, noiseless operation, higher speed ranges and long operating life. Torque to weight ratio is higher, enabling it to be used in applications where space and weight are critical factors. Recent developments in power electronics, microelectronics and modern control technologies have greatly influenced the wide-spread use of permanent magnet motors [1-2]. The major classifications of Permanent Magnet motors are permanent magnet synchronous motor (PMSM) and Permanent Magnet Brushless DC motors (PMBLDCM). While PMSM has sinusoidal back-EMF waveform, the BLDC motor has trapezoidal back-EMF waveform. Comparing with conventional DC motors, BLDC motors do not have brushes for commutation. Instead, they are electronically commutated. A new generation of microcontrollers and advanced electronics has overcome the challenge of implementing required control functions, making the BLDC motor more practical for a wide range of use, including mining applications [3]-[5].

The PMBLDC drive consists of a VSI and the PMBLDC motor, which is usually powered through a diode bridge rectifier fed from a single-phase AC mains followed by a DC

D.Saranya Devi PG Scholar, Department of EEE Easwari Engineering College Chennai, India adithisaranyadevi@gmail.com

link capacitor. This arrangement suffers from power quality disturbances such as poor power factor, increased total harmonic distortion of current at input AC mains. This is due to the uncontrolled charging of the DC link capacitor which results in a pulsed current waveform, which has a peak value higher than the amplitude of the fundamental input current at AC mains.

Furthermore, the power quality standards for low power equipment such as IEC 61000-3-2 [6] emphasize on low harmonic contents and near unity power factor current to be drawn from AC mains by these equipment. Hence use of a PFC converter has become inevitable for a PMBLDCM drive. High quality converters are used to interface AC line and DC load. Their aim is to make the load appear as resistive load so that a unity power factor is achieved even in the presence of distorted line voltage.

This paper presents the use of a SEPIC converter as a single stage PFC converter for a PMBLDC motor drive for mining applications, to improve the power factor, thereby satisfying the power quality norms. A detailed modeling, design and performance evaluation of the proposed drive is presented for a drive consisting of a PMBLDC motor (48V, 8A) and 1800 rpm. The hardware is implemented using low cost embedded controller. The experimental results are compared with the simulation results.

II. PFC CONVERTERS FOR PMBLDC DRIVES

A voltage source inverter can run the BLDC motor by applying three phase square wave voltages to the stator winding of the motor .A variable frequency square wave voltage can be applied to the motor by controlling the switching frequency of the power semiconductor switches. The square wave voltage will induce low frequency harmonic torque pulsation in the machine. Also variable voltage control with variable frequency operation is not possible with square wave inverters. Even updated pulse-width modulation (PWM) techniques used to control modern static converters such as machine drives, power factor compensators do not produce perfect waveforms, which strongly depend on the semiconductors switching frequency. Voltage or current converters, as they generate discrete output waveforms, force the use of machines with special isolation, and in some applications large inductances connected in series with the respective load.

A diode bridge rectifier fed from single-phase AC supply followed by a smoothening DC link capacitor and voltage source inverter are mostly used in a conventional PMBLDC motor drive. The motor is supplied by three-phase rectangular current blocks of 120° duration, in phase with the constant part of the back EMF. These motors need rotor position information at the commutation. Since the commutation points are at every 60° electrical in the three phases, a comparatively simpler controller is required for its commutation. In a PMBLDCM constant torque is achieved by a stable winding current and speed can be varied by varying the terminal voltage of the motor since the back EMF is proportional to motor speed and the developed torque is proportional to the phase current. In this work the motor speed is controlled by controlling the terminal voltage of the motor.

The conventional PMBLDC motor drive is fed from single phase AC supply through the rectifier and VSI. It has pulsed current waveform at AC mains having a peak value higher than the amplitude of the fundamental input current. This is due to uncontrolled charging of DC link capacitor which results in power quality problems in input AC mains such as poor power factor, increased total harmonic distortion in AC mains currents. Various PFC converter topologies are used for such drives [7]. The schematic of the PFC converter fed PMBLDC drive is shown in Fig 1.



Figure 1. Schematic for a PFC Converter fed PMBLDC Drive

In the field of inverter appliance, the application of AC/DC/AC converter is more and more popular. There are serious contaminations from harmonic currents at the mains side, making the products not pass IEC61000-3-2 and IEC61000-3-12 (harmonics standards) successfully. In order to mitigate the harmonic current pollution, most of the household inverters are equipped with power factor corrector as front AC/DC converter, and the input power factor approaches one.

Various types of converters can be applied for power factor correction. They are Cuk converter, canonical switching cell (CSC), bridgeless boost converter, zeta converter .The CSC converter forms the main block for all high frequency switching converters. It is found that the CSC converter has minimum components and is suitable for single phase rectifier circuit with power factor correction [8-10]. For large capacity

Special Issue of NCRTECE 2013 - Held during 8-9 February, 2013 in SMK Fomra Institute of Technology, OMR, Thaiyur, Kelambakkam, Chennai applications SEPIC and ZETA converters are used. But these converters do not take into account the stresses in the components, output voltage regulation which leads to distortion in output voltage and noise interference. The main factors which provide output voltage stabilization for boost PFC circuit with 100Hz switching frequency is described in [11]. But there is no provision for wide variation of output voltage.

III. DESIGN OF THE PROPOSED SEPIC CONVERTER

Single- Ended Primary-Inductor Converter (SEPIC) is a DC-DC converter. It gives output voltage greater than, less than, or equal to that of the input voltage. The output of the SEPIC converter is controlled by the duty cycle of the semiconductor devices. SEPIC provides the input-to-output gain, thus making it popular in battery-powered systems. Unlike buck-boost converter, it has non-inverting output. This is achieved by using a series capacitor to couple energy from the input to the output. Applications of SEPIC are where the output voltage can be above or below than that of the input voltage. SEPIC has pulsating output current. Since the SEPIC converter transfers all its energy via the series capacitor, the capacitor should have high capacitance and current handling capability. The circuit diagram of the SEPIC converter is shown in Fig 2. A SEPIC converter has two pairs of undamped complex poles, compared with other PFC converters, such as fly back converters and boost converters. It is less popular topology for PFC converter design since the control is not simple. Also due to the complexity of control, it is suitable only for very slow varying applications.. The output voltage is not necessarily limited by its input voltage. Furthermore, SEPIC PFC converter does not require an additional DC-DC stage for LED applications. Input current ripple can also be reduced by using two wound inductors. Thus power loss due to current ripple can be reduced.



Figure.2. SEPIC Converter

The working of the SEPIC converter is explained as follows: When the switch S is turned ON, the inductor L_1 is charged from the input voltage source V_{in}. Meanwhile the inductor L_2 takes energy from the capacitor C_2 . The capacitor C_2 supplies the load. As seen from the discussion, both L_1 and L_2 are disconnected from the load. This makes the control characteristics complex. When the switch is turned OFF L_1 charges C₁ and also supplies current to the load. L₂ is also

International Journal of Advanced Trends in Computer Science and Engineering, Vol.2, No.2, Pages : 203-208 (2013)

connected to the load. The output capacitor C_2 has a pulse of current during the OFF time, making SEPIC converter noisier than a buck converter while the input current is non-pulsating.

The SEPIC converter is designed for power factor correction and voltage control at DC link for a VSI fed PMBLDC motor drive. The design equations for the output voltage, V_0 of the PFC converter, input inductance L_1 , intermediate capacitor C_1 , output inductor L_2 and output capacitor C_2 are shown in Equations (1) – (5). D is the duty ratio.

$$V_o = \frac{V_{in}D}{(1-D)} \tag{1}$$

$$L_{1} = DV_{in} / \{f_{s}(\Delta I_{L1})\}$$
⁽²⁾

$$C_{1} = DI_{dc} / \{f_{s}(\Delta V_{c1})\}$$
(3)

$$L_2 = (1 - D)V_o / \{f_s(\Delta I_{L2})\}$$
⁽⁴⁾

$$C_2 = I_{dc} / (2\omega \Delta V_{C2}) \tag{5}$$

Based on these design equations the values of the parameters are set as L1 = 0.0036mH, $C1 = 0.054\mu$ F, L2 = 4.3mH, $C2 = 12 \mu$ F, Torque = 5.5Nm, Inertia of the motor = 0.8mJ, Input voltage = 230V.

IV. MATHEMATICAL MODEL OF THE PMBLDC DRIVE

Modeling and simulation play an important role in the design of power electronics system. The classic design approach begins with an overall performance investigation of the system, under various circumstances through mathematical modeling.

The circuit model of PMBLDC motor is shown in Fig 3.



Figure 3. Motor Circuit Model

Special Issue of NCRTECE 2013 - Held during 8-9 February, 2013 in SMK Fomra Institute of Technology, OMR, Thaiyur, Kelambakkam, Chennai connected to the load. The output capacitor C_2 has a pulse of The voltage equations of the BLDC motor are as follows:

$$V_a = R_a i_a + \frac{d}{dt} (L_{aa} i_a + L_{ab} i_b + L_{ac} i_c) + \frac{d\lambda_{ar}(\theta)}{dt}$$
(6)

$$V_b = R_b i_b + \frac{d}{dt} (L_{ba} i_a + L_{bb} i_b + L_{bc} i_c) + \frac{d\lambda_{br}(\theta)}{dt}$$
(7)

$$V_c = R_c i_c + \frac{d}{dt} (L_{ca} i_a + L_{cb} i_b + L_{cc} i_c) + \frac{d\lambda_{cr}(\theta)}{dt}$$
(8)

In balanced system the voltage equation becomes

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} L_{aa} & L_{ba} & L_{ca} \\ L_{ba} & L_{bb} & _{cb}L \\ L_{ca} & L_{cb} & L_{cc} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$
(9)

The mathematical model for this motor is described in Equation (1) with the assumption that the magnet has high sensitivity and rotor induced currents can be neglected [10]. It is also assumed that the stator resistances of all the windings are equal. Therefore the rotor reluctance does not change with angle. Now

$$L_{aa} = L_{bb} = L_{cc} = L \tag{10}$$

$$L_{ab} = L_{bc} = L_{ca} = M \tag{11}$$

Assuming constant self and mutual inductance, the voltage equation becomes

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L - M & 0 & 0 \\ 0 & L - M & 0 \\ 0 & 0 & L - M \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}$$
(12)

In state space form the equation is arranged as

$$\frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = -\frac{R}{L} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \frac{1}{L} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} + \frac{1}{L} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$
(13)

The electromagnetic torque developed is given as

$$T_e = (e_a i_a + e_b i_b + e_c i_c) / \omega_r$$
⁽¹⁴⁾

The equation of motion is given as

$$\frac{d}{dt}\omega_r = (T_e - T_L - B\omega_r) / J$$
⁽¹⁵⁾

Where ωr is the derivative of the rotor position θ . P is the number of poles, T1 is the load torque in Nm, J is the moment of inertia in kg-m2 and B is the friction co-efficient Nms/Rad. The derivative of rotor position is as

$$p\theta = \omega \tag{16}$$

Equations 6-16 represent the dynamic model of the PMBLDC motor. \dot{l}_a , \dot{l}_b , \dot{l}_c are currents and λ_a , λ_b , λ_c are

International Journal of Advanced Trends in Computer Science and Engineering, Vol.2, No.2, Pages : 203-208 (2013) Special Issue of NCRTECE 2013 - Held during 8-9 February, 2013 in SMK Fomra Institute of Technology, OMR, Thaiyur, Kelambakkam, Chennai

flux linkages. e_a, e_b, e_c are phase to neutral back EMFs of PMBLDC drive in respective phases. R is the resistance of motor windings/phase. Mutual inductances are represented as M and self-inductances are represented as L.

V. EVALUATION OF PERFORMANCE OF PFC SEPIC CONVERTER FED PMBLDC DRIVE

Using Matlab-Simulink environment the proposed PMBLDC drive is modeled and its performance is evaluated for mining applications. The load is considered as having a rated torque of 5.4 Nm. A 0.5kW rating PMBLDC motor is used to drive the load whose speed is controlled effectively by controlling the DC link voltage. Simulink model of the proposed model of the open loop controlled PMBLDC motor with PFC SEPIC converter, and a PI controller is shown in Fig 4.



Figure. 4. Open Loop Controlled PFC SEPIC Converter fed PMBLDC Drive

The input voltage waveform is shown in Fig.5; the inverter output voltage is shown in Fig.6. The AC mains current and the input voltage waveform is shown in Fig 7, and the back EMF waveform is shown in Fig.8.





Figure 7. Input Voltage and Input Current waveform



Figure 8.Back-EMF

The proposed PFC SEPIC converter based PMBLDC drive is fed from a 230 V AC mains and started at a rated torque (5.4Nm) and the reference speed is set at 1800 rpm. Simulink model of the proposed model of the closed loop controlled PMBLDC motor with PFC SEPIC converter, and a PI controller is shown in Fig 9. The performance evaluation of the proposed drive is evaluated on the basis of parameters like total harmonic distortion (THD) and power factor (PF) at the rated speed of 1800 rpm. It can be seen from Fig 14, that the motor attains the reference speed smoothly within 0.2 sec.

For current control at the input of the PFC converter an average current control scheme is employed using a current gain. The current control loop is placed inside a speed control loop, for CCM operation of the converter. The control loop processes the voltage error between the measured converter output voltage V₀ and the reference value of V₀, through a PI controller to generate modulating control signals. This signal is multiplied with a input AC voltage to generate a reference DC current Idc sensed after the diode bridge rectifier. The resultant current error is amplified and compared with a saw-tooth carrier wave of fixed frequency (f_f) to generate the PWM pulse for the PFC converter. The duty ratio of the converter (D) at a switching frequency (f_s) controls the DC link voltage at the desired value. Electronic commutator uses signals from Hall Effect position sensors to generate the switching sequence for the VSI as shown in Table I.

TABLE I.	Output	of the	electronic	commutator	based	on
the Hall Effect	Sensor	Signal	5			

Hal Signals			Switching Signals						
	Ha	H _b	H _c	S _{a1}	S _{a2}	S _{b1}	S _{b2}	S _{c1}	S _{c2}
	EMF_a	EMF_b	EMF_c	Q1	Q2	Q3	Q4	Q5	Q6
	0	0	0	0	0	0	0	0	0
	0	-1	+1	0	0	0	1	1	0
	-1	+1	0	0	1	1	0	0	0
	-1	0	+1	0	1	0	0	1	0
	+1	0	-1	1	0	0	0	0	1
	+1	-1	0	1	0	0	1	0	0
	0	+1	-1	0	0	1	0	0	1
	0	0	0	0	0	0	0	0	0



Figure. 9. Closed Loop Controlled PFC SEPIC Converter fed PMBLDC Drive



Figure 10. Inverter Output Voltage (Closed Loop)



Figure 11. Output Current Waveform



Figure 12. Input Voltage and Input Current waveform



Figure 13. Step Change in load torque applied at t=1 sec



Figure 14. Speed Response of PFC SEPIC Converter fed PMBLDC Drive

While the fig 7 shows the input voltage and input current waveform of the open loop controlled PFC SEPIC converter fed PMBLDC drive, Fig 12, gives the closed loop performance. Comparing both the diagrams it can be concluded, that the closed loop improves the input power factor and brings it to near unity. Figure 13 shows the step change in the torque is given at 1 sec and as seen from Fig 14, the speed attains its steady state instantly after the step change in the load torque.



Figure 15. Total Harmonic Distortion

As seen from Fig 15, the THD mains current of the proposed PFC SEPIC converter fed PMBLDC drive is observed under 5%, which is the requirement of power quality.

VI. CONCLUSION

A PFC SEPIC converter based PMBLDC drive for mining is simulated and implemented. Feedback signals from the PMBLDC motor representing speed and position are utilized to get the driving signals for the inverter switches through a PI controller. It is found that the power factor is near unity with the use of SEPIC converter. The efficiency increases due to the increase in the power factor. The PFC feature of the SEPIC converter has ensured power factor close to unity. SEPIC Converter fed PMBLDC motor is preferred to the other systems due to the improved power factor.

REFERENCES

- T.Kenjo and S.Nagamori, 1985, "Permanent Magnet Brushless DC Motors", Clarendon Press, Oxford.
- [2] T.J. Sokira and W.Jaffe, 1989. "Brushless DC Motors: Electronic Commutation and Control", Tab Books USA, 1989.
- [3] Tay Siang Hui, K.P. Basu , V.Subbiah," Permanent Magnet Brushless Motor Control Techniques", IEEE Proc., National Power Engineering Conference (PECon) 2003 Proceedings, Bangi, Malysia, 2003, pp. 133-138
- [4] Thirusakthimurugan,P, Dananjayan,P, "A New Control Scheme for the Speed Control of PMBLDC Motor Drive", IEEE Proc.- International Conf on Control, Automation Robotics and Vision ICARCV '06., 2006,pp.1-5.
- [5] N.Bianchi, S. Bolognani, Ji-Hoon Jang and Seung-Ki Sul, "Comparison of PM Motor structures and sensorless Control Techniques for zerospeed Rotor position detection", IEEE Transactions on Power Electronics, Vol 22, Issue 6, 2007, pp.2466-2475.
- [6] Limits for Harmonic Current Emissions (Equipment input current ≤ 16A per phase), International Standard IEC 61000-3-2, 2000.
- [7] J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase ac supplies and using either single or split dc rail voltage outputs", IEEE Proc. Applied Power Electronics Conf and Exposition, APEC'95.Vol 1, pp. 473-479.
- [8] K.Matsui, I.Yamamoto, T.Kishi and M,Hasegava," A comparison of various Buck-Boost converters and their application to PFC", IEEE Trans-Industrial Electronics Society, 2002, Vol 1, pp.30-36.
- [9] O.Garcia ,J.A.Cobos ,R. Prieto, P.Alou and J.Uceda ," Single phase power factor correction : a survey",IEEE Transactions on Power Electronics, 2003, Vol 18, Issue 3, pp.749-755.
- [10] A.Barkley, D.Michaud, E.Santi, A. Monti and D. Patterson, "Single stage brushless DC motor drive with high input power factor for single phase applications", IEEE trans on Power Electronics Specialists Conference, PESC, 2006, pp.1-10.
- [11] L. Rossetto, G. Spiazzi and P.Tenti, "Boost PFC with providing output voltage stabilization and compliance with EMC standards", IEEE Trans on Industry Applications, 2000, Vol 36, Issue1, pp.188-193.