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DESIGN OF PULSE TRIGGERED FLIP-FLOP USING DYNAMIC CONTROLLING CIRCUIT

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ABSTRACT

The choice of flip-flop topologies is an essential importance in design of VLSI integrated circuits for high speed and high performance CMOS circuits. In this paper, a novel pulse triggered flip-flop design is presented which has small delay and low power consumption. Two transistor AND gate is eliminated from the design and a transmission gate is used which in turn reduces the circuit complexity. In this paper we present a comparison of implicit type flip-flops in terms of its transistor count , delay and power consumption. The comparison includes the elucidation of circuit operation, simulation and power estimation. The operation of each flip-flop is estimated and it is simulated using microwind and T-SPICE simulator. The analysis of the various parameters are carried out at 0.12µm technology.

Keywords:

Pulse triggered, low power, flip-flop

1. INTRODUCTION:

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative time. P-FFs are thus less sensitive to clock jitter. Despite these advantages, pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network [4].

Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [6]. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional pre-charge, conditional discharge, or conditional data mapping are

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applied [7]–[10]. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches.

In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced. This gives rise to competitive power and power–delay–product performances against other P-FF designs. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced.

2. IMPLICIT TYPE P-FF:

2.1 ip-DCO(implicit pulsed-Data Close to Output)

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. A state-of-the-art P-FF design, named ip-DCO, is given in Fig 1(a) [6]. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on.

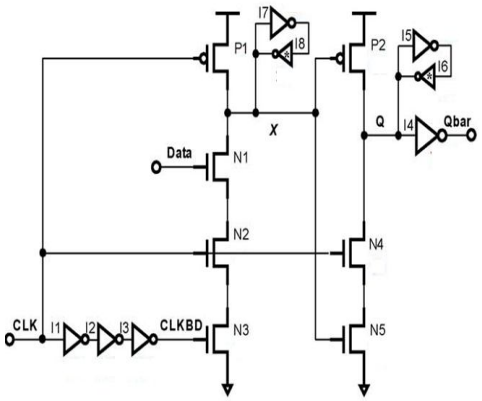

Figure 1(a). ip-DCO

2.2 MHLLF(Modified Hybrid Latch Flip-flop)

An improved P-FF design, named MHLLF Fig.1 (b) MHLLF, by employing a static latch structure presented in [10]. Node is no longer pre charged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero. This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q (D-to-Q) delay during “0” to “1” transitions because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node becomes floating when output Q and input

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Data both equal to "1 ". Extra DC power emerges if node X is drifted from an intact "1".

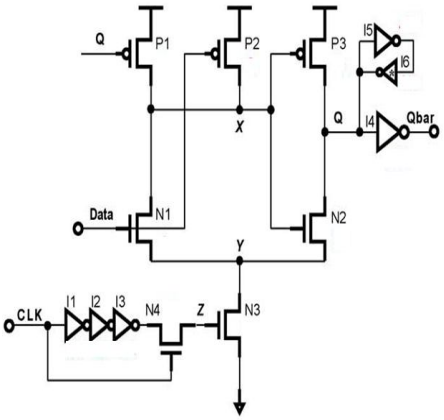

Figure 1 (b). MHLLF

2.3. SCCER(Single Ended Conditional Capture Energy Recovery)

A refined low power P-FF design named SCCER using a conditional discharged technique [9], [8]. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node [8]. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

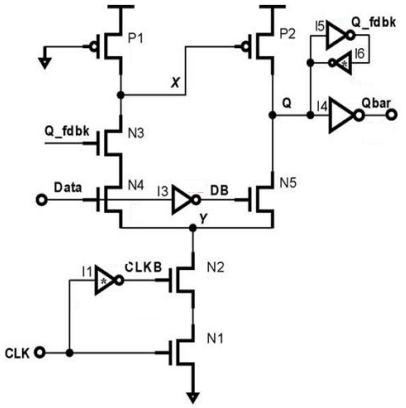

Figure 1(c). SCCER

2.4. P-FF Design with conditional pulse enhancement scheme

The design, as shown in Fig. 1(d), adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 1(d), the upper part latch design is similar to the one employed in SCCER design [12]. As opposed to the transistor stacking design in Fig. 1(a) and (c), transistor N2 is removed from the discharging path.Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic

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(PTL)-based AND gate [13], [14] to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node is kept at zero most of the time. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node , which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node can be reduced due to a diminished voltage swing.

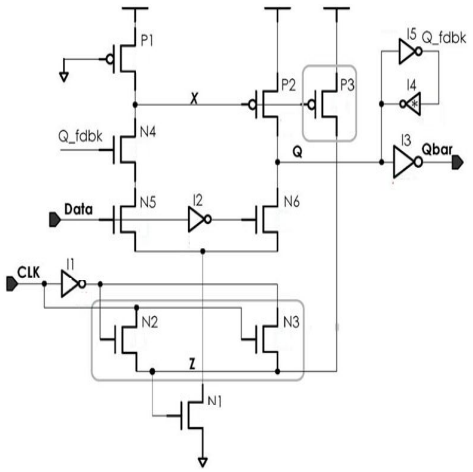

Figure 1(d). *P-FF Design with conditional pulse enhancement scheme*

3. PROPOSED DESIGN

*The de*sign is shown in figure 2. It overcomes the problem of the above described flip-flop. Referring figure 1© , the proposed design is similar to it in case of latching circuit and it differs only in the pulse generation circuit. It replaces two-input pass transistor logic (PTL)-based AND gate by a transmission gate and N1 and P3 is removed from the design. nMOS pass transistor logic passes only strong 0 whereas transmission gate passes strong 0 and strong 1. By doing so we get reduced transistor count and hence area gets reduced which is an important criteria in this modern era with the improved VLSI technology. Use of transmission gate reduces the voltage drop across the pass transistor and hence power dissipation gets reduced. It also doubles the area and interconnects but the overall size of the circuit gets reduced. At rising edge of the clock N1 turns on and at falling edge of the clock N2 gets turns on. If both clock and Data are high transistors N1, N5, N4 and P2 turns on while N2 and N6 turns off. If data is low transistor N6 turns on and transistor N5 turns off. Hence output occurs with low switching activity.

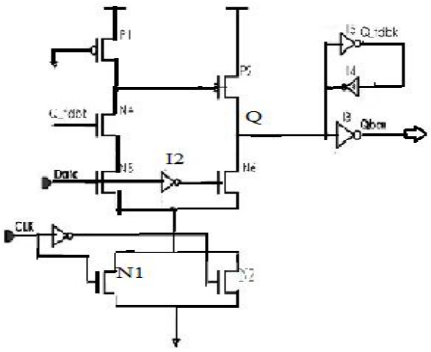

Figure 2 .Proposed design

4.RESULT

A simulation window appears with inputs and output. The power consumption is also shown on the right bottom portion of the window. If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the

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layout again and run the simulations till you achieve your target delays. Depending on the input sequences assigned at the input the output is observed in the simulation. To demonstrate the superiority of the proposed design, post layout simulations on various P-FF designs were conducted to obtain their performance figures. These designs include the three P-FF designs shown in Fig. 1 (ip-DCO [6], MHLLF [9], SCCER [10]), another P-FF design called conditional capture FF (CCFF) [7], and two other non-pulse-triggered FF designs, i.e., a sense-amplifier-based FF (SAFF) [2], and a conventional transmission gate-based FF (TGFF).. The operating condition used in simulations is 500 MHz/1.0 V.

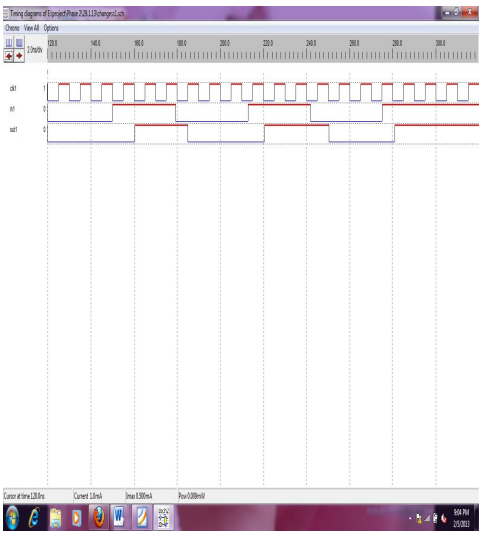

Figure 3. Output Waveform

Table 1.Comparions of ff

FF	Ip DCO	MHLLF	SCCER	PFF	PROPOSED
TRAN-SITOR COUNT	23	19	17	19	17

5.CONCLUSION

In this paper, the various Flip-flop design like, ip-DCO, MHLLF and SCCER are discussed. These were been also designed in Microwind tool and those result waveforms are also discussed. The comparison table also added to verify the designed methods. With these all results proposed design is better than ip-DCO and MHLLF designs.

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