

Power Quality Improvement for Grid Connected Photovoltaic System



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Abstract—This paper proposes a single-phase five-level photovoltaic (PV) inverter topology for grid-connected PV systems with a novel pulse width-modulated (PWM) control scheme. Two reference signals identical to each other with an offset equivalent to the amplitude of the triangular carrier signal were used to generate PWM signals for the switches. A digital proportional–integral current control algorithm is implemented to keep the current injected into the grid sinusoidal and to have high dynamic performance with rapidly changing atmospheric conditions.

The inverter offers much less total harmonic distortion and can operate at near-unity power factor. The proposed system is verified through simulation and the results are compared with the conventional single-phase three-level grid-connected PWM inverter.

Index Terms—Grid connected, photovoltaic (PV), proportional integral (PI) current control, pulse width modulated (PWM) inverter.

I. INTRODUCTION

The ever-increasing energy consumption, fossil fuels' soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun's energy directly into electricity. Photovoltaic-generated energy can be delivered to power system networks through grid-connected inverters. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW [1]. Types of single-phase grid-connected inverters have been investigated [2]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the

inverter's switching operation. In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width-modulated (PWM) inverters. They offer improved output waveforms, smaller filter size, lower EMI, lower total harmonic distortion (THD), and others [3]–[8].

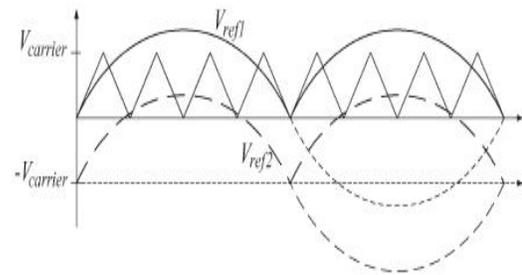


Fig.1. Carrier and reference signals

The three common topologies for multilevel inverters are as follows: 1) diode clamped (neutral clamped) [9]–[11]; 2) capacitor clamped (flying capacitors) [12]–[14]; and 3) cascaded H-bridge inverter [15]–[17]. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters, including the following: multilevel sinusoidal (PWM), multilevel selective harmonic elimination, and space vector modulation [3], [18].

A typical single-phase three-level inverter adopts full-bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage then has the following three values: zero, positive (+V_{dc}), and negative (–V_{dc}) supply dc voltage (assuming that V_{dc} is the supply voltage). The harmonic components of the output voltage are determined by the carrier frequency and switching functions. Therefore, their harmonic reduction is limited to a certain degree [4].

To overcome this limitation, this paper presents a five-level PWM inverter whose output voltage can be represented in the following five levels: zero, $+1/2V_{dc}$, V_{dc} , $-1/2V_{dc}$ and $-V_{dc}$. As the number of output levels increases, the harmonic content can be reduced. This inverter topology uses two reference signals, instead of one reference signal, to generate PWM signals for the switches. Both the reference signals V_{ref1} and V_{ref2} are identical to each other, except for an offset value equivalent to the amplitude of the carrier signal $V_{carrier}$, as shown in Fig. 1.

Because the inverter is used in a PV system, a proportional– integral (PI) current control scheme is employed to keep the output current sinusoidal and to have high dynamic performance under rapidly changing atmospheric conditions and to maintain the power factor at near unity. Simulation and experimental results are presented to validate the proposed inverter configuration.

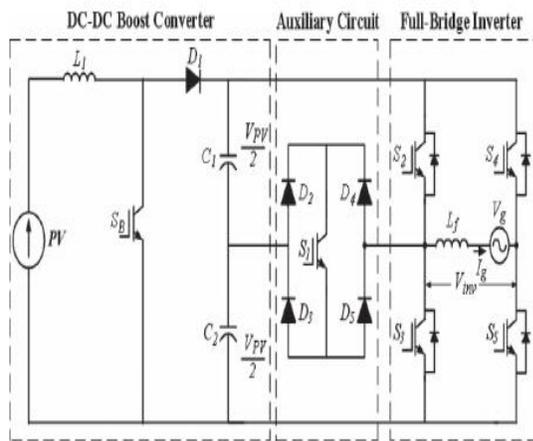


Fig.2.Single phase five-level inverter topology

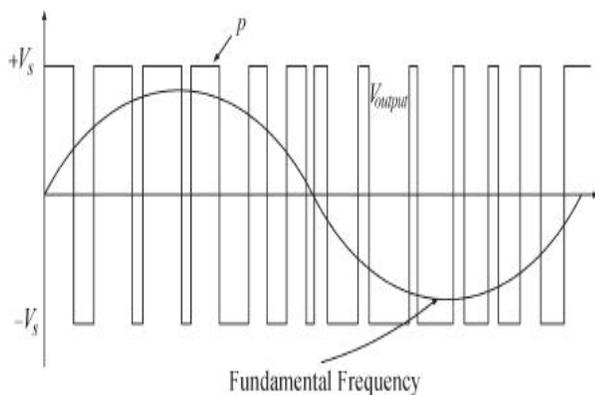


Fig.3.Sinusoidal PWM signal

II. FIVE-LEVEL INVERTER TOPOLOGY AND PWM LAW

The proposed single-phase five-level inverter topology is shown in Fig. 2. The inverter adopts a full-bridge configuration with an auxiliary circuit [4]. PV arrays are connected to the inverter via a dc–dc boost converter. Because the proposed inverter is used in a grid-connected PV system, utility grid is used instead of load. The dc–dc boost converter is used to step up inverter output voltage V_{inv} to be more than $\sqrt{2}$ of grid voltage V_g to ensure power flow from the PV arrays into the grid [19]. A filtering inductance L_f is used to filter the current injected into the grid. The injected current must be sinusoidal with low harmonic distortion. In order to generate sinusoidal current, sinusoidal PWM is used because it is one of the most effective methods. Sinusoidal PWM is obtained by comparing a high-frequency carrier with a low-frequency sinusoid, which is the modulating or reference signal. The carrier has a constant period; therefore, the switches have constant switching frequency. The switching instant is determined from the crossing of the carrier and the modulating signal.

Sinusoidal PWM Law

A fundamental period in Fig. 3 consists of p pulses whose widths vary sinusoidal throughout the cycle to give the fundamental component of frequency. The basis of equivalence between the desired sinusoid and the actual pulsed waveform is taken to be volt–seconds, as shown in Fig. 4, i.e., $A_{s1} = Ap1$ and $A_{s2} = Ap2$. One of these pulses, the general k th pulse, is characterized in detail in Fig. 5.

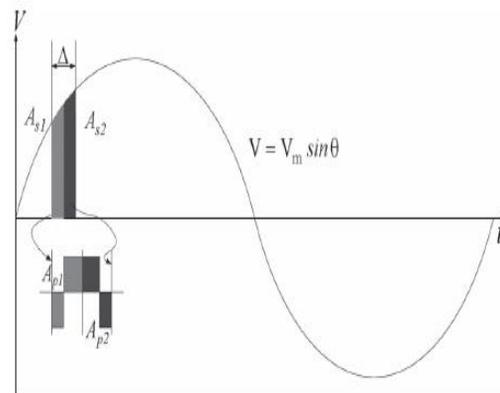


Fig.4.Basis of equivalence for sinusoidal PWM

III. OPERATIONAL PRINCIPLE OF THE PROPOSED INVERTER

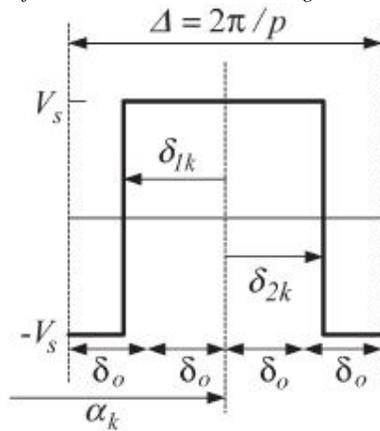


Fig.5.Characterization of pulse

M is the “modulation index” and

$$M = V_m / V_s \tag{1}$$

Equation (1) can be expressed in terms of amplitude of carrier signal V_c by replacing V_s with V_c . Because, in this topology, two identical reference signals are used, $V_s = 2V_c$ and $V_m = V_{ref1} = V_{ref2}$.

If $M > 1$, higher harmonics in the phase waveform are obtained. Therefore, M is maintained between zero and one. If the amplitude of the reference signal is increased to be higher than the amplitude of the carrier signal, i.e., $M > 1$, this will lead to over modulation. Large values of M in sinusoidal PWM techniques lead to full over modulation [20].

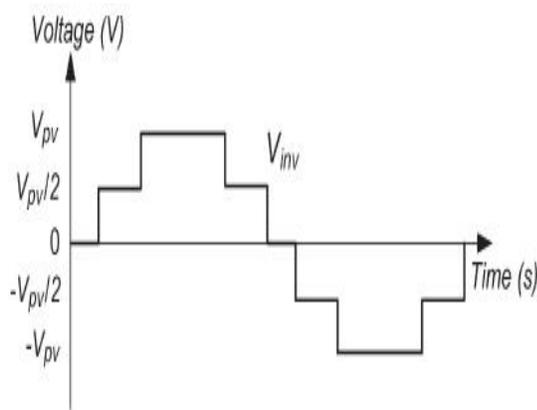


Fig.6.Ideal five-level inverter output voltage

Because PV arrays are used as input voltage sources, the voltage produced by the arrays is known as V_{pv} . V_{pv} is boosted by a dc-dc boost converter to exceed $\sqrt{2}V_g$. The voltage across the dc-bus capacitors is known as V_{pv} . The operational principle of the proposed inverter is to generate five level output voltage, i.e., $0, +V_{pv}/2, +V_{pv}, -V_{pv}/2,$ and $-V_{pv}$ as in Fig. 6. As shown in Fig. 2, an auxiliary circuit which consists of four diodes and a switch S_1 is used between the dc-bus capacitors and the full-bridge inverter. Proper switching control of the auxiliary circuit can generate half level of PV supply voltage, i.e., $+V_{pv}/2$ and $-V_{pv}/2$ [4].

Two reference signals V_{ref1} and V_{ref2} will take turns to be compared with the carrier signal at a time. If V_{ref1} exceeds the peak amplitude of the carrier signal $V_{carrier}$, V_{ref2} will be compared with the carrier signal until it reaches zero. At this point onward, V_{ref1} takes over the comparison process until it exceeds $V_{carrier}$. This will lead to a switching pattern, as shown in Fig. 8. Switches S_1 – S_3 will be switching at the rate of the carrier signal frequency, whereas S_4 and S_5 will operate at a frequency equivalent to the fundamental frequency.

IV. CONTROL SYSTEM ALGORITHM AND IMPLEMENTATION

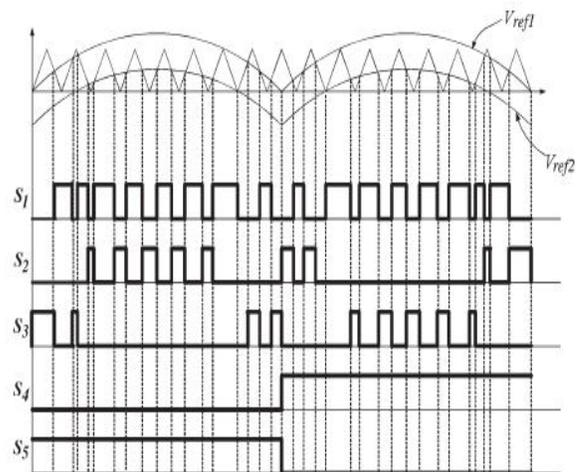


Fig.7.Switching pattern for the single phase five-level inverter

The feedback controller used in this application utilizes the PI algorithm. As shown in Fig. 8, the current

V. SIMULATION RESULTS

Simulation Results

In order to verify that the proposed inverter, simulations were performed by using MATLAB SIMULINK.

One of the problems in the PV generation systems is the amount of the electric power generated by solar arrays always changing with weather conditions, i.e., the intensity of the solar radiation. A maximum power point tracking (MPPT) method or algorithm, which has quick-response characteristics and is able to make good use of the electric power generated in any weather, is needed to solve the aforementioned problem [21]. Various MPPT control methods have been discussed in detail in [22]. Constant m is derived from the MPPT algorithm.

The perturb-and-observe algorithm is used to extract maximum power from PV arrays and deliver it to the inverter [23], [24]. The instantaneous current error is fed to a PI controller. The integral term in the PI controller improves the tracking by reducing the instantaneous error between the reference and the actual current. The resulting error signal u which forms V_{ref1} and V_{ref2} is compared with a triangular carrier signal, and intersections are sought to produce PWM signals for the inverter switches.

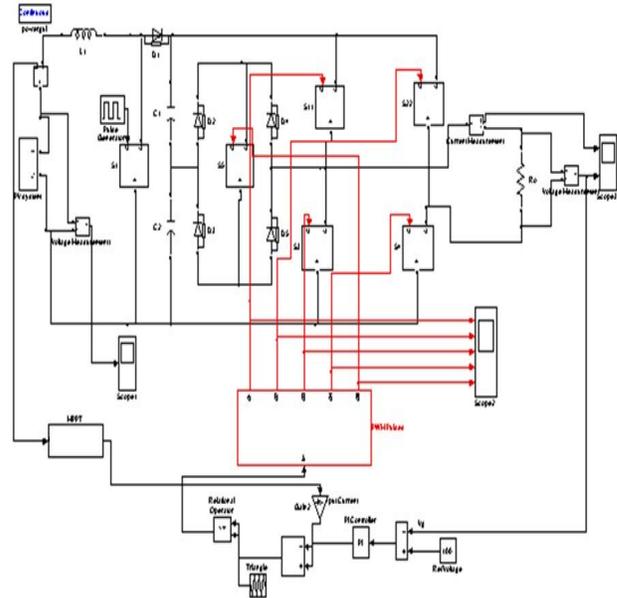


Fig.9. Matlab circuit diagram of five level inverter with controller

Fig.9.shows the Matlab circuit diagram of five level inverter with controller circuit. Fig.10.shows the PWM switching strategy used in this paper. It consists of two reference signals and a triangular carrier signal. Both the reference signals are compared with the triangular carrier signal to produce PWM switching signals for switches S1–S5 as in Fig. 7.

Note that one leg of the inverter is operating at a high switching rate equivalent to the frequency of the carrier signal, whereas the other leg is operating at the rate of fundamental frequency (i.e., 50 Hz). The switch at the auxiliary circuit S1 also operates at the rate of the carrier signal. As mentioned earlier, the modulation index M will determine the shape of the inverter output voltage V_{inv} and the grid current I_g . Fig. 11 shows V_{inv} and I_g .

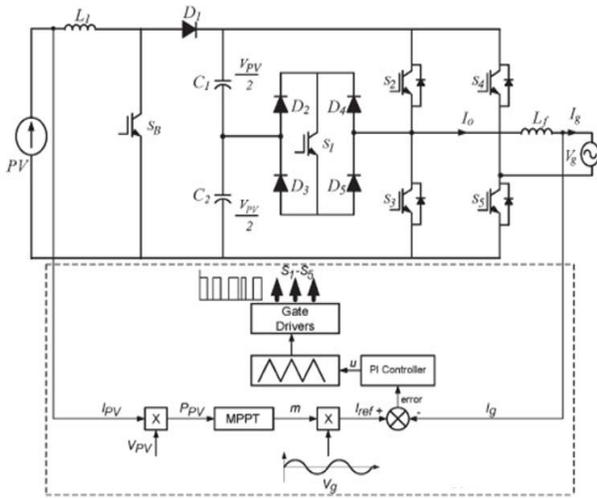


Fig.8.Five level inverter with controller

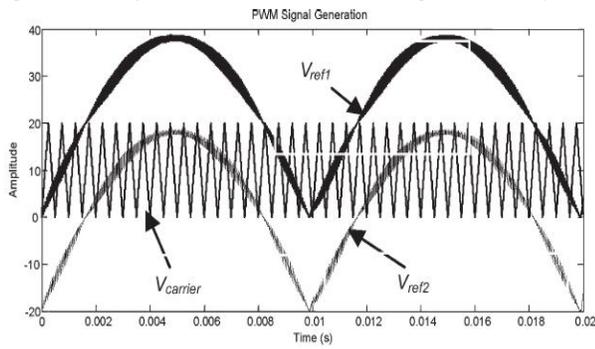


Fig.10.PWM switching strategy

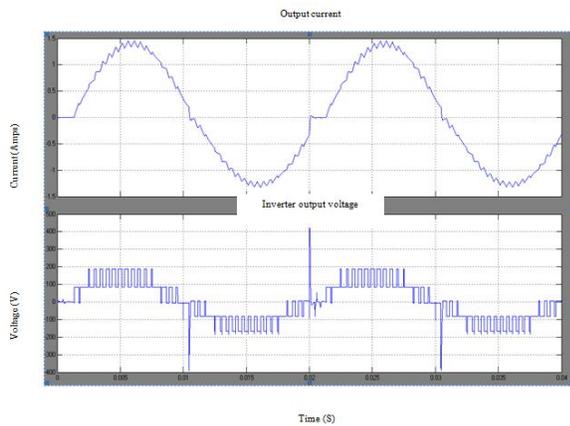


Fig.11.Inverter output voltage and grid current

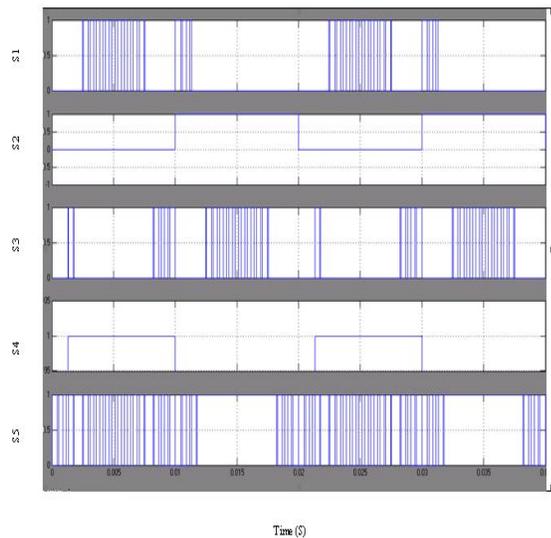


Fig.12.Output of PWM pulses for the switching circuit

The above fig.12.shows the output of PWM pulses for the switching circuit. And the THD result of the three-level PV inverter is shown in fig.13.

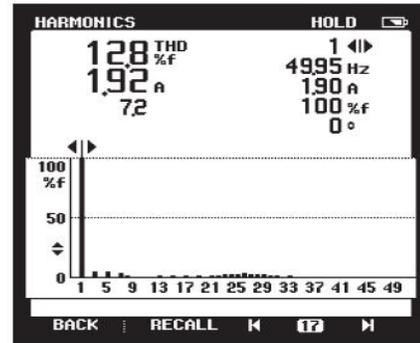


Fig.13.TH D result of the three-level PV inverter

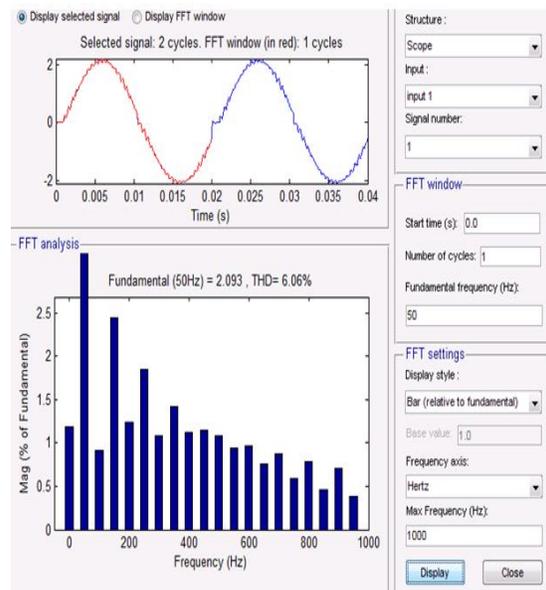


Fig.14.FFT analysis for THD result of the five-level inverter

The Fast Fourier Transform analysis for the THD result of the five-level inverter is given in fig.14. These results indicate that the THD of the five-level inverter is much lesser than that of the conventional three-level inverter.

VI. CONCLUSION

This paper presented a single-phase five level PWM inverter for PV application. It utilizes two reference signals and a carrier signal to generate PWM switching signals. The circuit topology, modulation law, and operational principle of the proposed inverter were analyzed

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 in detail. A digital PI current control algorithm is implemented to optimize the performance of the inverter. The results indicate that the THD of the five-level inverter is much lesser than that of the conventional three-level inverter. Furthermore, both the grid voltage and the grid current are in phase at near-unity power factor.

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