ISSN 2278-3091
Volume 9, No.1, January – February 2020
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse79912020.pdf
https://doi.org/10.30534/ijatcse/2020/79912020

Design of BCD Adder using Quantum Cellular Automata

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ABSTRACT

QCA is a technology which is transistor less and it is one of its kind and emerging technology. Working of QCA purely works on the principle of coulombic repulsions. Due to these coulombic repulsions of electrons in quantum dots, high speed digital circuits can be designed. When compared to existing CMOS technology, computational speed of Quantum Cellular Automata is significantly high. This paper mainly depicts the functioning and simulation results of BCD Adder which was designed using Quantum Cellular Automata. Digital Circuits with high complexity can be designed by using Quantum Cellular Automata by using crossovers. When crossovers and multi-layer connections are used area occupied by the circuit and delay time will be reduced.

Key words : BCD Adders, CMOS, Crossovers, Coulombic Repulsions.

1.INTRODUCTION

A quantum dot is made up of a semiconducting material called Cadmium Selenide(CdSe). Functioning of a quantum cell depends upon Coulombic force of repulsions where Coulombic force is the force which is exerted by an object bearing electric charge on the other object bearing an electric charge. In this case the coulombic force is repulsive because both charges are negative. A quantum dot is also called as a potential well where electrons are present. In a quantum cell there are four quantum dots in which electrons will occupy any two diametrically opposite quantum dots because coulombic force of repulsion is less in between two diametrically opposite quantum dots when compared to two adjacent quantum dots. The electrons are not capable of coming out of the quantum cell but they can tunnel between the potential wells [1]. The electrons can tunnel between the quantum wells through tunnel junctions as shown in Fig. 1.

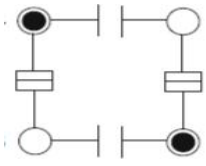

Figure 1: Ordinary QCA cell with Tunnel junctions and capacitance.

In QCA if there is change in position of electrons within a cell, the information will be transferred from on end to the other end in a QCA wire as shown in Fig. 2 .

1.1.Polarity

As shown below, Fig. 3a represents negative polarity and Fig. 3b represents positive polarity [2].
The alignment of the dots in the quantum wells will raise the topic of polarity. There are two types of polarity- positive (+1) and negative (-1). The positive polarity cell is used to get the logic level 1. Similarly, the zero logic is obtained by using the negative polarity cell.[3-8]

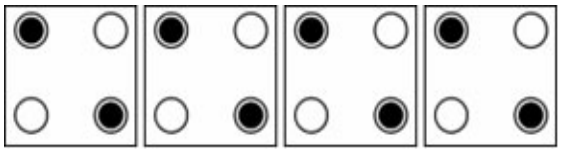

Figure 2: QCA wire

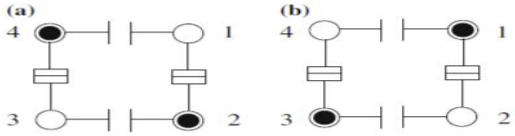

Figure 3: (a) Negative Polarity and (b) Positive Polarity

The quantum dot has 4 potential well p1, p2, p3and p4 in which any two diagonal wells will be consisting of electrons. The position of the presence of electron is indicated with a logic 1 and the absence of electron is represented with a logic in the mathematical representation[4] shown below.

$$\text{Polarity}=\frac{(p1+p3)-(p2+p4)}{p1+p2+p3+p4}$$

2.MOTIVATION

Current era of technology is demanding the miniaturized versions of the systems and simultaneously the computational speed of the system must be high, and the delay must be low. Quantum Cellular Automata is one of the emerging technologies which satisfies all these requirements. A circuit which is designed by using Quantum Cellular Automata

occupies less area, thereby power dissipation will be decreased.

3.HOW QCA IS FASTER WHEN COMPARED TO MOSFET?

Consider an n channeled MOSFET. A MOSFET is a Quad terminal device which has gate, drain, source and substrate. In NMOS electrons are present in n+ region which was heavily doped in source and drain. And holes are present under the oxide layer. When a positive voltage is supplied, the positive charge carriers below the oxide layer experience opposing force and are forced to move downwards. And when the voltage of gate is greater than the threshold voltage (Vgs>Vth) an appreciable channel is formed between the drain and source. As the applied voltage is positive, the electrons present in n+ regions experience attractive force and are attracted into the channel which was formed earlier. The voltage of gate controls the electrons present in the channel.

As there are a greater number of electrons travelling between source and drain in a transistor , the area occupied will be more, and as each quantum cell contains only two electrons, the area occupied will be less. And as the voltage of the drain (Vds) starts to show growth in the transistor, due to modulation effect of channel, the channel length decreases. The speed of electrons is directly proportional to the channel's length. As the channel length decreases, the speed also decreases. The speed of electrons in Quantum wires depends upon the coulombic repulsions in Quantum wires. The computational speed of QCA is far better when compared to the conventional MOSFET [29-31].

3.1.Majority GATE

Most of the circuits in Quantum Cellular Automata are built using majority gates[9]. A majority gate is a presence of five quantum cells represented in fig. 4,a logic cell placed in the center, three input cells labelled A, B and C and an output cell. The logic function of the majority gate is

Majority (A, B, C) = C.A+ A.B+B.C

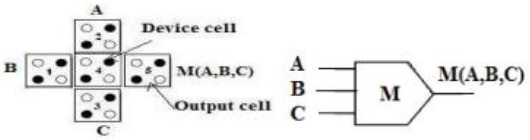

Figure 4: Majority gate QCA representation and the Block representation

In simple words, the output of the majority gate will be the input which is same for at least two or at most three input cells.

4.METHODOLOGY

A BCD adder is circuit which is used to produce a 4-bit BCD result by adding two BCD numbers (4-bit) in parallel. Block Schematic of the conventional BCD adder is presented in Fig. 5. The correction logic included in the circuit is used to generate exact BCD output (BCD numbers are from 1 to 9)[6]. A conventional 4-bit parallel adder is used to add two

BCD numbers (4-bit) X and Y with carry as also an input. The sum and a carry is taken out as shown in Fig. 5. Through the successive stage parallel adder circuit as shown in fig. 5, 0110 is added to the medieval sum output if result is greater than 9[10-13].

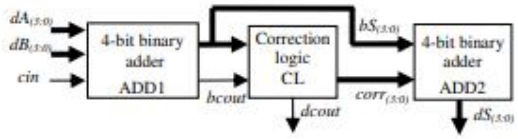

Figure 5: Basic block diagram of the BCD adder

For a binary adder of inputs are given at dA(3:0) & dB(3:0) as well as its carry "cin" and binary output is obtained at bS(3:0) and "bcout" as shown in fig. 5. Block diagram of BCD adder which will be built in QCA Designer can be designed in two ways. One way is to build BCD adder through the proposed methodology as shown in fig. 6 and the correction logic for the proposed methodology is shown in Fig.7. Another way to build BCD adder is through AND gates as shown in Fig. 10. (In QCA Designer an AND gate is obtained by fixing one of its input as logic '0' i.e, polarization will be -1 and other two inputs are variable)[14].

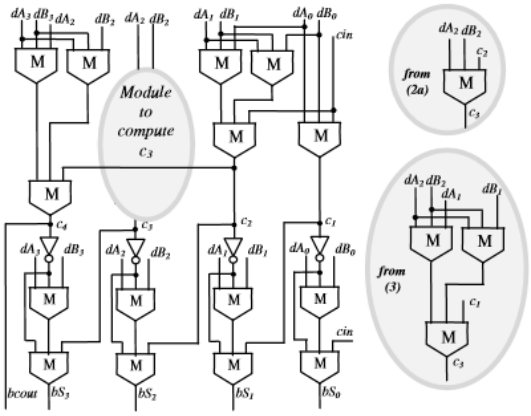

Figure 6: Majority gate implementation of the ADD1

The disadvantage in the above circuit is ,it is only 4-bit BCD adder. It can't perform n-bit BCD adder operation[15].

5.WORKING AND SIMULATION

A Majority Gate are converted as an AND logic gate by making one of the three inputs as logic'0'(fixed) as shown in fig. 8 and remaining two inputs must be variable[16]. And if the fixed input is logic'1',the majority gate pretends as an OR logic gate[16] as represented in fig. 9. And if a cell is rotated 45 degrees , it acts as an INVERTER[16].

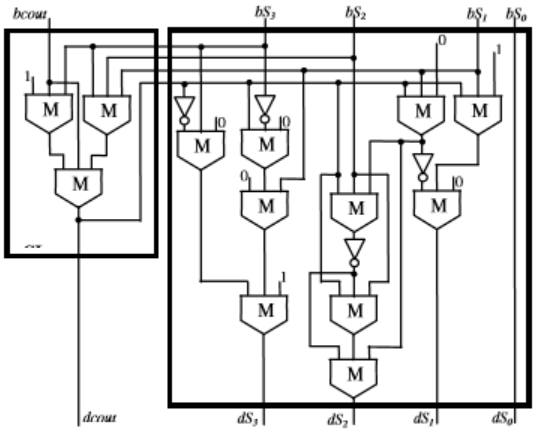

Figure 7: ADD2 Module along with the correction logic.

While designing layout, clock zones[17,18] are provided if there is any crossover so that there will be delay in processing of the data in that respective wire. If there is a crossover between three wires, the first QCA wire is provided with Clock 0 (green)as shown in Fig. 11. so that the data will be passed normally, and the second wire must be provided with clock 1(pink) as shown in Fig. 11 so that there will be some amount of delay. And due to this delay the data in the second wire will be processed after the data in the first wire is processed. Similarly, the third QCA wire is provided with Clock 2(Blue).

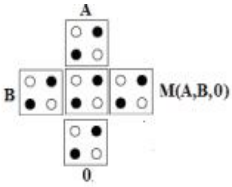

Figure 8: Schematic of AND Gate

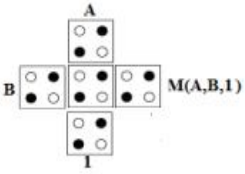

Figure 9: Schematic of AND Gate

The BCD Adder circuit can be built in Logisim as shown in fig .10 by using AND,OR and inverters. Similarly, in QCA designer[9]

The inputs given in the Fig. 12 are DA2, DA3, DB2, DB3, DA0, DB0, DB1, DA1 and Cin respectively. The outputs obtained are DS0, Dout, DS3, DS1, DS2 respectively as shown in the Fig. 13. The outputs obtained as shown in the Fig. 13 are not accurate but approximate where DA0-DA3 is one 4-bit binary input and DB0-DB3 is another 4-bit binary input. DS0-DS1 is the output which is obtained after binary addition as shown in Fig. 13.

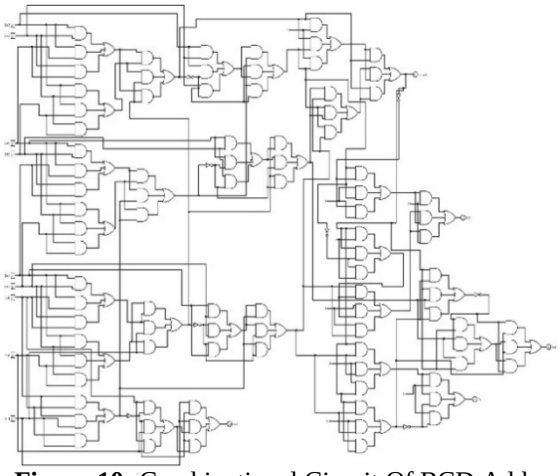

Figure 10: Combinational Circuit Of BCD Adder

Figure 11: Implementation in QCA Designer.

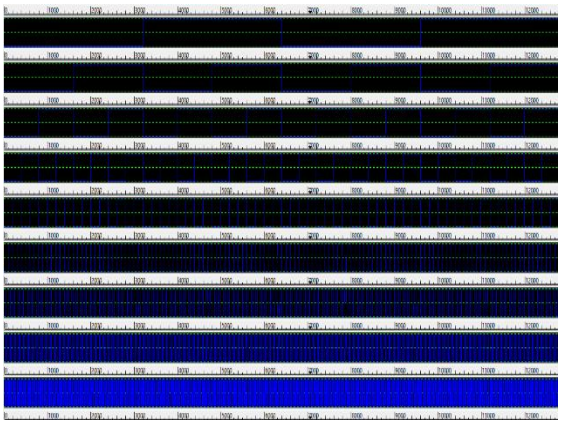

Figure 12: Inputs given to the designed circuit

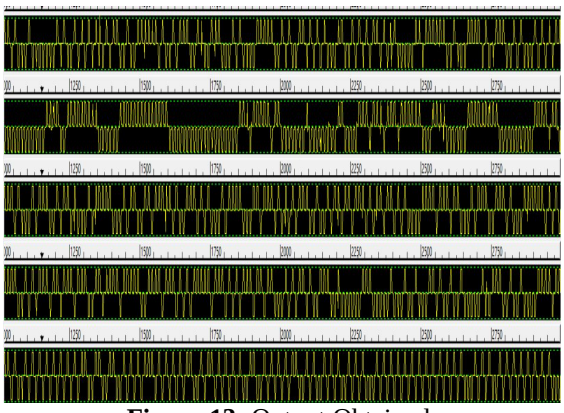

Figure 13: Output Obtained

6.FUTURE SCOPE

Performance parameters like number of cells, area and clock cycles provide further future improvements in the efficiency of the digital circuits designed using QCA. Proficient routing and interconnects are the strategies in which QCA will have a broad spotlight.

7.CONCLUSIONS

QCA circuit works effectively irrespective of the provided clock zones[3].QCA based digital circuits can be implemented by using crossovers so that the cells used for the design is minimal. Thus, the proposed circuit will exhibit computational delay and area occupancy up to 30% and 40% respectively lower than other circuitry.

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