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DESIGN OF FIR FILTER ALGORITHM FOR NOISE REMOVAL IN ECG SIGNAL USING OPEN CORE SoC

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ABSTRACT

The emerging technology in computer architecture has led to the development of various ISAs depending on the needs of the desired technology, architectures, and processor cores. Instruction Set Architectures (ISAs) for processors from Intel, AMD, Intel, RISC-V, etc. This has provided the path to implement various functions on an open core SoC Platform. Among the many DSP applications, the FIR filter has been implemented on an open core SoC platform that uses RISCV. Here specifically filtering of noise from ECG signal. The performance cycle count has been obtained for the same and compared with its counterpart ARM M7 on the Keil platform.

Key words: Digital filters, FIR, RISC-V, Keil-5, Open Core, Electrocardiogram.

I. INTRODUCTION

Digital filters are among the vital tools that signal processors have to modify and improve signals. The early days saw analog signal processing as the norm, almost all filtering was attained by using RLC circuits. In the recent times, a great deal of filtering is achieved digitally with simple procedures that can work on special digital signal processing hardware or general-purpose processors. Noise reduction is one of the many reasons for using digital filters. Let's assume the obtained signal exhibits unwanted frequency components, e.g. it contains noise in a frequency range where it is little or no desired signal, then filter are recommended to reduce the relative amplitude of the signal at those frequencies. Such filters are known as frequency blocking filters because they block signal components at certain frequencies. For instance, the lowpass filters block high-frequency signal components, highpass filters block low-frequency signal components, and bandpass filters block all frequencies except those in the mentioned range of frequencies.

In this paper, let's consider removal of elements of noise from ECG signal. An electrocardiogram (ECG) is an instrument whose function is to monitor the electrical signal of the heart. This electrical signal of the heart is represented by in the form of line tracings, which shows spikes and dips known as waves. The functionality of ECG is to measure the current functioning of heart.

FIG 1: BLOCK DIAGRAM OF DIGITAL FILTERING PROCESS

A set of SoC DSP platforms contains a diverse line of application tailored, programmable DSP cores and highly revamped application-oriented co-processors. These platforms also promotes a global software development environment to port the specific code to the platform along with an integrated hardware/software co-verification and emulation environment. They also come with a complete DSP subsystem, BIST, DMA, JTAG, debug, and powerful bus interfaces to RISC controllers, peripherals, memory, and I/O.

Here, we are concentrating on RISC-V core. RISC-V is an open core standard instruction set architecture (ISA) derived from the established reduced instruction set computer principles. In contrast to other accessible ISA designs, the RISC-V ISA is supported under the open source licenses, where it is nonessential to use a license. Several companies are offering RISC-V hardware, open-source operating systems with RISC-V assistance are obtainable and the instruction set is supported in many renowned software tool chains.

II. LITERATURE SURVEY

Apurva Singh Chauhan, Vipul Soni[1] The paper outlines the evolution of FIR filters on Field programmable gate array (FPGAs) by employing IP cores. They have been mapped out and realized by FPGA to filter the digital signal. The execution of this filter on theXilinx XC3S400FPGA is considered and the coefficients are evaluated via the Hamming windowing technique. The model is competent to perform the filtering operations such as low pass, high pass, bandpass, and bandstop based on the choice that is embedded into the design.

Bishwajeet Pandey, Bhagwan Das, Amanpreet Kaur, Tanesh Kumar, Abdul Moid Khan, D M Akbar Hussain, Geetam S Tomar[2].Three different FPGA and SOC are being considered and here the design is implemented on these four ICs and it is found that most energy efficient architecture and also find the architecture that will deliver highest performance among these four architectures taken under consideration.

Swain, Ayas & Mahapatra, [3]The SoC Platform has been implemented by adopting the Open Cores design methodology. The first result show that a portion of the architecture could be charted into an FPGA. The simulation result demonstrates the precise functioning of WISHBONE bus signal and CPU internal signals for a multiplication instruction.

T. Erdogan and T. Arslan[4] An introduction of a framework for the implementation of high throughput FIR filters for low power applications. The design methodology followed in this framework leads to highly flexible FIR filter cores, which are can be modified by coefficient and data manipulation techniques paving a path in significant power savings. Due to power savings within the multiplier units and on system buses, these result in ideal FIR filters for use of IPs on SoC based platforms.

III. METHODOLOGY

A digital filter utilizes a digital processor to accomplish numerical calculations on sampled values of a signal. The processor could either be a general-purpose computer such as a PC, or an exclusive DSP chip. Digital filters are majorly used in the separation of signals that have been merged and for the rehabilitation of signals that have been warped. Digital Filters are preferred to analog filters as they can achieve better results. The difference equation of the nth order digital filter (FIR) can be written as:

$$y(n) = \sum_{(k=0)}^{(N-1)} h(n)\,x(n-k) = \sum_{(k=0)}^{(N-1)} b_k\,x(n-k)$$

The transfer function H(z) is given as:

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{i=0}^{N} a_i z^{-i}$$

The FIR filter is a filter where there is no presence of feedback in its equation. Therefore making the filter inherently stable. A boon of FIR filters is that they can produce linear phases as well. Hence advisable to use in applications that require property of linear phase. The main downside of using a digital FIR filter is that it take more execution time. This is due to the absence of a feedback, that leads to calculation of more coefficient values in the system equation to meet the requirements. If there exists and extra coefficient, this leads to extra multiply and memory for DSP. In the case of a challenging system, the speed and memory requirements to carry out the FIR system can make the system impracticable.

The ECG signal gets corrupted due to the presence of noises, that will give on to wrong diagnosis. Therefore, in order to reduce and remove these noise signals from the required signal, digital filters find it's place in biomedical signal processing. Analog filters are not preferred as they introduce nonlinear phase shift, which is not desirable.[5]

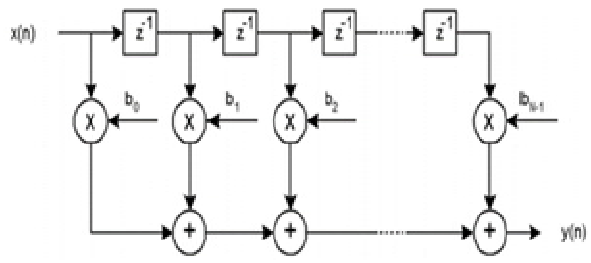

FIG 2: DIRECT FORM REALIZATION OF FIR FILTER

The first step is to build the open core platform, starting with the installation of GNU toolchain. Setting up the GNU Toolchain for building the real-time kernel and its application are one of the main steps in reconfigurable virtual platform. The toolchain utilized in embedded systems is called a cross-platform Toolchain. The method to of compile on a host to generate the respective code for the target system is known as cross compilation and the compiler used for this purpose is called a cross-compiler .The compiler requires a set of support libraries and binaries which are together called cross-platform toolchain. The GNU Toolchain comprises of components like binutils, GNU Cross Compiler Collection (GCC), GDB, new lib.

The steps for building Toolchain as follows:

1. The first step is to choose a target of choice.
2. The different version of binutils, GCC, GDB, Newlib should be chosen from various available versions.
3. Download and install the necessary patches.
4. Compile and build binutils and minimal GCC.
5. Finally compile and build Newlib.

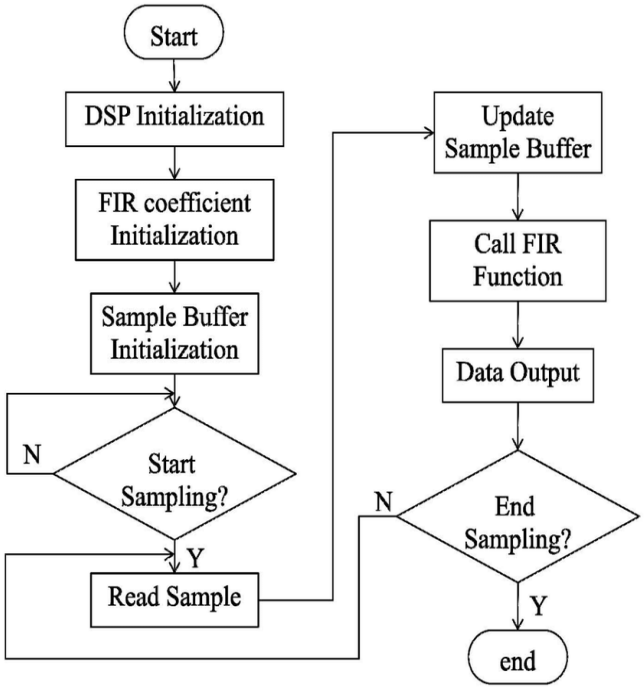

FIG.3: FLOW CHART OF FIR FILTER

After building the open core platform, the next step is to select the cores available. On simulating and attaining the performance analysis of the filtering process. The same is then simulated using

the counterpart ARM controller and performance has been compared.

IV. RESULTS

The implementation of FIR filter for noise filtering of ECG signal is done on both the Open core platform and Keil. This is done to compare the performance cycles for the same code.

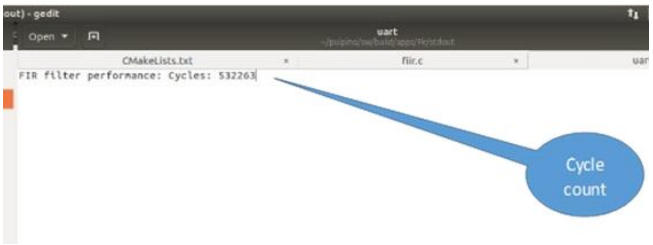

FIG.4: PERFORMANCE CYCLE OBTAINED ON UART WINDOW OF OPEN CORE PLATFORM

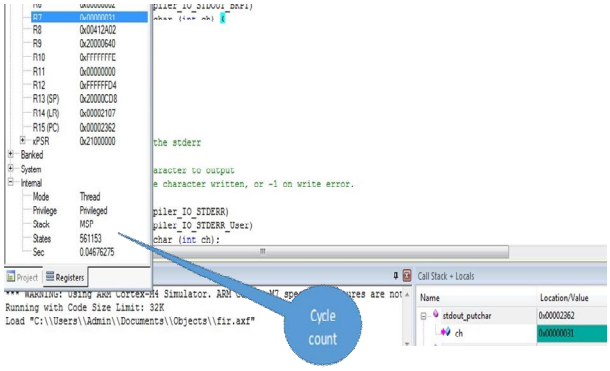

FIG.5: PERFORMANCE CYCLE OBTAINED ON KEIL PLATFORM

TABE 1:PERFORMANCE ANALYSIS OF DIFFERENT CORES

Sl. no	Performance Analysis		
	CORE	***RISCV***	***ARM***
1.	**Cycle count**	**532262**	**561153**

V. CONCLUSION

The development of various ISA's has led to the emergence of open core SoC platforms. Using an open source ISA come to be of great under customization. In this paper, the performance cycle has been evaluated for FIR filter. The simulation statistics are evaluated for both RISCV ISA and ARM proprietary ISA in terms of simulated, instructions, and time. When compared with its counterpart ARM, we can conclude that implementation on RISCV core is more performance efficient. This is due to the use of multiple statements, followed by print statements.

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