ISSN 2278-3091
Volume 8, No.4, July – August 2019
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse72842019.pdf
https://doi.org/10.30534/ijatcse/2019/72842019

A Case Study in the Design Stage for Hardware System Performance Enhancement of Active Electronic Engine Mount Control Module

JeongHyun Cho[1], Ryu HyunKi [2]
[1] Dept. of Computer Engineering, Yeungnam University College, Korea, petercho@ync.ac.kr
[2] GyeongBuk Research Institute of Vehicle Embedded Technology, Korea, hkryu@givet.re.kr

ABSTRACT

Automotive companies are applying mechanical / electronic technologies to various automotive parts for decreasing vehicle vibration. One of the ways to reduce engine vibration is to apply an active engine control mount(ACM). In this paper, to decrease design errors by predicting and correcting signal malfunction and electromagnetic compatibility(EMC) [1][2] in the design process of ACM electronic control module. To do this process, we analyzed the power integrity(PI) analysis which is one of Computer Aided Engineering(CAE) methods. In addition, we introduce ways to secure SI and PI using various methods. So, by applying the analysis results to the design stage, we improved the electromagnetic wave performance. Also, we can reduce the PCB design cost, and improved the reliability of the electromagnetic wave.

Key words : Computer Aided Engineering(CAE), active engine control mount(ACM), electromagnetic compatibility (EMC), SI/PI, PCB.

1. INTRODUCTION

Until now, the automotive has developed acceleration, braking and user convenience devices based on mechanical technology. However, as the emotional requirements of users are increasingly becoming specific, electronic elements have been gradually being applied to overcome mechanical limitations. Mechanical noise and vibration of automobile engines have been significant due to the increase of output, and even small vibration sources have been causing noise and vibration due to lightweight vehicles. The recent criteria for selecting cars have been focused more on interior noise, comfort, and ride quality. [3] Accordingly, in the automobile industry, active studies on engine mounts have been conducted to prevent noise and vibration generated by the engine. The engine mount has a function of reducing unnecessary body vibration and noise between the vehicle body and the engine while simultaneously isolating the vibration of the engine.

Recent studies have been conducted on active electronic engine mounts (ACM) to efficiently isolate various vibration sources of the powertrain. [4] - [7] A typical active engine mount includes a driver that generates a control force inside an existing hydro-mount, with the structure to reduce the dynamic characteristics of the mount by the movement of the movable plate connected to the actuator. An active engine mount is classified into electronic type, pneumatic type, and electric type, according to the type of the actuator used. To ensure the performance of the active mount, the actuator must be capable of generating sufficient force and displacement of the movable plate, and the main rubber characteristics, the liquid chamber size, and the characteristics of the movable plate must all be optimized. Figure 1 shows the result of ACM module to be developed. This ACM system consists of engine mount and control electronic module.

Figure 1: Electronic ACM System Module

This paper applied a Power Integrity (PI) analysis to ACM system, which is a Computer Aided Engineering (CAE) method that can predict, correct, and minimize signal malfunctions and Electro Magnetic Compatibility (EMC) in the process of designing ACM. This CAE method is an essential step for reliability, such as the use of specialized software verification tools for software validation [8]. This study used ANSYS SIwave for simulation to predict and improve the electromagnetic wave performance, thereby reducing the design cost of the PCB as well as improving the reliability of the electromagnetic wave.

2. MODIFICATIONS OF THE CIRCUIT DESIGNS

2.1 A. Power Integrity Methods

The purpose of Power Integrity analysis [9][10] is to quantitatively analyze the appropriate decoupling design to identify design improvements. This study analyzed the AC noise for each voltage rail as follows with the following three steps. First, the impedance for the frequency of the decoupling capacitors is verified to find decoupling capacitors that do not operate properly on the layout. Second, the impedance of the power rail is verified to be adjusted below the target impedance between the voltage regulator module (VRM) and the main IC. Third, a resonance analysis between the power layer and the ground layer confirms whether there is a problem by comparing the clock frequency and the harmonic component frequency of the device. Each target impedance calculation equation is shown in Equation (1).

$$Z_{Target} = \frac{((\mathrm{Power\,Supply\,Voltage}) \times (\mathrm{Allowed\,Ripple}))}{\mathrm{Current}} \quad (1)$$

2.2 Analysis and Improvement of Boost Controller Circuit

The basic switching loop in the boost regulator consists of an output capacitor, an N-channel MOSFET, and a power switch. Minimizing the area of this loop is supposed to reduce drift inductance and minimize the noise. Particularly, placing a high-quality ceramic output capacitor closer to the loop than a bulk aluminum output capacitor can minimize the output voltage ripple and ripple current of the aluminum capacitor [11].

In order to prevent a dv/dt induced turn-on of high-side switch, HW and SW should be connected to the gate and source of the high-side synchronous N-channel MOSFET switch through short and low inductance paths. In FPWM mode, the dv/dt induced turn-on can occur on the low-side switch. LO and PGND should be connected to the gate and source of the low-side N-channel MOSFET through short and low inductance paths. All of the power ground connections should be connected to a single point. Also, all of the noise sensitive low power ground connections should be connected together near the AGND pin and a single connection should be made to the single point PGND. CSP and CSN are high impedance pins and noise sensitive. CSP and CSN traces should be routed together with kelvin connections to the current sense resistor as short as possible. If needed, place 100-pF ceramic filter capacitor as close to the device. MODE pin is also high impedance and noise sensitive. If an external pull-up or pull-down resistor is used at MODE pin, the resistor should be placed as close the device. VCC, VIN and BST capacitor must be as physically close as possible to the device. The LM5121 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. The junction to ambient thermal resistance varies with application. The most significant variables are the area of copper in the PC board, the number of vias under the exposed pad and the amount of forced air cooling. The integrity of the solder connection from the device exposed pad to the PC board is critical. Excessive voids greatly decrease the thermal dissipation capacity. The highest power dissipating components are the two power switches. Selecting N-channel MOSFET switches with exposed pads aids the power dissipation of these devices.

As shown in Fig. 2, the impedance of the Vout capacitor was measured after relocating the Vout capacitor close to the FET.

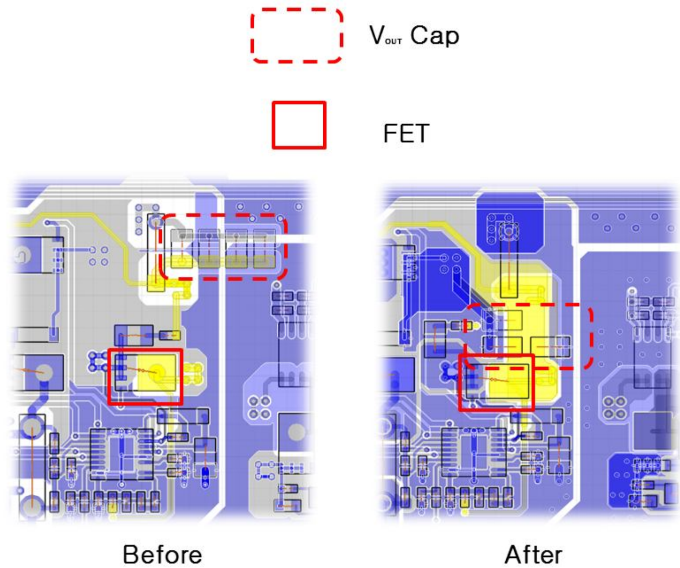

Figure 2: Before and after relocating Vout capacitor on ACM board

The measurement result is shown in Fig. 3, and the relocation of the Vout capacitor is expected to exert the lowering effect on the impedance of the Vout terminal as well as the noise source by 3 dB in the range from 1 MHz to 1 GHz. As a result, noise reduction can be further expected.

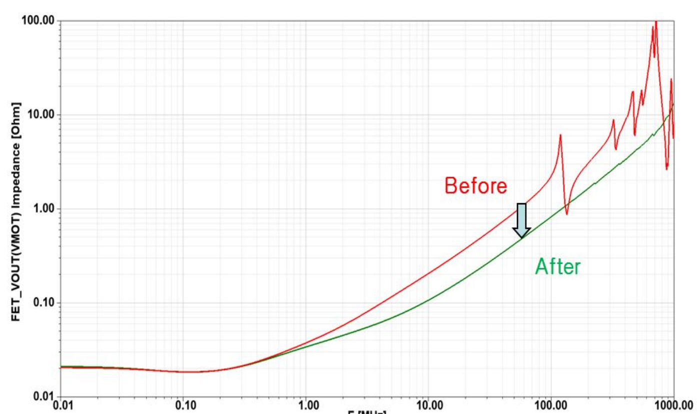

Figure 3: Measurement result on impedance in FET

2.3 Analysis and Improvement of Motor FET Driver Circuit

The main power section of the motor driver [12] is performing the switching operation, thus requiring a drive circuit. Any unsuitable drive circuit could deteriorate the performance of the device, leading to the cause breakage in worst case. Because such drive circuits are vulnerable to switching losses, the drive circuits require optimized drive circuit design to reduce these losses. This study analyzed how the capacity of decoupling capacitors affects the switching noise in an active engine mount.

Figure 4 is a design layout modified by adding a Decap to the VBB terminal.

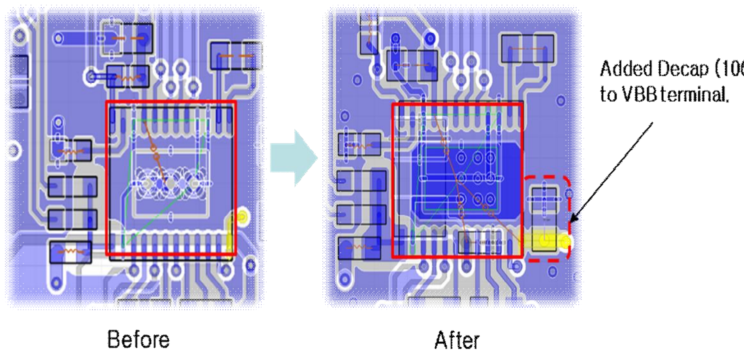

Figure 4: Addition of Decap (106K) to VBB terminal

Figure 5 shows the measurement result on impedance after adding the Decap to the VBB terminal. Because the addition of Decap leads to lowering the impedance in the 1MHz or higher band, a 3 dB to 10dB noise source reduction effect is expected, this prevents the switching noise.

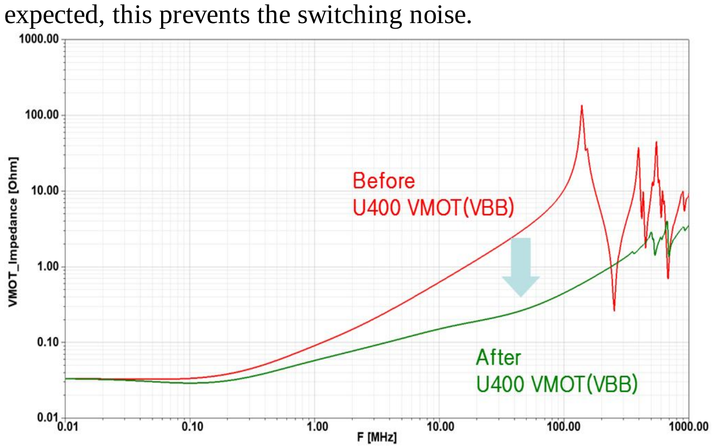

Figure 5: The result of Decap (106K) addition

In addition, change the capacity and kind of the Decap in MotorFET Driver, we can analyze the impedance change and the Noise Source reduction effect.

The (a) of Figure 6 is a comparison of the results before and after the change of the capacity of the Motor FET Driver. As shown in the figure 6, the impedance of Decap is lowered below 10MHz, so we can expect a decrease in Noise Source of about 3dB. The (b) of Figure 5 is a comparison of the results before and after the change of the type of Decap in Motor FET Driver. By changing the type of Decap, it can be seen that lowered impedance at 10kHz~10MHz bandwidth. In this result is expected to reduce Noise Source of about 3dB in the same bandwidth, although the capacity is the identical, different Decap type.

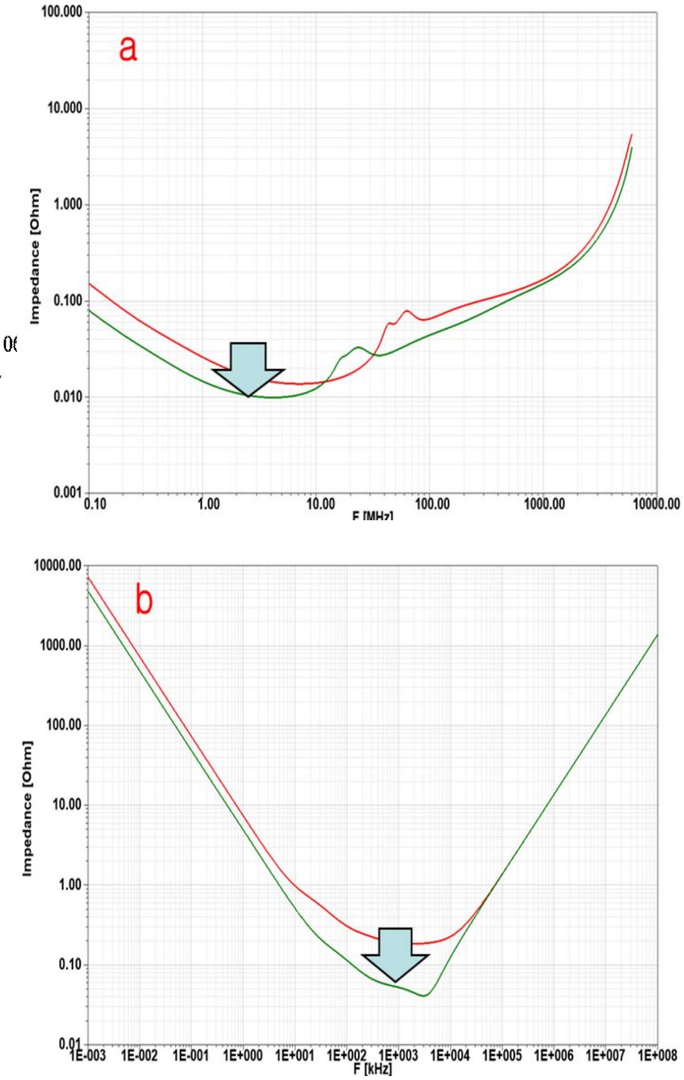

Figure 6: The results before and after the change of the capacity (a) and type(b)

Figure 7 shows the result of impedance measurement in LVREG Net after the type and capacity change of Decap.

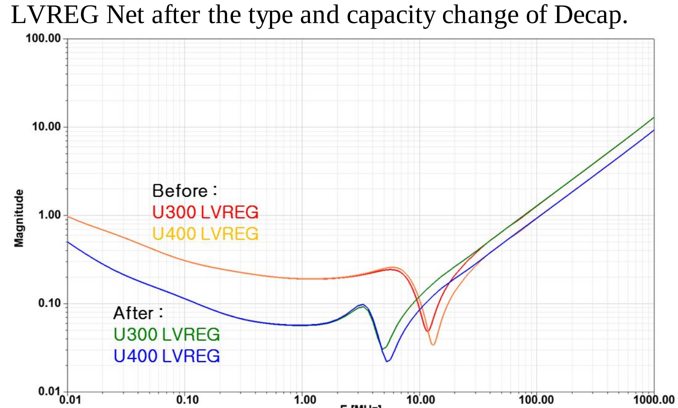

Figure 7: The comparison of LVREG Impedance before and after Decap Change in Motor FET Driver

As shown in the figure 7, the impedance of the FET Driver Out-Put terminal in the 10kHz ~ 10MHz band is lowered, so we can expect the noise source reduction of about 3dB in this frequency band. As shown above example, it can be seen that the use of appropriate Decap according to capacity and type can be used as a noise source reduction.

2.4 Analysis and Improvement of Motor FET Driver Circuit

Common Mode Noise Filter(CMNF) circuit is required to block noise from external connectors, and is important design part in noise-sensitive motor drivers. As shown in figure 8, GND between the in/out of CMNF should be sufficiently isolated, so the GND pattern of the lower part (RED box in figure 8) where CMNF is placed should be removed. The X-Cap also needs to increase the capacity of the Cap to sufficient capacity, and the Y-Cap is optimized by arranging as close to Float GND as possible.

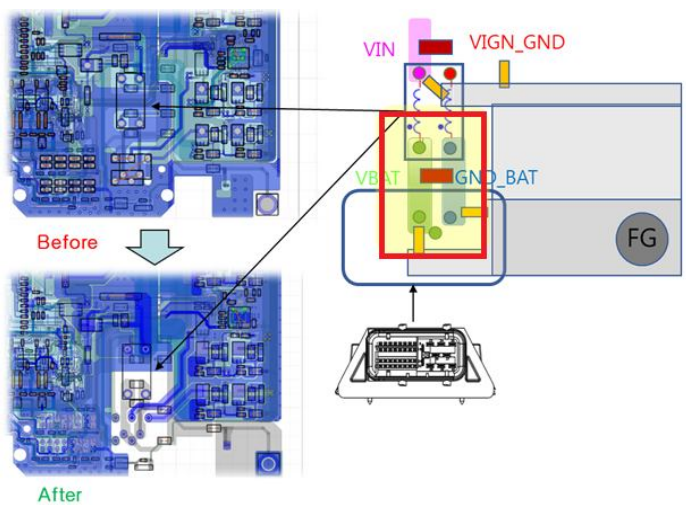

Figure 8: The result of CMNF Filter relocation

2.4 Analysis and Improvement of Motor FET Driver Circuit

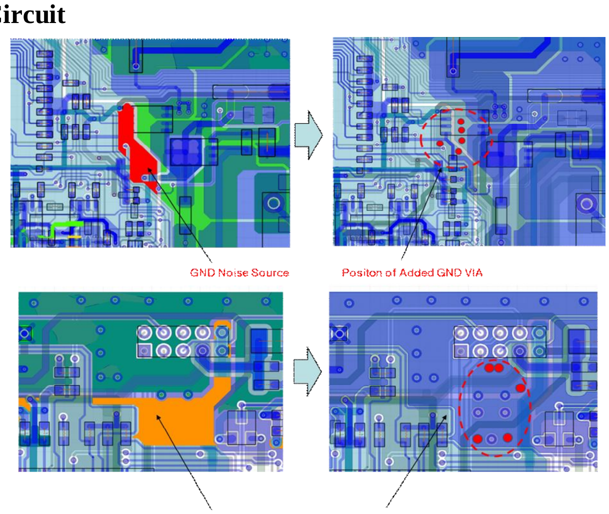

Figure 9: Noise Source change result with Ground Via addition

As shown in Figure 9, the addition of ground via can also expect a Noise Source reduction effect. Depending on the shape of the Net and pattern, the Decap cannot be added or the deformation is difficult situation sometimes. However, in this case, Via can be applied simply to reduce Noise Source.

3. CONCLUSION

This paper identified resonance and impedance characteristics of a frequency band of the circuit area, which is problematic in the design process of active engine mount, and improved the system by changing the position and capacity of the capacitor. The proposed method is expected to reduce the design cost and improve the reliability of the electromagnetic wave for the system by predicting, correcting, and improving signal malfunctions and EMC in the design process.

Future works will analyze resonance and impedance characteristics through the change of circuit region and GND type which are not discussed in the present study, and solve the problems. The study results would contribute to developing an active engine mount according to the specifications presented both at Domestic and abroad.

ACKNOWLEDGEMENT

This research paper was supported by the Yeungnam University College Research Grants in 2018.

REFERENCES

1. Bruce Archambeault, Colin Brench, Sam Connor. **Review of Printed-Circuit-Board Level EMI/EMC Issues and Tools,** *IEEE Trans. on Electromagnetic Compatibility*, Vol. 52, pp. 455-461, 2010. https://doi.org/10.1109/TEMC.2010.2044182
2. Terry M. North, James Muccioli. **Automotive EMC testing - The challenges of testing battery systems for electric and hybrid vehicles**, *IEEE Electromagnetic Compatibility Magazine*, Vol. 1, Issue. 1, pp. 97-100, 2012. https://doi.org/10.1109/MEMC.2012.6244957
3. Matsuoka, H., Mikasa, T. and Nemoto, H. **NV Countermeasure Technology for a Cylinder-On-Demand Engine-development of Active Control Engine Mount**, SAE Technical Paper Series, 2004-01-0413. https://doi.org/10.4271/2004-01-0413
4. Gennesseaux, A. **Research for New Vibration Isolation Techniques: From Hydro-mounts to Active Mounts**, SAE Technical Paper, 93-13-254, 1993. https://doi.org/10.4271/931324
5. Swanson, D. D. **Active Engine Mounts for Vehicles**, SAE Technical Paper, 93-02-432, 1993. https://doi.org/10.4271/932432

6. Aoki K, Shikata T, Hyoudou Y, Hirade T, and Aihara T. **Application of an Active Control Mount(ACM) for Improved Diesel Engine Vehicle Quietness**, SAE Technical Paper, 1999-01-0832, 1999. https://doi.org/10.4271/1999-01-0832
7. Lee, Y. W. and Lee, C. W. **Desing of Active Engine Mount Using Electro-magenetic Actuator**, in *Proc. the KSNVE Autumn Annual Conference*, 1995, pp. 208-213.
8. Leelavathi Rajamanickam, Nurul Azlia Binti Mat Saat, Siti Norbaya Binti Daud. **Software Testing: The Generation Tools,** IJATCSE, Vol. 8, No.2, pp. 231-234, 2019.
https://doi.org/10.30534/ijatcse/2019/20822019
9. Esmaeil Ghahremani, Innocent Kamwa. **Local and Wide-Area PMU-Based Decentralized Dynamic State Estimation in Multi-Machine Power Systems**, *IEEE Trans. Power Systems*, Vol. 31, Issue. 1, pp. 547–562, 2016.
https://doi.org/10.1109/TPWRS.2015.2400633
10. Ihsan Erdin, Ramachandra Achar, Kaya Erdin. **Power Integrity Aware Approach to Dynamic Analysis of Buck Converters**, *IEEE Trans. Components, Packaging and Manufacturing Technology*, Vol. 8, Issue. 1, pp. 32-40, 2018.
https://doi.org/10.1109/TCPMT.2017.2741967
11. L. Kovács, D. Fodor, R. Marschalko. **Power converter based test bench design for aluminum electrolytic capacitor development**, in *Proc. 4th International Youth Conf. Energy (IYCE)*, 2013, pp. 1-4.
https://doi.org/10.1109/IYCE.2013.6604139
12. Chang-Gyun Kim, Tae-Heon Lee, Sang-Kook Kim, Jin-Yong Jeon, Jae-Kyung Wee. **Module design using 2-layers PCB for an automotive BLDC motor driver**, *2008 Electrical Design of Advanced Packaging and Systems Symposium*, 2008, pp. 109-112.
https://doi.org/10.1109/EDAPS.2008.4736011