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Design of High Speed and Low Power Differential Voltage Charge Sharing Comparator using Small Swing Domino Logic

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ABSTRACT

Propagation delay and leakage power are the two major designing challenges in VLSI circuits, in sub-micron technologies. The paper presents here a novel dynamic charge sharing comparator with a technique: Low Voltage Power Reduction Technique(LVPRT), to decrease the propagation delayand leakage power. This comparator shares a charge to get approximately half of the supply voltage at both the outputs. The conventional analog comparators are occupies larger area due to their chain of pre-amplifiers, where as the design of dynamic comparators can avoid the general structure of chain pre-amplifier, therefore lesser area can be occupied, which in turns make us to achieve lower power consumption. The comparator proposed here has been simulated in CMOS 90nm technology node with constant supply voltage of 1V, at frequency of 100MHz using CADENCE Virtuoso tool and comparative analysis has been done with previous work. Simulation results shows that the power reduction of 66.87% and Propagation delay of 51.39% compared to previous work.

Key words : Charge Sharing, Dynamic Comparator, Leakage Power, Propagation Delay.

1. INTRODUCTION

Comparator plays major role in several application like data transmission, power regulators, zero crossing detectors, peak detectors etc. It can compare two inputs and gives a single output based on input voltage(V_{in}) and reference voltage(V_{ref}). If $V_{in} > V_{ref,}$ the output becomes “1” otherwise “0”. The major factors while designing of comparator are speed, power and area. Many Analog to Digital Converters(ADCs) that are especially used in portable devices have limited power supply energy uses the comparator. The conventional analog comparators are occupies larger area due to their chain of pre-amplifiers, so higher power consumption and lower speeds. However, when we go for the sub-micron technologies the threshold voltage of the CMOS devices are not shrinks same rate as the technology [1]. Which leads to increasing the complexity of the comparator design at lower supply voltages.

Besides, the design of dynamic comparators can avoid the general structure of chain pre-amplifier, therefore lesser area can be occupied, which in turns make us to achieve lower power consumption. The general idea of designing dynamic comparators are either outputs are charged V_{dd} or discharged to gnd. The overview of the several dynamic comparators, such as double tail comparators, differential pair comparator, Lewis-Grey comparator resistive diode comparator, and dynamic latched comparatorare discussed in [2]. These CMOS dynamic comparators uses the regenerative inverter latch structure to convert the small change in input signal, which in turns achieve low power and high speed [3]. These dynamic comparators works in the two phases called: (1) Pre-charge phase (2) evaluation phase. In phase one, the output capacitors outp and outnare charged to $V_{dd.}$ In phase two, the outputs outp and outn are conditionally discharges based on the input and reference voltages [4]. Figure 1 shows the taxonomy of comparator.

There are many comparator which uses charge sharing logic[1,5-8], Where the NMOS pass transistor is used in pre-charge phase to share a charge between outputs outp and outn with approximately equal to half of supply voltage(V_{dd}). The output capacitors should not go less than threshold voltage.Which leads us to comparing of input signals becoming speed ups.

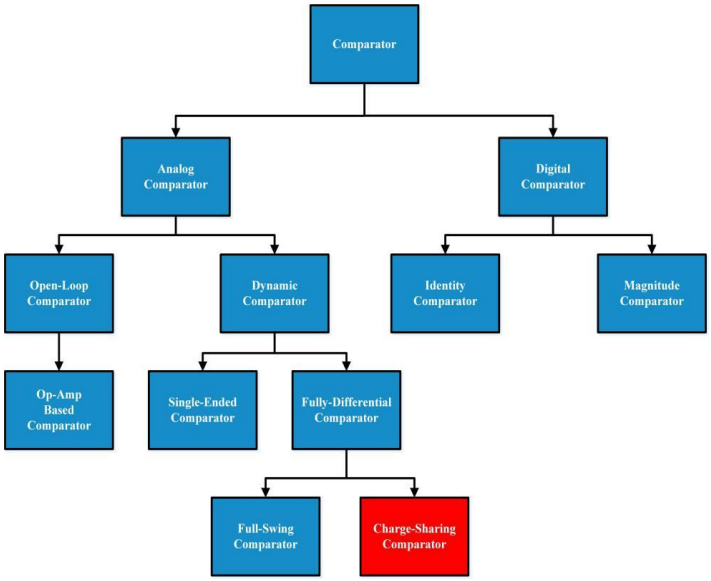


Figure 1: Taxonomy of the Comparator

Therefore reduction in the power dissipation and propagation delay of comparator [1]. In paper [7] to get a low power and higher speeds, inputs have taken in a complementary differential pair and also uses the charge sharing logic. Which also not required many stacking transistors or voltage boosting circuits and works at a lower supply voltages. They are several techniques to reduce leakage power consumption, which has been divided in two types: (1) State Destructive and (2) State Preserving techniques [9]. Where MT-CMOS, SC-CMOS, DT-CMOS etc are fall under state destructive techniques and transistor stacking, LECTOR, Sleepy stack, sleepy keeper, VCLEARIT[11]etc are fall under state preserve techniques. In paper [7] they have used a state preserve power reduction technique is used: leakage control transistor(LECTOR) and achieved a low in power and delay of the comparator compared to existing methodologies. Which has been discussed later in the section 2 of the paper. This paper presents a novel dynamic differential comparator, which can improve the reduction in total power consumption and propagation delay and details can be explained in section 3, which is compared to previous work.

The organization of paper divides into five main sections: the section 2 discusses the review of related work, the section 3 to deals with proposed work, the section 4 presents simulation results and comparative analysis and the section 5 depicts the conclusion of the work.

2. REVIEW OF RELATED WORK

2.1 Dynamic Latch Charge Sharing Comparator

The comparator shown in figure 2 depicts the CMOS Dynamic Latch Charge Sharing Comparator circuit topology. In a regeneration phase to get a low power, a resistive comparing input circuit is used in series with the NMOS. During pre-charge phase, there is no M10transistor and the transistor M5 equally divides the two output voltages to approximately half of the supply voltage. During this the circuit is removed from the VDD and ground voltage by the M11 and M10 transistors [7]. This has been simulated in 90nm CMOS technology node at constant supply voltage of 1V and at a frequency of 100MHz. The simulated results shows that the power dissipation of 9.913μW and the propagation delay of 5.469ns. The problem with this circuit topology is the more consumption of total average power.

2.2 Small Swing Domino Charge Sharing Comparator

The comparator shown in figure 3 presents the A Small Swing Domino Charge Sharing Comparator circuit topology. This circuit topology uses the power leakagereduction technique: Leakage control transistor(LECTOR) and achieves a low in power and delay of the comparator compared to [7,10]. This LECTOR circuit topology says that "the stage with one or more transistors OFF in supply to Gnd path is less leaky than the stage with only one transistor is OFF in a path of VDD to Gnd". The transistors L1 and L2 are the LECTOR transistors, in which one of the transistor in nearly equal to cut-off region always, irrespective of the input. The inclusion of LECTOR transistorsL1 and L2 improves the path resistance from supply to Gnd [8]. Which also improves the propagation delay. To combat with this effect the leakage control transistors L1 and L2 has to be sized properly to get approximate delay of the conventional counterpart. Generally, this L1 and L2 are the high V_{th} transistors.

The operation of the comparator as follows, in pre-charge mode when clock is '0' the transistors M10 and M11 are disconnected the inverter latch from VDD and Gnd respectively. The output is given by the NMOS pass transistor M5. Which equally divides the outputs outp and outn to half of the supply voltage $V_{dd}/2$ [8]. During this phase node X and node X1 are charged to supply voltage and the transistor L1 is substrate biased to node X, which switch OFFs the L1 transistor. Therefore no current flows through the L1, so even at logic '1' $V_x<V_{dd}$.The operation of the comparator as follows, in pre-charge mode when clock is '0' the transistors M10 and M11 are disconnected the inverter latch from VDD and Gnd respectively. The output is given by the NMOS pass transistor M5. Which equally divides the outputs outp and outn to half of the supply voltage $V_{dd}/2$ [8]. During this phase node X and node X1 are charged to supply voltage and the transistor L1 is substrate biased to node X, which switch OFFs the L1 transistor. Therefore no current flows through the L1, so even at logic '1' $V_x<V_{dd}$.

In evaluation Phase when clock is '1', NMOS input circuit can discharge or maintain outputs based on inputs and reference voltages. At the same time the NMOS input circuits and inverter latch gives a less power by the series connection of these topology[8]. This has been simulated in 90nm CMOS technology node at constant supply voltage of 1V and at a frequency of 100MHz. The simulated results shows that the power dissipation of 3.746μW and the propagation delay of 5.189ns.The Width and Lengths of the previous worksare shown in table 1.

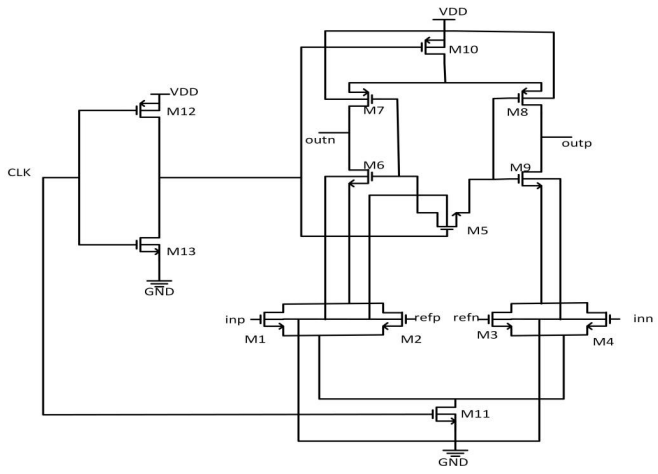


Figure 2:A Charge Sharing CMOS Dynamic Comparator [7]

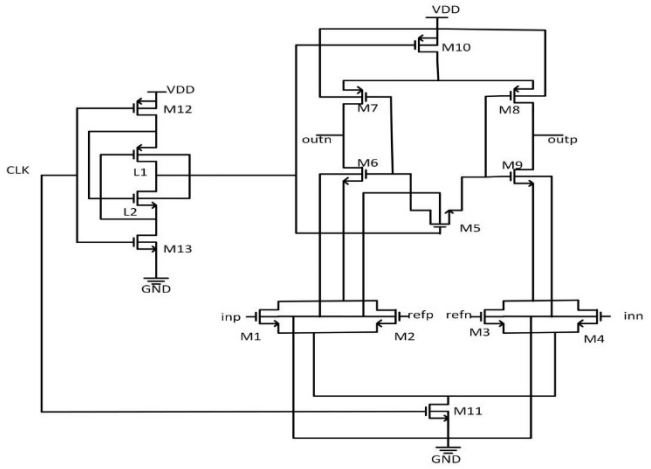


Figure 3:A Small Swing Domino Charge Sharing Comparator [8]

Table 1: Width and Lengths of the Transistors

For Charge Sharing Dynamic Charge Comparator [7]	
Length	100nm
W_p/W_n	6μ/3μ
For Small Swing Domino Charge Sharing Comparator [8]	
Length	100nm
W_p/W_n	2μ/1μ

3. PROPOSED WORK

The comparator shown in figure 4 presents the a proposed Charge Sharing Comparator circuit topology. This circuit topology uses the leakage power reduction technique: Low Voltage Power Reduction Technique(LVPRT)and achieves even a low in power and delay of the comparator compared to [7] and [8]. This LVPRT circuit topology says that "there is a balancing of voltage levels by using the combination of the standard and high V_{th} sleeper transistor devices with a well balanced trade-off between the delay and the power". This LVPRT circuit topology consists of the three sleeper devices, which are two PMOS devices {S1 and S3} and one NMOS device {S2}. The sleeper transistor S3 is the high threshold voltage device, which is sized to get a low delay as the conventional CMOS circuits. The sleeper transistors S1 and S2 standard threshold devices to maintain a sufficient supply levels at the pull-down and pull-up networks. The pull-up and pull-down networks connected parallel to the input CMOS devices and the output of this circuit taken at a node Y2.

Here the input to the sleeper transistors is same as the clock. In pre-charge mode when clock is '0', the transistors S1, S2 are OFF and S3 is ON. Now the circuit acts same as the normal CMOS circuit and the transistors M10 and M11 are disconnected the inverter latch from VDD and GND respectively. The output is given by the NMOS pass transistor M5. Which equally divides the outputs outp and outn to half of the supply voltage $V_{dd}/2$.

In evaluation Phase when clock is '1', NMOS input circuit can discharge or maintain outputs based on inputs and reference voltages. At the same time the NMOS input circuits and inverter latch gives a less power by the series connection of these topology. During this phase, the sleeper transistors S1,

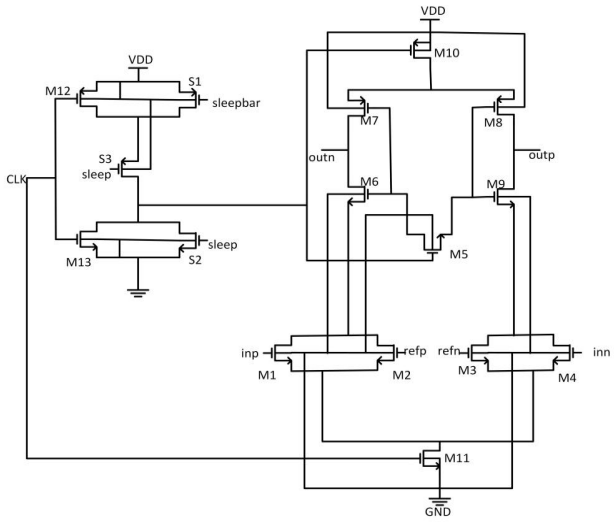


Figure 4: Proposed comparator circuit topology

Table 2: Width and Lengths of the Transistors

For the proposed comparator circuit topology	
Length	100nm
W_p/W_n	240nm/120nm

S2 are ON and S3 is OFF. Since S1 is ON, node Y1 is also at supply voltage V_{dd}. Therefore now the pull-up network is between the two common voltages of $V_{dd}$and hence no leakage from the pull-up network. Also the sleep transistor S2 is ON, hence the node Y2 also at the ground. This causes Pull-down network is between the two common voltages of ground and hence no leakage from the pull-down network. During this phase the node Y2 always at logic '0', therefore the output is also at logic '0'. The only leakage can occur in this phase is through the sleep transistor S3 and which is OFF, because, the nodes Y1 and Y2 are connected between the two different voltages.

This has been simulated in 90nm CMOS technology node at constant supply voltage of 1V and at a frequency of 100MHz. The simulated results shows that the power dissipation of 1.241μW and the propagation delay of 2.522ns. This contributes to the percentage reduction of total average power consumption and Propagation delay of 66.87% and 51.39% respectively compared to previous work [8].The Width and Lengths of the Proposed workis shown in table 2.

4. SIMULATION RESULTS AND COMPARATIVE ANALYSIS

This has been simulated in 90nm CMOS technology node at constant supply voltage of 1V and at a frequency of 100MHz. Figure 5 shows the output wave forms of charge sharing proposed comparator. The input voltages $V_{inp}$and $V_{inn}$of '+1V' and '-1V' of 10ns pulse signals respectively and reference voltages $V_{refp}$and V_{refn} of '+0.5V' and '-0.5V' respectively.

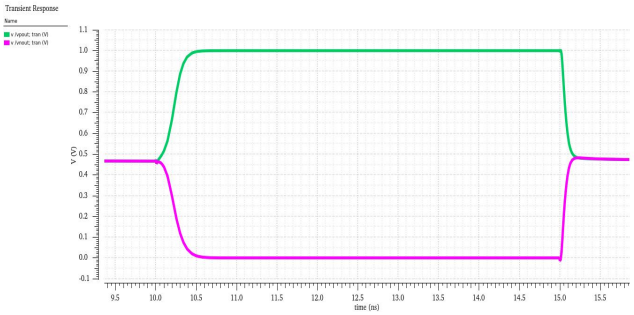


Figure 5: Output wave forms of the proposed charge sharing comparator

4.1 Propagation Delay of Comparator

The speed of the comparator is the main parameter which will be determined by the Propagation delay. The speed of the comparator will be lower, if there is a high the propagation delay and vice versa. It can be calculated based on the two timing intervals 't_{phl}' and 't_{plh}'. The propagation delay can be mathematically written as

$$\frac{t_{phl} + t_{plh}}{2}$$

Figure 6 depicts the delay of the work [8] and delay is 5.189ns, where as the figure 7 depicts the delay of proposed work and delay is 2.522ns. The table 3 shows the comparison of the propagation delay between present and previous work. Table 4 shows the percentage of delay reduction compared to work [7] and [8].

Table3: Comparative analysis of propagation delay between previous and present work

Work	outputs	T_{phl}(s)	T_{plh}(s)
[7]	outp	9.586n	1.452n
	outn	136p	194.8p
[8]	outp	5.326n	5.052n
	outn	-0.998p	0.018n
Present Work	outp	5.028n	15.2p
	outn	-0.409a	17.53p

Table 4: Delay reduction in % compared to previous works

Work	[7]	[8]
Reduction in %	53.88	51.39

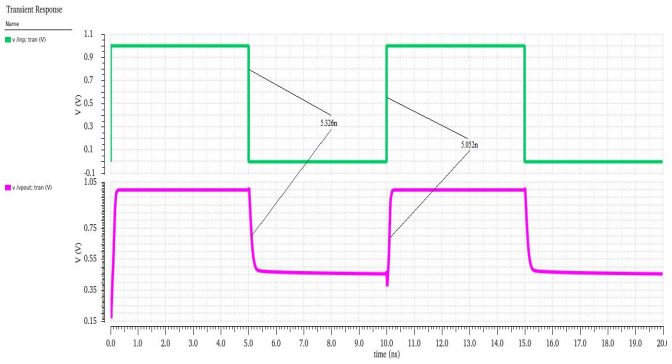
Table5: Power reduction in % compared to previous work

Work	[7]	[8]
Reduction in %	87.48	66.87

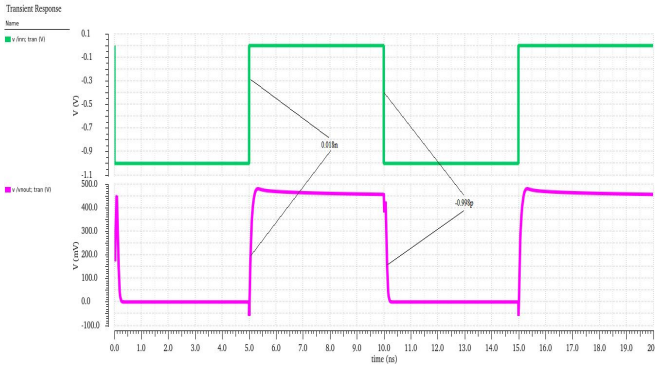
4.2 Total Power Dissipation

Reduction in total power dissipation is the main parameter in any of the circuit design along with delay of the circuit design. It can be calculated mathematically as the product of voltage applied at supply(V_{dd}) and current(I_{dd}) in the circuit.Table 5 shows the percentage of power reduction compared to work [7] and [8].

$$\text{Power(P)} = V_{dd} \times I_{dd}$$

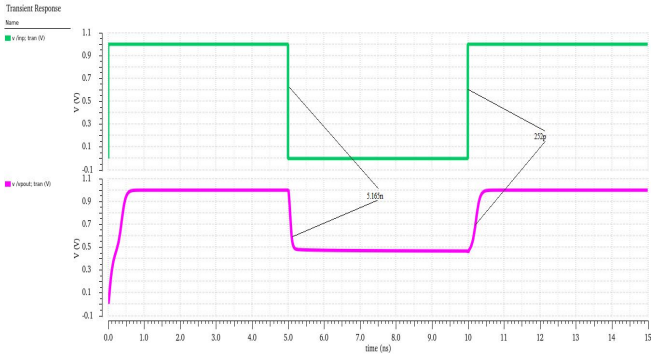


(a)

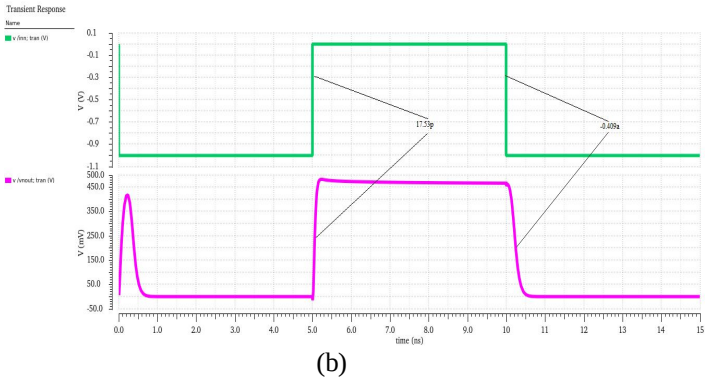


(b)

Figure 6: Propagation delay of comparator [8]



(a)



(b)

Figure 7: Propagation delay of proposed comparator

Table 6 : Total comparative analysis of previous work and present work

Parameters	Previous work[7]	Previous work[8]		With novel power reduction technique	
		Without power reduction technique	With power Reduction technique		
Technology	90nm	90nm	90nm	90nm	90nm
Supply Voltage	1V	1V	1V	1V	1V
W_p/W_n	6μ/μ3	2μ/1μ	2μ/1μ	2μ/1μ	240nm/120nm
average power(μW)	9.913	5.213	3.746	3.288	1.241
Frequency(MHz)	100	100	100	100	100
Input difference (Δv_{in}) (mV)	500	500	500	500	500
No.of Transistors	13	13	15	16	16
Delay(ns)	5.469	5.240	5.189	5.020	2.522
PDP(fs)	44.701	14.674	19.437	16.505	2.656
Energy efficiency(fj/conv)	99.13	52.13	37.46	32.88	12.41

5. CONCLUSION

This paper presents a novel charge sharing differential voltage comparator using small swing domino logic with lower power and high speed. To increase the speed of the comparator the outputs have been equalized to half of the supply voltage and to decrease the total power dissipation of proposed design, the power leakage reduction technique: Low Voltage Power Reduction Technique(LVPRT) is used. Which in turns reduction in power 87.48% and 66.87% compared to work [7] and [8] respectively. Total comparative analysis of present work and previous work is show in table 6. Which shows that, this topology can be highly optimized in delay and power compared to existing works.

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