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Development and Implementation of a Board Checker for Fast Loop Circuitry in Testing Microelectronic Packages

Jeffrey P. Abillar[1], Marilyn A. Aceron[2], Glenn N. Ortiz[3], Mark Joseph B. Enojas[4]
[1]Analog Devices Inc., General Trias Cavite, Philippines, jeffrey.abillar@analog.com
[2]Analog Devices Inc., General Trias Cavite, Philippines, Marilyn.aceron@analog.com
[3]Technological University of the Philippines Taguig, Philippines, glenn.46@yahoo.com
[4]Technological University of the Philippines Taguig, Philippines, markjoseph_enojas@tup.edu.ph

ABSTRACT

This paper presents a method of development and implementation of a board checker for Fast Loop Circuit (FLC) for Microelectronic Packages test. Some microelectronic package has fast loop circuitry which has instrumentation amplifiers installed. These are connected to the device under test (DUT) such as operational amplifiers test boards. A fast loop topology (FLT), which is composed of three instrumentation amplifiers, are used to function as precision close-loop gain blocks for the board checker. These amplifiers are used for differential measurements to obtain offset voltage and input bias current measurements. A program was developed to measure these parameters and to compute the gain for evaluation. The checking of such amplifiers in fast loop circuits needs more integrity to avoid rejects and down time in the production of microelectronic packages. A device interface board (DIB) is introduced to interface the DUT and the board checker. A case study was attempted to be resolved about returned products due of failure in meeting the desired specifications due to over acceptance of the board checker with large offset voltage and out of range bias current. Several samples of Analog Devices products were tested using the board checker. The results show that the developed checker was able to detect good samples with higher accuracy and repeatability and were recommended for use in test processes in the production of microelectronic packages.

Key words: Board checker, fast loop topology, microelectronic packages, instrumentation amplifiers

1. INTRODUCTION

Microelectronic packages produced by semiconductor companies are tested thru a device under test (DUT) boards, which are composed of different circuitries. A lot of testing is done from test devices such as automated test equipment (ATEs), to the DUTs are being done to ensure high quality microelectronic products. Other issues that may affect in working in low powered microelectronic devices and its packaging, such as electrostatic discharge and material processing, are treated using sealing and protections [1][2][3]. In testing microelectronic products, isolating and debugging hardware is difficult specially when other manufacturers have different designs and standards. Therefore, testers, or sometimes called board checker should be able to adopt physically and electronically to the DUT. A device interface board (DIB) has been introduced to the test head of a tester which sends signals from the DUT to the tester for evaluation. In case studies that have been conducted, there are voltage offsets (VOS) found and verified through ATE and bench testing. The post-chemical de-capsulation showed no die surface anomaly and shows that instrumentation amplifiers installed for fast loop circuitry (FLC) in a microelectronic package with a program driven calibration factor obtains result that is significantly lower than the expected failed and thus results to customer returns due to voltage offset and over acceptance of lot.

1.1 Circuit or Board Checker

Circuit check or board check evolves and changes the test fixtures and systems of microelectronic product developers. This checkers has routine programs in automated test equipment (ATE) to verify the integrity of the circuit design and components. The system ATEs are designed to reduce the amount of test time needed to verify the functionality and quality control of microelectronic packages [4]. There are different metrics for assessment of microelectronic packages such as that incorporates assessment on performance, manufacturability, and efficiency [5]. Other than ATEs used for tests, some resorts on developing multifunctional test chips which extracts device properties [6]. There are also hardware checker modules developed which uses checker program to identify faults and prevent downtime [7].

1.2 Design Challenges

To reduce manufacturing costs and improve yield,

semiconductor devices are being tested before it is being put to the circuit boards. Tests are dependent of the test devices and test programs. On the other end, quality assurance is conducted while these devices are installed in the circuit board. Board checkers need such programs that could detect faults on the devices or on the specific part of the board, or sometimes called the site. Commonly, board checkers use servo loop topology which are composed of two operational amplifiers loop with one DUT and one Null amplifier. In this measurement process, the null or zero voltage is forced at the amplifier input, thus allowing the amplifier under test to measure the error. This setup is an error-sensing negative feedback that is used as a correcting signal. Other developers use simulation software to somehow predict the functionality of microelectronic packaging such as finite element analysis method. There is still exits a quest in predicting failures in designs in order to make better quality products [8][9]. Non-destructive means are also developed such as presented by [10] which uses acoustic microscopy. Additionally, drop tests are also conducted considering the solder quality and the reliability of microelectronic packages under worse conditions [11].

This research concentrates on board checking of instrumentation amplifiers in FLC installed in each production site for microelectronic packaging. The board checker is programmed and inserted for checking packages before starting setups to detect quality issues to make the isolation of devices to be efficient and fast in every start of the setup. A board checker was developed with DIB to interface FLC and the DUT in testing microelectronic packages. See Fig. 1 for the major sections of the low cost tester. As an advantage, this research lessens the customer return, detects lot over acceptance, and additionally helps technicians to easily identify board related issues in every initial setup in the low cost tester (LCT) by reducing the isolation time and predicting failures of boards in the sites. The board checker for the FLC is integrated to the low cost tester in Fig. 1, for microelectronic packages from Analog Devices Inc. (ADI) such as AD8045, AD8031, D8041, and AD8099 with completed SECNs. DUT boards with fast loop circuitry can check the functionality of instrumentation amplifiers prior to isolation. A program written in C++ was developed and generated for board checking and implemented by embedding it to the existing system in ADI Philippines.

Figure 1: Major sections of a low cost tester

2. METHODOLOGY

2.1 FLC for Circuit Checking

The fast loop topology (FLT) is a circuit which is composed of three instrumentation amplifier to allow checking of signals to the DUT. As an example, an operational amplifier is tested using the FLT developed as presented in Fig. 2. The critical test measurements that can be performed using the checker are the offset voltage (VOS), positive and negative input bias current across the DUT, and the instrumentation amplifier inputs. In this setup, the faulty component can be diagnosed and in result, reduce the probability of failure and lessen potential risks in the circuit. This was simulated using the NI Multisim.

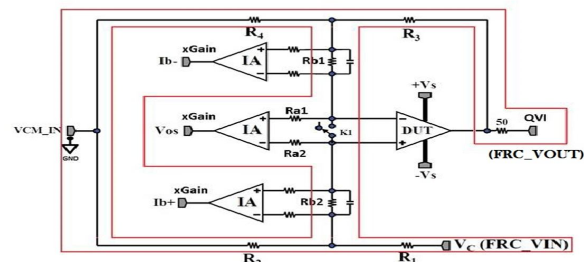

Figure 2: Fast loop topology using three instrumentation amplifiers

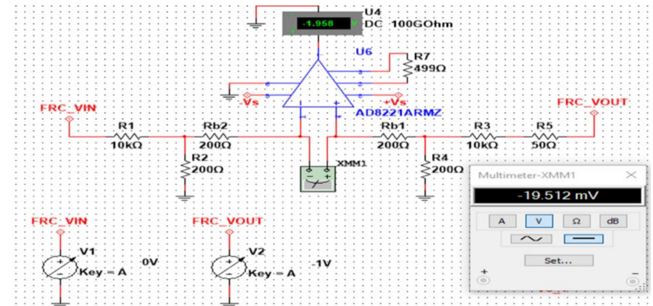

Figure 3: Simulated Test for VOS

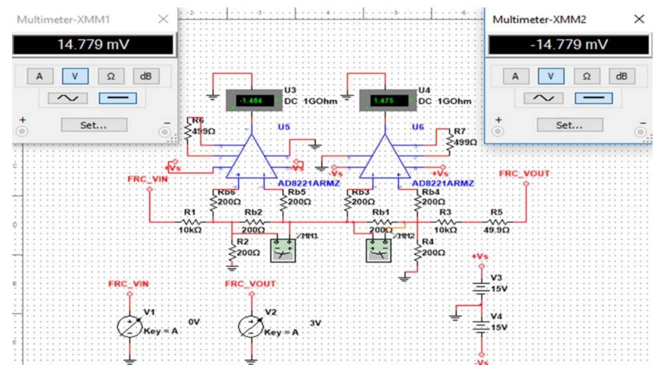

Figure 4: Simulated Test for ± Ibias

2.2 FLC Circuit Analysis

In order to check the VOS, a relay should be de-energized such that ±1V for two level testing is forced at FRC_VIN and/or QVI at the DUT output (FRC_VOUT) to serve as the

differential input at the instrumental amplifier. See Fig. 3. The measured output voltage is saved in a register for gain computation. To check the input bias current, a ±3V for two level testing is forced at FRC_VIN and/or QVI at the DUT output (FRC_VOUT) to serve as the differential input at the instrumentation amplifier. The gain is computed using (1).

$$Gain = \frac{V_{out2} - V_{out1}}{V_{in2} - V_{in1}} \quad (1)$$

The V_{out1} and V_{out2} are the measured instrumentation amplifier output at first and second level differential output respectively, while the V_{in1} and V_{in2} is the first and second level differential input respectively. The values for the setup in Fig. 2 are as follows: R3 = 10k ohms; R4 = 200 ohms; Rb1 = 200 ohms; Rb2 = 200 ohms; R1 = 10k ohms; R2 =200 ohms. For a positive level with gain of 100, FRC_VIN at 0V, and FRC_VOUT at 1V, V_{out1} is 1.951V and V_{in1} is 0.091512V. In the negative level with gain at 100, FRC_VIN at 0v, and FRCVOUT at -1V, V_{out2} is -1.951V, and V_{in2} is -0.019512V. These gain values should match the data sheet specifications.

2.3 Software Design and Project Development

A pseudo code has been constructed for the FLT that is present in the DIB. It can save measurements of the tester when compiled and run. The data is then evaluated from the tested units. The Software Engineering Change Notice (SECN) is accomplished as a proof when the process is complete and verified to be ready for production use.

2.4 Project Testing and Evaluation

The DIB is attached to the test head of the tester to validate and verify that the new program was generated. Loading the new program automatically performs checking fo the FLC and performs board checking. Several good and bad sample products are tested to calibrate and validate the board checker program. All of the test passed and verified. Accuracy and reliabity test is conducted to meet the required criteria of the customer. Functionality test is also conducted to evaluate the capability of the board checker with different desired device specifications accordingly to the SECN.

3. RESULTS

3.1 Software and Hardware Design Results

Using the DIB, the board checker developed will be integrated to the existing low-cost tester. The DIB is mounted to the test head to load the program and start the analysis. The actual DIB is presented in Fig. 5. The actual application of LCT based testers used to copy production program to the saved commands are used to edit or insert the new program. See Fig. 7.

A reflection of the file transfer protocol client application was used to replace the existing production program with the new board checker program. The pseudo code for the new program is presented in Fig. 6. The parameters are initialized first, given the resistor values mentioned in Section II.B. The current site is first identified so that it can locate the particular instrumentation amplifier. Both positive and negative parameters examined and the gain for each condition is computed for evaluation. The gain lower and upper limit is at 95 to 105. This process is done after the codes are transferred and run. The newly generated program is loaded into the board checker codes as presented in Fig. 8. This tester tool application presents only the LCT/CTS testers.

Figure 5: Actual Device Interface Board

Pseudo Code for Evaluation

```
1:   initialize parameters Vin1, Vin2, Vout1, Vout2 and input given resistor values
2:   identify current site
3:   // for positive Ib gain
4:   force FRC_Vout = 3V and FRC_Vin = 0V
5:   calculate Offset Voltage gain of instrumentation amplifier Vos_inamp_gain
6:   // for negative Ib gain
7:   force FRC_Vout = -3V and FRC_Vin = 0V
8:   calculate Offset Voltage gain of instrumentation amplifier Vos_inamp_gain
9:   compute for gain
10:  switch (sites)
11:        {
12:        case 1: // for site 1
13:              if gain>95 && gain<105
14:                    printf "passed"; // site 1 passed, proceed
15:              else
16:                    printf "failed"; // proceed
17:        case 2: // for site 2
18:              if gain>95 && gain<105
19:                    printf "passed"; // site 2 passed, proceed
20:              else
21:                    printf "failed"; // proceed
22:        case 3: // for site 3
23:              if gain>95 && gain<105
24:                    printf "passed"; // site 3 passed, proceed
25:              else
26:                    printf "failed"; // proceed
27:        case 4: // for site 4
28:              if gain>95 && gain<105
29:                    printf "passed"; // site 4 passed, proceed
30:                    else
31:              printf "failed"; // proceed
32:        break;
33:        }
```

Figure 6: Pseudo code for board checking

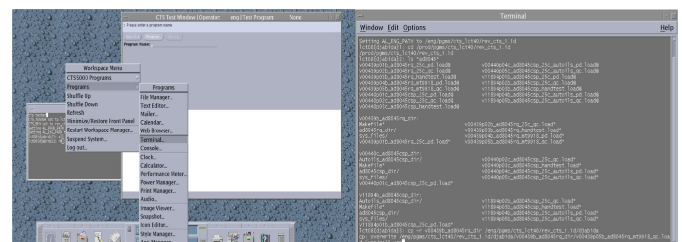

Figure 7: Terminal application used as input interface for inputting commands

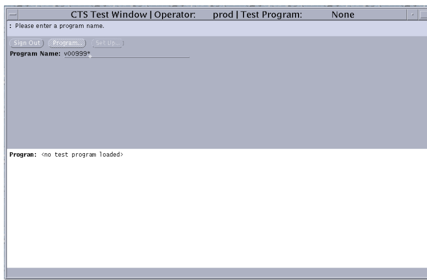

Figure 8: Tester tool of LCT system

Figure 9: Board checker output

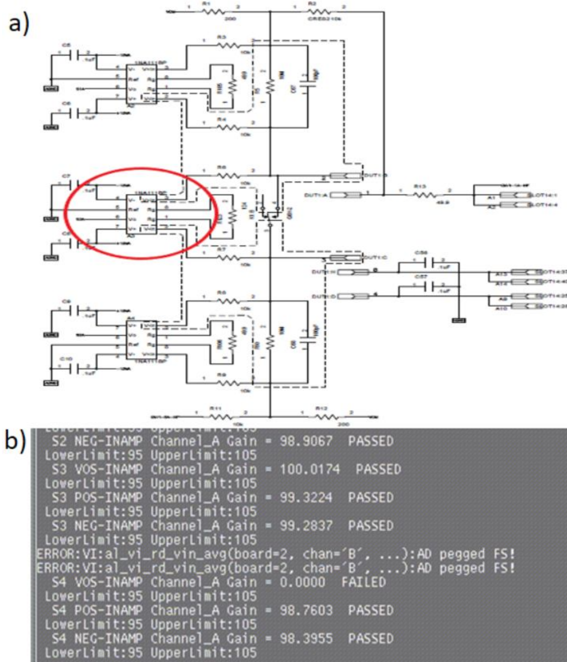

Figure 10: Detection of faulty VOS of instrumentation amplifier on site 4. a) circuitry, b) notification of error/fault

3.2 Functionality Results

Using the DIB, the board checker developed will be integrated to the existing low-cost tester. The DIB is mounted to the test head to load the program and start the analysis. The actual DIB is presented in Fig. 5. The actual application of LCT based testers used to copy production program to the saved commands are used to edit or insert the new program. See Fig. 7.

Board checker initiates checking when the developed program is loaded and run. Fig. 9 presents the board checker passed, satisfying the required parameters. Fault simulation was done by replacing reject instrumentation amplifier unit on the DIB. This verifies that the new program is able to detect faulty circuitry and to identify the reject or damaged instrumentation amplifier, and detached components. The actual fault simulation was conducted by replacing one instrumentation amplifier unit from the DIB with defective or reject unit at site 4. See Fig. 10. Series of tests are conducted showing the specific error or fault on instrumentation amplifiers with bias on specific sites identified. See Fig. 11 and Fig. 12.

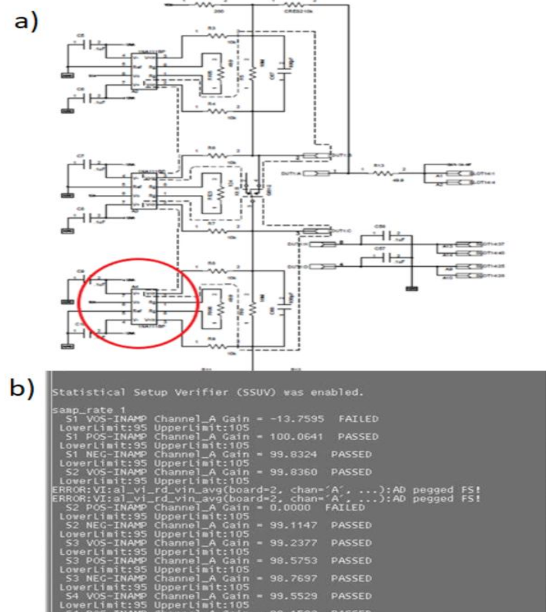

Figure 11: Detection of faulty instrumentation amplifier with Ibias on site 2. a) circuitry, b) notification of error/fault

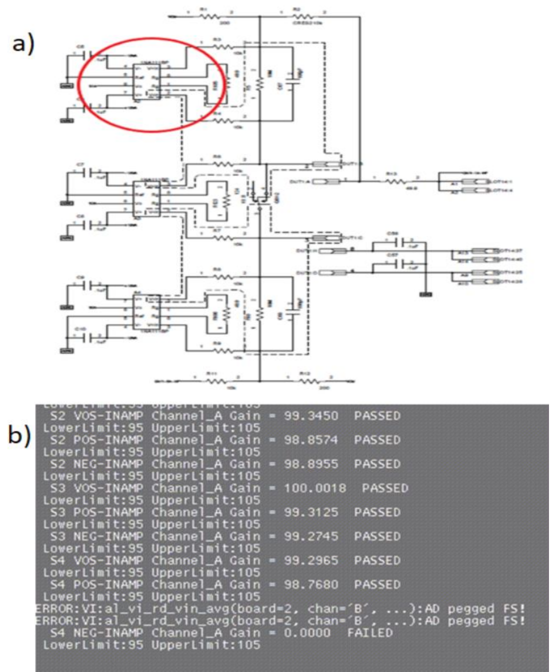

Figure 12: Detection of faulty instrumentation amplifier with Ibias on site 4. a) circuitry, b) notification of error/fault

Data correlation was also conducted for comparative analysis of the old and the new program generated. Testing is repeatedly done a hundred times with good sample units to check the repeatability and to compare the old and the new program functionality. The results show that the old and the new program significantly match as presented in the data distribution. See Table 1. This signifies that the developed program functions well in terms of the parameters listed in Table 1. Therefore, the functions are kept using the new program yet having advantage of detecting faults in the in the offset voltage and the particular site where the device is located.

Table 1: Correlation Data comparing the parameter data between the old and new board checker program

Analysis Data View Report — Wednesday 22 May 2019

Test Number	Test Name	Units	Test Result	Mean Shift Criteria	% Mean Shift Over Limit Range	Mean Old Platform	Mean New Platform	Sigma Spread Criteria	Stdv Ratio	Stdv Old Platform	Stdv New Platform	Cpk Old Lo	Cpk Old Hi	Cpk New Lo	Cpk New Hi
1	Test Site	null	PASS	PASS	0.00	2.5	2.5	PASS	0.998746	1.12084	1.119434	0.74349	0.74349	0.744424	0.744424
2	Comp Cap Pin Continuity	V	PASS	PASS	0.325812	-0.022581	-0.021603	PASS	0.900633	0.011792	0.01062	-26.080224	34.560857	-28.92699	38.343297
3	Is Fl +/- 2.5V	mA	PASS	PASS	0.832507	14.593948	14.567307	PASS	1.145492	0.058707	0.067248	14.728207	3.441114	12.725486	3.136097
4	Is Dis +/- 2.5V	mA	PASS	PASS	0.580793	1.460494	1.456719	PASS	1.018981	0.005885	0.005997	26.083797	10.734189	25.388069	10.744091
5	Is Fl +/- 5.0V	mA	PASS	PASS	0.667252	15.065556	15.048208	PASS	1.08303	0.05994	0.064917	11.48676	2.972101	10.517055	2.833328
6	Is Dis +/- 5.0V	mA	PASS	PASS	0.410483	1.744524	1.740625	PASS	1.043132	0.007519	0.007844	33.005108	9.108843	31.474666	8.897926
7	V Offset Fl +/- 2.5v	uV	PASS	PASS	0.131161	-7.146267	-5.913357	PASS	1.092531	3.330181	3.638327	46.32918	47.759787	42.518322	43.601853
8	V Offset Fl +/- 5.0v	uV	PASS	PASS	0.124154	-42.623224	-41.456178	PASS	1.07408	3.198374	3.435309	44.541044	53.425396	41.582268	49.627382
9	+Input Ibias En +/- 2.5v	uA	PASS	PASS	0.018144	-0.053557	-0.054283	PASS	0.966922	0.013768	0.013313	47.124754	49.718062	48.718676	51.437042
10	-Input Ibias En +/- 2.5v	uA	PASS	PASS	0.171251	-0.083098	-0.089605	PASS	0.827525	0.011301	0.009352	53.589517	58.49145	64.526853	70.914351
11	I Offset En +/- 2.5v	nA	PASS	PASS	0.118296	33.590805	35.483543	PASS	0.891237	7.46573	6.653732	37.218544	34.218988	41.855382	38.30013
12	+Input Ibias Fl +/- 2.5v	uA	PASS	PASS	0.037077	-5.669935	-5.674495	PASS	1.244732	0.007252	0.009026	327.750923	237.648719	263.141995	191.092005
13	-Input Ibias Fl +/- 2.5v	uA	PASS	PASS	0.041509	-5.668036	-5.673142	PASS	0.826885	0.0063	0.005209	377.377394	273.459021	456.057755	331.036644
14	I Offset Fl +/- 2.5v	nA	PASS	PASS	0.074532	-2.503239	-1.459794	PASS	1.13461	6.099836	6.920932	38.115603	38.389188	33.643839	33.784456
15	+Input Ibias Fl +/- 5.0v	uA	PASS	PASS	0.189001	-5.355857	-5.332799	PASS	0.170786	0.059145	0.010101	40.826717	27.93034	239.813143	162.779317
16	-Input Ibias Fl +/- 5.0v	uA	PASS	PASS	0.006244	-5.314902	-5.31414	PASS	0.435485	0.012816	0.005581	189.47931	127.832466	435.145346	293.495185
17	I Offset Fl +/- 5.0v	nA	PASS	PASS	1.318588	-37.355887	-18.368224	PASS	0.122474	46.785489	5.730025	4.863646	5.395946	40.816101	42.953174
18	+Input Ibias En +/- 5.0v	uA	PASS	PASS	1.578467	-0.087894	-0.027912	PASS	0.227259	0.069406	0.015773	8.702979	9.547229	39.562976	40.742699
19	-Input Ibias En +/- 5.0v	uA	PASS	PASS	2.562133	0.199717	0.10748	PASS	0.140739	0.084837	0.01194	7.857105	6.287686	53.252604	47.251395
20	I Offset En +/- 5.0v	nA	PASS	PASS_CP	9.597768	-287.610352	-134.046066	PASS	0.085987	137.264215	11.802909	1.24429	2.64116	18.80762	26.378977
21	Logic Pin Leakage En	uA	PASS	PASS	0.11782	16.788666	16.77924	PASS	1.183372	0.041872	0.049551	38.121024	25.56439	32.150484	21.666407
22	Logic Pin Leakage Dis	uA	PASS	PASS	0.134767	-34.823938	-34.802375	PASS	1.052435	0.10425	0.109716	19.747589	31.411459	18.829226	29.780952
23	Logic Leakage En +/- 2.5v	uA	PASS	PASS	0.083273	16.113314	16.106653	PASS	1.069628	0.041269	0.044143	33.223483	31.392988	31.010479	29.399752
24	Logic Leakage Dis +/- 2.5v	uA	PASS	PASS	0.117621	-33.179077	-33.160258	PASS	1.055753	0.099239	0.104772	22.910821	30.831637	21.760804	29.143582
25	+Psrr Fl +/- 2.5V	uV/V	PASS	PASS	0.17023	-37.184362	-37.107758	PASS	0.926316	0.489277	0.453225	8.730996	21.926458	9.481845	23.614266
26	-Psrr Fl +/- 2.5V	uV/V	PASS	PASS	0.098365	-28.787115	-28.826462	PASS	1.006744	0.473291	0.476483	11.41855	16.752994	11.314529	16.668287
27	+Psrr Fl +/- 5V	uV/V	PASS	PASS	0.151519	-29.31442	-29.253813	PASS	0.854619	0.467139	0.399226	11.192655	17.349878	13.14726	20.250691
28	-Psrr Fl +/- 5V	uV/V	PASS	PASS	0.643521	-20.05222	-20.245276	PASS	0.939105	0.535212	0.50262	9.309572	9.374617	9.785202	10.110531
29	Cmrr Fl +/- 2.5v	uV/V	PASS	PASS	0.349387	-1.667489	-1.597612	PASS	0.838067	1.212283	1.015974	2.291134	3.208131	2.756758	3.805086
30	Cmrr Fl +/- 5v	uV/V	PASS	PASS	0.011193	-0.118894	-0.116655	PASS	0.865261	0.294426	0.254756	11.18685	11.456061	12.931802	13.237076
31	Avol Fl +/- 2.5v Rl=none	uV/V	PASS	PASS	0.110049	91.966435	92.076484	PASS	0.708547	2.087697	1.47923	8.297252	7.669308	11.735042	10.799203
32	Avol Fl +/- 5.0v Rl=none	uV/V	PASS	PASS	0.025781	53.529694	53.542584	PASS	0.845507	0.273899	0.231583	40.80544	20.044267	48.280076	23.688257
33	Pos Vsat Fl +/- 2.5v Rl=none	V	PASS	PASS	0.040173	1.131865	1.131749	PASS	0.620423	6.7068E-4	4.16106E-4	115.238822	28.893556	185.648882	46.664031
34	Neg Vsat Fl +/- 2.5v Rl=none	V	PASS	PASS	0.006717	1.125682	1.125703	PASS	1.074841	3.73308E-4	4.01246E-4	201.515934	66.359606	187.501232	61.722283
35	Pos Vsat Fl +/- 2.5v Rl=1k	V	PASS	PASS	0.065388	1.140795	1.140599	PASS	1.141145	5.16007E-4	5.88839E-4	155.550268	38.245416	136.19963	33.625989
36	Neg Vsat Fl +/- 2.5v Rl=1k	V	PASS	PASS	0.069003	1.134145	1.134359	PASS	1.014403	3.72149E-4	3.77509E-4	209.723427	67.943205	206.934447	66.789605
37	Pos Vsat Fl +/- 2.5v Rl=100	V	PASS	PASS	0.013848	1.208261	1.208205	PASS	0.895254	6.13343E-4	5.49098E-4	167.530212	49.857595	187.097925	55.72465
38	Neg Vsat Fl +/- 2.5v Rl=100	V	PASS	PASS	0.007835	1.20483	1.204862	PASS	1.006959	3.61577E-4	3.64093E-4	281.019494	87.735922	279.106033	87.100879
39	Pos Vsat Fl +/- 5.0v Rl=none	V	PASS	PASS	0.010247	1.162726	1.162829	PASS	0.897099	7.03242E-4	6.30877E-4	314.129214	159.866242	350.215288	178.149424
40	Neg Vsat Fl +/- 5.0v Rl=none	V	PASS	PASS	0.040214	1.15718	1.157313	PASS	0.872465	4.67029E-4	4.07467E-4	183.557823	51.973636	210.49837	59.462439
41	Pos Vsat Fl +/- 5.0v Rl=1k	V	PASS	PASS	0.005349	1.184543	1.184525	PASS	0.815379	7.21195E-4	5.88048E-4	131.514456	25.632074	161.282076	31.446081
42	Neg Vsat Fl +/- 5.0v Rl=1k	V	PASS	PASS	0.016625	1.179945	1.179885	PASS	0.863019	4.97426E-4	4.29288E-4	187.595923	53.646142	217.325252	62.207495
43	Pos Vsat Fl +/- 5.0v Rl=100	V	PASS	PASS	0.00991	1.355792	1.355748	PASS	0.916053	0.001185	0.001085	100.097717	26.504187	109.256956	28.94672
44	Neg Vsat Fl +/- 5.0v Rl=100	V	PASS	PASS	0.061396	1.367174	1.366892	PASS_CP	1.354981	4.58918E-4	6.21825E-4	266.695477	67.423906	196.674555	49.911421

Table 2: Device Status with the board checker program

GENERIC	P-Specs (Fast Loop)	V-Specs	NOTE	Remarks	STATUS
AD817	GTP-00054	V01283	with relay	ECN 141573	Released.
AD8041	GTP-00054	V01183	with relay	ECN 141610	Released.
AD8031	GTP-00054	V01019	with relay	ECN 141613	Released.
AD8099	P-09576	V00281	w/o relay	ECN 141618	Waiting for Release
AD8045	P-09576	V00439	w/o relay	ECN 141617	Waiting for Release
AD829	GTP-00054	V00999	with relay		Done data gathering, for Raise of SECN
AD9632	GTP-00054	V02786	with relay		Done data gathering, for Raise of SECN
AD810	GTP-0054	v01248	with relay		Done data gathering, for Raise of SECN
AD818	GTP-0054	v01216	with relay		For Data Gathering
AD8055	GTP-00055	V01206	with relay		For Data Gathering
AD811	GTP-00055	v01207	with relay		For Data Gathering

3.3 Evaluation Results

An improvement on the performance of checker in each of the DUT available. About 700 devices were returned by the customer that were marked failed by the board checker. In these samples, the researchers took five different devices checked with the new board checker. These samples are ready for production and sent for SECN release. See Table 2. The generated board checker program is good for use in the production line.

4. CONCLUSION AND RECOMMENDATIONS

In this research, a board checker has been developed and implemented for FLC instrumentation amplifier as a solution to detect offset voltages. Two different boards with 10 devices on it were tested. The source QVI for every connected amplifier in each board was checked and determined to generate a command written in C++. The data shows that when an instrumentation amplifier is detached, error is detected and displayed using the program generated. Ten good samples were fed and checked. 10/10 was checked to be in good condition. Before the performing the device test, the functionality of the device or board can be verified using the tester developed.

Additional features can be added for the improvement of test process. One of the sought adjustments for improvement is fanning out the board check across all DIB to make larger scale test of devices.

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