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Broadband and High Efficiency Rectifier Design Based on Dual-mode Operation for RF Ambient Energy Harvesting

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ABSTRACT

This paper presents a novel design approach in the design of a broadband dual mode rectifier with an improved incident power level for wireless power transmission applications. The proposed rectifier makes use of a T-Junction power divider in combination with the two identical rectifiers to provide 2-port and 3-port operational modes. The 2-port operation is obtained by introducing phase matching between the feed line and each rectifier circuits. A harmonic rejection filter (HRF) in the form of low pass filter is designed and placed at the input of the signal source to ensure the rejection of all the harmonics generated from the diodes. By providing such a condition, the generated harmonics are terminated and forced to participate on another cycle of rectification leading to increased efficiency of the overall system. As a result, the proposed rectifier attains a high power conversion efficiency over a broad frequency span of 1.85 to 2.6 GHz under various input power levels. A prototype has been fabricated and tested to validate the design. Measurement results indicate a peak efficiency of 70.3% obtained at 2.3 GHz. Furthermore, a very good power dynamic range of 14 dBm from -8 to 6 dBm is obtained in which the efficiency remains above 40% at all the sampled frequencies. These are in good agreement with the simulation results. The simple, compact and good performance shown over the targeted RF frequencies and power levels makes the proposed rectifier fitting for RF energy harvesting applications.

Key words: Energy harvesting; Microwave rectifier; RF-to-DC conversion; broadband; high efficiency

1. INTRODUCTION

Radio Frequency (RF) Energy harvesting (EH) and Wireless power transfer (WPT) technologies have recently attracted significant attention especially to support the widespread used of low power devices in the Internet-of-Things environment. Microwave rectifiers, are key components in enabling WPT and have extensively been used and studied. Conventional rectifiers generally suffer from narrow band operation and low dynamic power range caused by nonlinearity of the rectifying element [1]. As an alternative, dual band [2] and multi-band [3] rectifiers with complex matching network is employed to increase the harvested energy from multiple source of power. Broadband rectifiers are particularly important for the EH applications due to the wide range of available ambient wireless spectrum and thus higher amount of energy can be harvested leading to a higher DC output power. Furthermore, owing to their wide operational bandwidth, a broadband rectifier can be less sensitive to the input power variation. Broadband rectifiers using a single shunt and single series diode have been presented in [4, 5] and [6], respectively. In an EH application, a single diode rectifier with low loss performance where the level of received RF power is typically low ($P_{RF} \leq 10$ mW) may not suffice to provide the required operating DC voltage to the load integrated circuit (IC).A full-wave rectifier, such as a voltage doubler, may be preferred instead. A broadband rectifier using lump elements presented in [7] had an efficiency better than 70%. Nonetheless, the lossy behaviour of the lumped element at the high frequencies can unfavourably impact the conversion efficiency of the rectifiers. In [8], the authors proposed a broadband rectifier with high efficiency designed at 2.45 GHz demonstrating a high power conversion efficiency of over 70% for a fractional bandwidth of 21.5% based on second-order branch line coupler. However, the employment of the coupler resulted in a significantly large foot print of the overall design which makes it undesirable for many WPT and EH applications. In this paper, a method for the design of a compact and broadband rectifier based on dual mode

switching configuration is proposed, which can effectively enhance the efficiency and input power range of the rectifier, simultaneously. The proposed method takes advantage from 2/3-port operational modes of a 3-port loss less network when combined with a pair of common output rectifiers. The method presented in this paper can be applied on a variety of power, load and frequency based on their applications.

2. MATERIAL AND METHODS

A. Rectifier Principle of Operation

The principle of operation of a voltage doubler is shown inFigure 1. When the injected input signal is at its positive cycle, the series diode (D_2) behaves as a closed switch and conducts the current coming from the positive node of the source (Figure 1(a)). Under this condition the output capacitor (C_2) is charged in which the resultant voltage across the capacitor is a subtraction of input voltage and the diode forward threshold with respect to the ground. Furthermore, the shunt diode (D_1) behaves as a closed switch during the negative cycle and the series diode (D_2) is open, causing the charges to be stored on the input capacitor (C_1) with the same amount of voltage as the output capacitor considering both diodes to be identical (Figure 1(b)). It should be noticed that, the resultant output DC voltage is increased but is not exactly doubled as the input signal needs to overcome the voltage threshold of diodes.

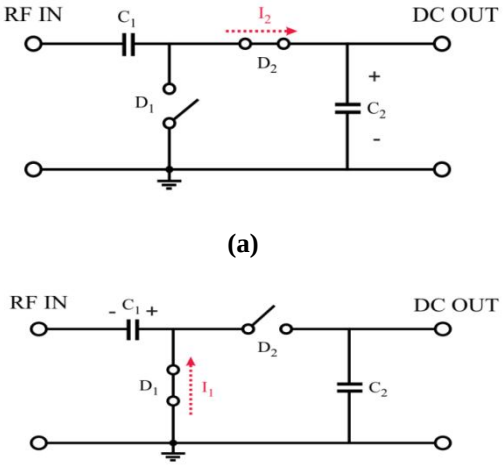

Figure 1: Principle of operation of a voltage doubler at (a) positive cycle, (b) negative cycle

This problem has been significantly reduced by introducing Zero-bias Schottky diodes resulting in an output voltage nearly close to twice the input voltage. The unwanted effects and the cost impact of two single diode can also be minimized by employing two diodes in a single small package such as SOT-323 and SOT-23. There is also another advantage when using voltage doubler in terms of harmonic generation and will be discussed in the next section.

B. Voltage-Doubler/Multiplier Harmonic Analysis

The schematic of a N stage voltage doubler in the form of Dickson charge pump is shown inFigure 2. To begin with the harmonic analysis of the voltage doubler based rectifier it is necessary to have the IV expression of the Schottky diode as

$$I = I_s\left(e^{\gamma v} - 1\right) + C_d \frac{dV_d}{dt} \tag{1}$$

Assuming the input voltage provided by antenna is in the form of $\pm V_0 \cos(\omega_0)$, the voltage across each diode composed of DC and RF components can be written as

$$V_d = V_{RF} + V_{DC} = \pm V_0 \cos(\omega_0) - \frac{V_{Tot}^{DC}}{2N} \tag{2}$$

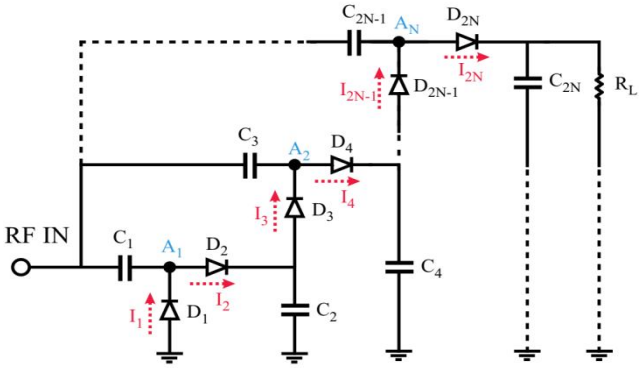

Figure 2: Schematic of a N stage voltage doubler in the form of Dickson charge pump

where V_{Tot}^{DC} presents the total DC voltage provided from N stage cascaded voltage doublers. By casting (1) into (2) it yields

$$I = I_s\left(e^{\frac{\pm V_0 \cos(\omega_0 t) - \frac{V_{Tot}^{DC}}{2N}}{V_T}} - 1\right) \pm C_d V_0 \omega_0 \sin(\omega_0 t) \tag{3}$$

Here, C_d is the diode's junction capacitance and the signs indicate the direction of the current flow. To find the total current at the input of the voltage multiplier, it is sufficient to calculate the current at one node (i.e. A_1) and multiply that by N as

$$I_{RF} = NI_s\left[e^{-\frac{V_{Tot}^{DC}}{2NV_T}}\left(e^{\frac{V_0\cos(\omega_0 t)}{V_T}} - e^{-\frac{V_0\cos(\omega_0 t)}{V_T}}\right)\right] - 2NC_d V_0 \omega_0 \sin(\omega_0 t) \tag{4}$$

By taking the Fourier transform of the periodic signal in(4), the harmonic current generated from a voltage doubler can be written as

$$I = 4NI_s e^{-\frac{V_{Tot}^{DC}}{2NV_T}} \sum_{n=1}^{\infty} J_m\left(\frac{V_0}{V_T}\right)\cos\left(m\omega_0 t\right) - 2NC_d V_0 \omega_0 \sin\left(\omega_0 t\right) \quad (5)$$

In the above equation J_m is the Bessel function of the first kind and order m where $m = 2n-1$. It can be noticed that the odd harmonics are the only existing harmonics in the case of voltage multipliers where the even harmonics are cancelled due to their opposite flow direction. There are also rich information in equation (5)that can be observed by plotting the dominant and harmonic contents of the voltage multiplier as shown inFigure 3(a).

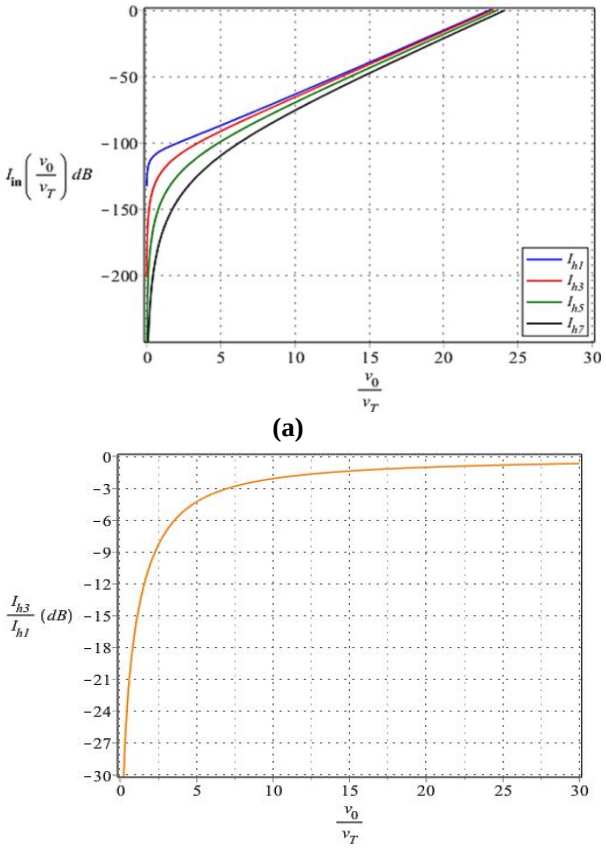

Figure 3: (a) The impact of output voltage on the harmonic current generation of a voltage multiplier. (b) Comparison of the third to the fundamental harmonic currents of a voltage multiplier in a logarithmic scale

As is seen, increasing the output voltage can lead to increment on the harmonic levels where the influence becomes more considerable when $V_0 / V_T > 10$. To better demonstrate this phenomena, a comparison between fundamental and third harmonics in a logarithmic scale is demonstrated in Figure 3(b). It can observed that, when V_0 / V_T reaches to around 7, the third harmonic current is nearly half of fundamental harmonic signifying the importance of odd harmonic terminations for achieving more efficient voltage multiplier.

C. Rectifier Efficiency

The efficiency of a rectifier is calculated as of the ratio between output DC power and accepted RF power by the rectifier as

$$\eta = \frac{\int_0^t P_{DC}\, d\tau}{P_{RF-Acc}\, d\tau} \quad (6)$$

However, for the energy harvesting system the transferred power from the harvester to the rectifier is of paramount importance and the efficiency is calculated as

$$\eta_{EH} = \frac{P_{outDC}}{P_{inEH}} \quad (7)$$

Where P_{inEH} is the total amount of power delivered to the input of the system. The difference between these two equations is that, due to non-linearity of the rectifying element, part of the harvested energy is reflected back to the harvester resulting in a lower amount of power delivered to the rectifying element. Therefore, the maximum efficiency of an energy harvesting system is achieved when the amount of reflected power is minimized. This can be done by properly designing a matching network taking into account the input impedance of the rectifying element, power and load conditions. Hence, it is to be said that the maximum efficiency for an energy harvesting system is obtained when $P_{inEH} = P_{RF-Acc}$.

D. Matching Network

For a rectifier circuit to operate effectively and provide high efficiency rate during the rectification process, the role of a high quality matching network is vital. A well dimensioned matching network can also absorb the parasitic effects of the diodes and allows the efficiency reaches to its extreme. The design of matching network is performed under the harmonic balanced (HB) analysis. HB is a frequency-domain analysis technique developed to take into account distortions in nonlinear circuits and systems. During the analysis, the circuit is divided into linear and nonlinear sub-circuits in which the linear sub-circuit is analyzed similar to any other passive circuits in the frequency domain, while the nonlinear sub-circuit is analyzed differently and in the time domain. Once the results of the time domain analysis are accomplished they are transformed into the frequency domain following the Fourier Transformation. A solution is then found if the currents through the interconnections between the two sub-circuits are the same. The analysis gains its name since, the currents in the linear and nonlinear sub-circuits through these interconnections have to be balanced at every harmonic. The HB analysis is usually performed in any compatible software such as ADS.

E. Filter Considerations

Harmonic generation of the rectifying component can be a huge source of loss as each harmonic component carries a fraction of injected power that has not converted into DC form. The employment of low pass/ band pass filter at the input can suppress the harmonics and re-inject them back to participate into another rectification cycle. Furthermore, in some cases, these harmonics can be detrimental to the consumer device particularly at the higher power levels. Hence, a low pass filter, typically made from quarter wave-length stub resonators, is used to terminate any outgoing harmonics and protect the consumer device.

F. Diode Selection

The choice of diode plays an important role on the performance of the rectifier and needs to be chosen based on requirements of the intended application. For the energy harvesting systems a diode with low built-in voltage is preferred as the available power to run the circuit is inherently low. Moreover, the efficiency of a diode is tightly related to the series resistance R_s and junction non-linear capacitance C_{j0}. While the series resistance R_s is a linear component and increases the ohmic loss on the diode, the junction capacitance C_{j0} contributes to the generation of the harmonic currents and its influence becomes more significant as the frequency increases.

Basically, diodes in the smaller package can considerably reduce the junction capacitance since its value is directly related to the wafer area. The breakdown voltage V_{br} is also another important factor as it determines the power handling capability of the diode. Ideally, a diode with high breakdown voltage, low junction capacitance and low series resistance is desirable. However, due to physical trade-offs and manufacturing constrains such diode is not feasible. The HSMS28XX family of zero-bias Schottky diodes from BROADCOM technology are attractive candidates as they do not required any external bias voltage and are capable of operating at microwave frequencies with a very low turn-on power. Although HSMS282X is the most recommended diode for the operation around 2 GHz, but the built-in voltage is relatively high (350 mV) which is not the best choice when available power is extremely low.

On the other hand, HSMS285X and HSMS286X possess a built-in voltage of 150 mV and 250 mV, respectively, which makes them more suitable for our application. A comparison between HSMS285X and HSMS286X reveals that, while HSMS285X has the lowest built-in voltage, but the series resistance and break down voltage are 25 Ω and V_{br} = 3.8 V. On the contrary, the HSMS286X possesses a much lower series resistance of 6 Ω and the break down voltage of V_{br} = 7 V which is almost double to that of HSMS285X. A complete comparison between different parameters of the aforementioned diodes are given inTable I. Since the focus of this work is on the energy harvesting application at the low power levels the diode model HSMS285C with the lowest available built-in voltage (V_f = 150 mV) in the HSMS-28XX family is chosen and will be considered here.

The general configuration of the proposed rectifier is given in Figure 4. The basic configuration of a rectifier is composed of a DC-block filter (C_1), with a matching network for maximum power transfer to the rectification circuit, rectifying elements in the form of voltage doubler, DC pass filter (C_2) and an output load (resistor).

Table I: Comparison Of Typical Schottky Diode Values from HSMS-28XX Family

Diode Type	**HSMS-281X**	**HSMS-282X**	**HSMS-285X**	**HSMS-286X**
I_{BV} (A)	1.00E-04	1.00E-03	1.00E-03	1.00E-04
C_{j0} (pF)	1.1	0.7	0.18	0.18
B_v (V)	25	15	3.8	7
E_G (eV)	0.69	0.69	0.69	0.69
V_j (V)	0.65	0.65	0.35	0.65
N	1.08	1.08	1.06	1.08
V_f (mV)	400 (I_f = 1 mA) 1000 (I_f = 35 mA)	340 (I_f = 1 mA) 500 (I_f = 10 mA) 700 mV (I_f = 30 mA)	150 (I_f = 0.1 mA) 250 (I_f = 1 mA)	350 (I_f = 1mA) 600 (I_f = 30 mA)
X_{TI}	2	2	2	2
I_s (A)	4.8E-09	2.20E-08	3.00E-06	5.00E-08
R_s (Ω)	10	6	25	5
V_j (V)	0.65	0.65	0.35	0.65
M	0.5	0.5	0.5	0.5

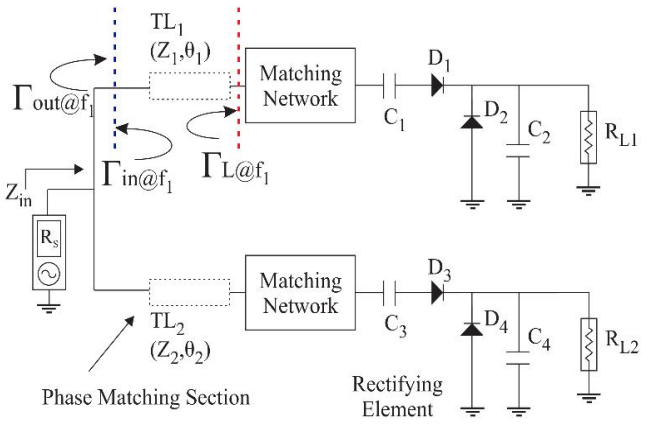

Figure 4: An illustration of the proposed rectifier

A lossless T-junction power divider is employed to feed the two rectifiers matched to their respective input transmission line impedances at the targeted frequency f_0 and input power level. The frequency dependent characteristic of the feeding T-junction is vanished by eliminating commonly used quarter-wavelength transformers which also results in more compact size of the overall rectifier. Hence, under the same power condition, the entire matching network and the rectifier can be treated as a resonant load at the frequencies f_1 and f_2 where the magnitude of Γ_{out} equates Γ_{in} with an arbitrary phase value θ. The required electrical length to achieve phase matching for a single branch of the power is then determined as

$$Z_{in} = Z_1 \left(\frac{1 - \left|\Gamma_{L\_f1}\right| e^{-2j\theta_l}}{1 + \left|\Gamma_{L\_f1}\right| e^{-2j\theta_l}} \right) \tag{8}$$

where Z_1 , is the characteristic impedance of the transmission line and θ_1 is the electrical length of the line at the frequency of f_1 . Here, Γ_{L_f1} is the reflection coefficient of the complex load at the input of the matching network and defined as

$$\Gamma_{L\_f1} = \frac{Z_{L\_f1} - Z_1}{Z_{L\_f1} + Z_1} \tag{9}$$

where Z_{L_f1} is the complex load value at frequency of f_1. After some mathematical simplification, the required electrical length for the phase matching can be found as

$$t = \frac{X_L Z_1}{R_L^2 + X_L^2 - \frac{R_L Z_1}{\alpha}} \tag{10}$$

While the same procedure can be applied on the second branch, it is pertinent to observe that the maximum power transfer to each rectifier is achieved only if the energy conservation requirements of a 3-port loss less network is satisfied simultaneously. Therefore, by assigning each output branch to be matched at frequencies f_1 and f_2, respectively, one rectifier remains operational while the other one experiences large mismatch at the exact same frequency and power level, resembling 2-port matching condition of a 3-port network.

3. RESULTS AND DISCUSSION

The proposed rectifier as described in the previous section is targeted to operate within the 2GHz to 3GHz range using commercial Schottky diode HSMS-285C from BROADCOM with built-in voltage of V_f = 150 mV, breakdown voltage V_{br} = 3.8 V, series resistance R_s = 25 Ω, and a junction capacitance of C_{j0} = 0.18pF. The co-simulation using the harmonic balance analysis is performed to precisely predict the rectifier behaviour in Advanced Design System (ADS). A harmonic rejection filter in the form of low pass filter is also designed and placed at the input of proposed rectifier to prevent the reradiation of harmonic contents which can effectively improve the overall PCE.

Figure **5** shows the configuration of the broadband rectifier. The parameter values of the proposed design are: l_1 = 3.4 mm, l_2 = 7.3 mm, l_3 = 5.74 mm, l_4 = 7.3 mm, l_5 = 8.9 mm, W_1 = 0.5 mm, W_f = 1.18 mm, l_s = 9.5 mm, W_{R2} = 0.3 mm, W_{R3} = 2.8 mm. The length of the short and long arms are calculated from equation (10) and are found to be 11.7 ° and 102 °, respectively. The diameter of all via holes are 0.8 mm. The 3-dimensional (3D) view of the S_{11} versus both frequency and input incident power under the large signal condition is illustrated in Figure 6..

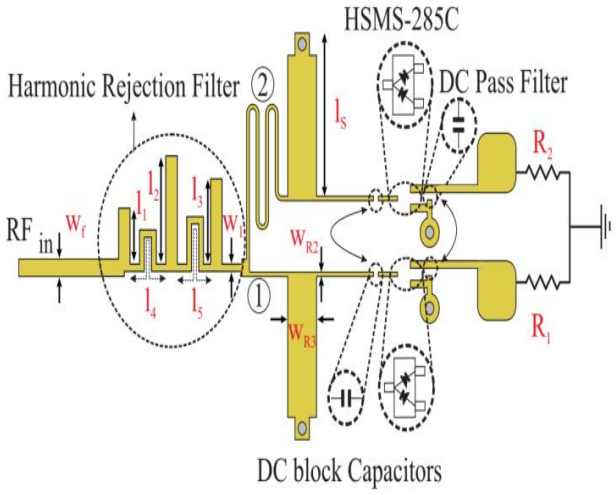

Figure 5: Layout of the broadband dual output rectifier

The rectifier is then fabricated on a RO4003C material that has a relative permittivity of 3.39, loss tangent of 0.0027 and thickness of 20 mil. A photograph of the fabricated rectifier prototype is depicted in
Figure **7**.

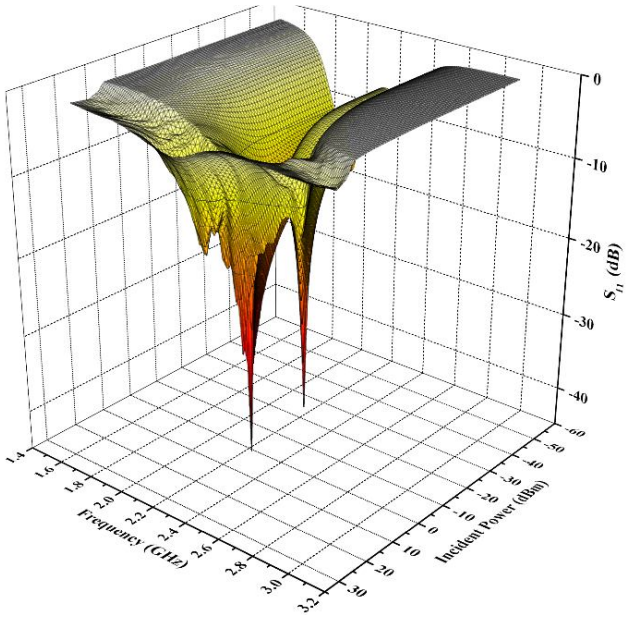

Figure 6: Simulated 3-D view of the return loss versus frequency and power level

The overall dimensions of the proposed rectifier is 0.38 λ_0 × 0.25 λ_0 , where λ_0 is the free space wavelength at the required frequency. The return loss is verified using a vector network analyser (VNA) and the results are provided in Figure 8 for three different input power values, i.e. 3,-7 and -17 dBm. The variation on the rectifier return loss response comes from the impact of junction capacitance which imposes change on the input impedance of the diodes as the power varies.

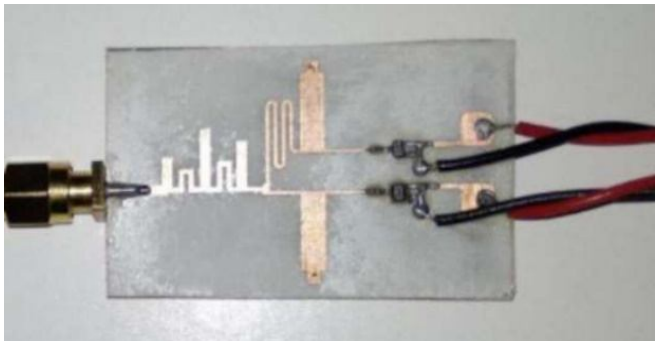

Figure 7: Photograph of the fabricated broadband rectifier

The rectifier conversion efficiency is evaluated by

$$\eta(\%) = \frac{P_{DC1} + P_{DC2}}{P_{in}} \times 100 = \frac{{V_{out1}}^2 + {V_{out1}}^2}{R_L P_{in}} \times 100 \quad (11)$$

where V_{out1} and V_{out2} are the output DC voltage measured across the output resistors R_{L1} and R_{L2} ,respectively, and P_{in} is the incident RF power.

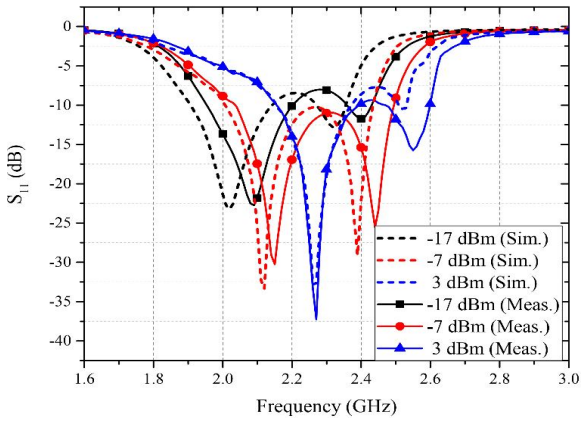

Figure 8: Return loss verification using a VNA

Figure **9** provides the measured and simulated power conversion efficiency for three different input power values of 3, -7 and -17 dBm, respectively.

As is observed, good efficiency over wide range of frequency (1.9 to 2.6 GHz) has been achieved. The highest measured efficiency is 70.3% obtained at 2.3 GHz. The efficiency drops lower input power values. However, even at -17 dBm, an efficiency better than 10% from 1.85 to 2.5 GHz is obtained. The measured efficiency along with the simulated results as a function of input incident power at different frequency of 2, 2.15, 2.3 and 2.45 GHz are shown in
Figure **10**. There is an overall good agreement.

In comparing the measured and simulated results, the efficiency from the simulation is observed to be slightly better than the measured ones. The slight variance between them is mainly related to the imprecision of modelled diode, connector losses as well as the fabrication tolerances. However, a very good power dynamic range of 14 dBm from -8 to 6 dBm is obtained in which the efficiency remains above 40% for all sampled frequencies.

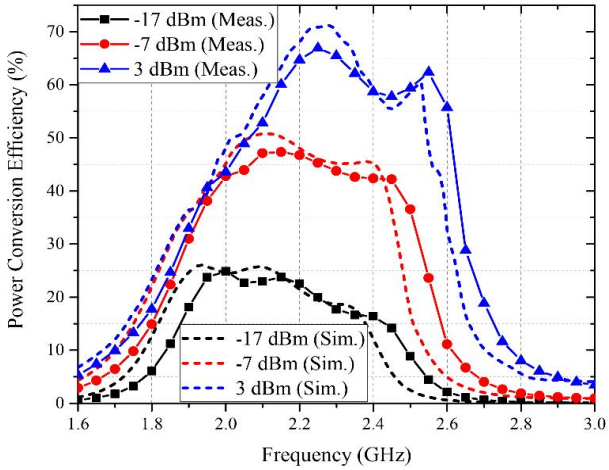

Figure 9: Power conversion efficiency at various frequencies for three power levels of 3, -7 and -17 dBm

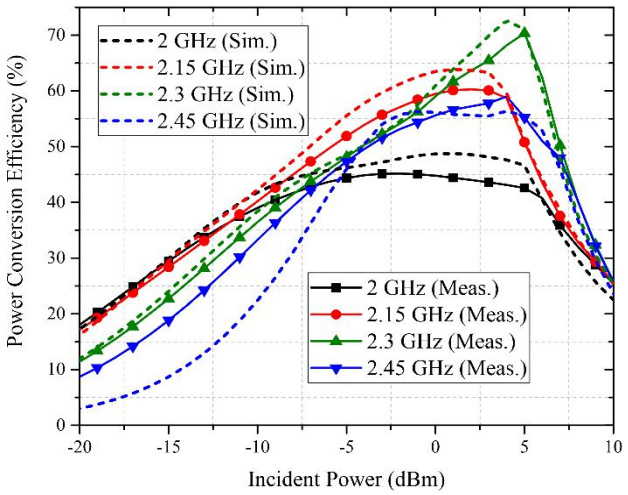

Figure 10: Power conversion efficiency under various incident power levels over several frequencies

4. CONCLUSIONS

A novel method for the design of a compact and broadband rectifier based on dual mode switching configuration is presented, which can effectively enhance the efficiency and input power range of the rectifier, simultaneously. The proposed method takes advantage from 2/3-port operational modes of a 3-port loss less network when combined with a pair of common output rectifiers. The empirical results agree well with theoretical verifying the validity of the proposed design approach. good efficiency over wide range of frequency (1.9 to 2.6 GHz) has been achieved. The highest measured efficiency is 70.3% obtained at 2.3 GHz. The efficiency drops lower input power values. Simplicity, compactness as well as high efficient performance over a wideband of commercial RF frequencies, i.e. 2-3GHz makes the designed rectifier desirable to be a good candidate for the WPT and EH applications.

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