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Design of Reconfigurable Low Power Pipelined ADC for Bio-Impedance Measurement

Hari Kishore Kakarla, **Mukil Alagirisamy**
Postdoctoral Research Fellow in Electronics and Communication Engineering,
Lincoln University College, Petaling Jaya, Selangor, Malaysia
Senior Lecturer, Faculty of Engineering, Lincoln University College, Petaling Jaya, Selangor, Malaysia
kakarla.harikishore@gmail.com

ABSTRACT
In this brief, a reconfigurable pipelined ADC is equipped to calculate the ultra-low-power bio-impedance using FinFET transistors working in a region of weak inversion. The proposed structure consists of an auto adaptation unit which differentiates bio-signal with high frequency from that of the bio-signal having a very low frequency and builds the proposed reconfigurable Pipelined ADC to work in correct operating approach. Moreover, the proposed converter is well capable of reconfiguring itself into three modes of operation depending on the provided input signal. The designed adaptation unit here has two control bits so that either 8-bit or 12-bit resolution with a 10KS/s or 1GS/s sampling rate can be chosen. The power dissipation with a supply voltage of 1 V along the adaptation unit for 8-bit and 12-bit pipelined ADC is 114.70 µW and 144.70 µW respectively. For a proposed pipelined ADC, the corresponding values of SNR, SINAD, and SFDR are stable with a minimum value of 70.95db, 70.94DB and 75.51db respectively. The total work is carried out by using FinFET 18nm Technology.

Keywords: Adaptation Unit, Pipelined ADC, FinFET

1. INTRODUCTION

Biological material's electrical impedance, typically referred to as bio-impedance, is an important measurement of physiological processes and thus offers vital monitoring possibilities for a variety of biomarkers. More than a century ago the prospective use in medical applications was already developed [1]. Research on bio-impedance is still an increasing area of study, and its advancements are extensively used in many medical applications. The characterization of bio-impedance is as the EIT principle [2]. It is widely used in applications such as regulation of the pulmonary system, detection of breast cancer, prediction of cervical intraepithelial neoplasm's etc. Bio-impedance is also effectively applied to sense various types of cancers [3]. In addition, bio-impedance measurements are used to eliminate artifacts as part of additional instruments in other forms of measurement, such as ECG [4]-[6].In such applications, bio-impedance is usually extracted on a single frequency. Additionally, newly developed surgical instruments that act on measures of bio-impedance [7]. Various other uses include fluid analysis in the human body and classification of cells different for implantable and wearable healthcare applications [8], [9], interactive bimolecular impedance sensing [10], [11]. Implantable devices capable of impedance conduction also test tissue bio-impedance under the skin; however implantable sensors [12] have strict scale, strength, and communication limitations that essentially determine the function of the sensor. The size of the implantable device should be minimum for both practical and medical purposes, so that the miniaturization of the instrument is of paramount importance [13]. The availability of electric energy is another big problem for the implantable system. The use of batteries is strongly discouraged as they have a short life cycle and thus have a significant effect on the form factor. Energy harvesting techniques such as inductive coupling is preferred as power transfer, and wireless communication can be accomplished simultaneously [14]-[16]. Nonetheless, inductive harvesters are capable of collecting only small amounts of power at large distances (low efficiency); thus, the development of implantable electronic circuits must be performed using ultra-low power design techniques. Typically, biomedical monitoring systems which track specific physiological parameters cannot assume specified amplitude or frequency signals, since the signal properties can differ significantly across separate and identical bio-signals; Furthermore, advances in biomedical science have resulted in informative bio-signal monitoring schemes that make it possible to obtain continuous vital patient details. Implantable devices are required for the recording, analysis and transmission of this critical information using limited area and energy. Consequently, every ADC intended for these systems must also meet these restrictions. For bio-sensing applications, reconfigurable ADCs are ideal, as they can respond to a broad variety of signals. Conversely, most reconfigurable Analog to Digital Converter (ADC) implementations lack an automated reconfiguration scheme that enables the user to manually reconfigure the device. The popular ADCs developed for the implementation of biomedical applications are in the form of SAR ADCs, because of low small area, medium resolution and low power characteristics that are mostly attractive for the implementation of bio-sensing applications. Another form of bio-signal monitoring, idea bio-impedance measurement has recently gained interest in medical science because there are many possibilities for health tracking [17], [18]. Studies using bio-impedance have been reported for example to track breast cancer cells. Bio-impedance measurements are taken in order to obtain reliable, functional data from lower to higher frequencies, since the resistance and reactivity measured vary in frequency. The ADC pipeline introduced in this brief solves the problem and is able to use a limited amount of power to process conventional bio signal without the use of sub-threshold bias. Implementation of the adaptation unit, which

decides the optimum operating mode for the type of input data. The paper is further organized as follows. In section 2, the methodology implemented in this work is discussed. In the section 3 proposed systems is discussed followed by results and conclusion in section 4 and 5 respectively.

2. METHODOLOGY

The following section discusses the details of the methodology which will be used to implement the proposed technique. The flow chart in Fig.1 shows the method employed in the reconfigurable ADCs to construct the adaptive structure. The intended circuit is implemented with a supply voltage of 0.8V in 18nm Fin FET technology. Firstly, the required specifications for the design are specified. Secondly, the required technology is selected. Based on the selected technology and designing techniques the size of the transistors is derived as well as supply voltage is chosen depending on stacking of transistors. Later, the based on the various existing topologies, a new topology of the proposed circuits is designed and simulated for required parameters. If the derived parameters are meeting the specifications, then the designed topology can be implemented otherwise the proposed topology of the circuits must be changed until the simulated parameters meet the required specifications.

3. SYSTEM ARCHITECTURE

In order to calculate the bio-impedance, a non-harmful current pulse is injected into the patient at the target area, and the voltage decrease is determined. For reliable, useful information to get, the frequency ranges of the current injected ranges from approximately 10 Hz to 10 MHz [19]. The measurements of low frequency signals are almost completely exempt, because the injected current signal cannot move through the capacitance of the cell membrane. Moreover, the injected pulse signal frequency rises above a range of hundred

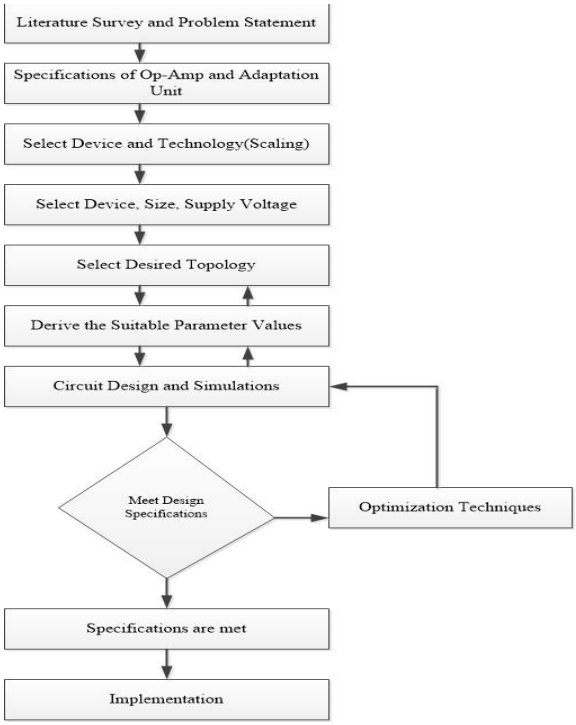

Figure 1: Flow Chart of the Methodology

Kilohertz, the impedance of the intracellular membrane is measured as the signal voltage crosses the capacitance of the cell membrane. In addition, the ADC is accountable for digitizing these data and it should be able to handle this range of frequencies effectively while occupying a less area and utilizing sufficient power for implantable electronic applications. Figure 2 provides a block diagram for the proposed structure. Then the input signal is forwarded directly to the A/D converter after the adaptation unit. Afterwards, the two control bits provided by the adaptation unit are used to determine the converter's sampling rate and resolution. The two blocks are further described in the sections below.

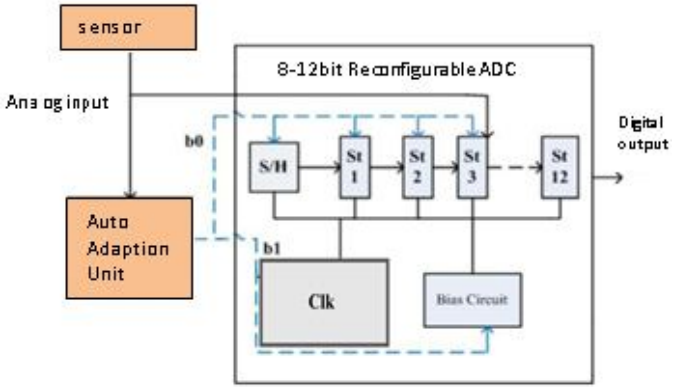

Figure 2: Proposed Block diagram of the system

3.1 Reconfigurable Low Power Pipelined ADC

The proposed reconfigurable system uses a typical ADC design to achieve 1bits/stage. The sample-and - hold stage (S/H) circuit has a maximum 12bit resolution. The use of digital correction circuit improves the accuracy of the proposed system. In terms of speed and resolution the converter can be reconfigured. To achieve substantial power savings, the lower complex method of disconnecting the final stages of the pipeline is used by disconnecting the S/H stage, as well as the two first stages of the pipeline. Since the stage 3 of the pipeline ADC receives single residue from the previous stages, the third stage needs no more pair of input signals apart from the original input with the requirement of an extra circuitry. Due to this, the question of leakage current from the off signal terminal combines with the correct signal. In order to overcome this problem of interference, the impact of the Op-amps with high CMRR is used. This problem of interference is eliminated by converting the leakage signal to a Common mode signal of the op-amp terminals; and thus the leakage signal problem can be ignored.

3.2Operation of Transistor

The problem with traditional MOSFETs is that of increasingly smaller and smaller sensors. We face serious problems, including reduction of drain-induced barriers (DIBL), increased current of leakage, etc. One problem solving contributes to another. Some MOSFETs have been added to solve the problem, including FinFET, Double Gate, Tri-gate, and so on. Figure 3 shows Fin FET's general schematics.

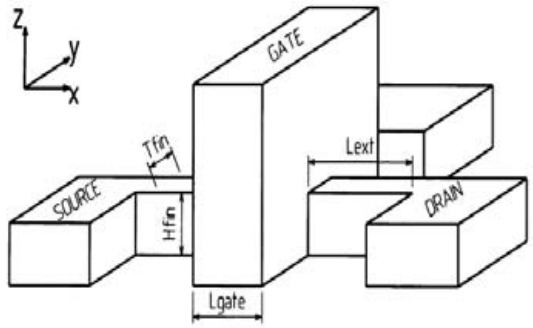

Figure 3: General Schematic of Fin FET architecture [20]

To function correctly from this point of view, understanding the features of MOSFET is of paramount importance. FinFET operates in the three areas which follow.

Linear Area: This is the sector where the Ids are increased linearly with Vds voltage, the Ids current is given in the linear region for a given voltage of Vg > Vth as the first approximation is,

$$I_{ds} = \frac{2\mu WC_{OX}}{L}\left\{V_g - V_{th} - \frac{V_{ds}}{2}\right\}V_{ds} \text{.....1}$$

Where V_{th} is the threshold voltage in the inversion region known as carrier mobility, i.e. the tube, W / L is the ratio of the interface width to length, C_{ox} is the capacitance of the gate oxide per unit field,

Saturation region: Ids in this area are constant, and Vds are on the rise. Again Ids are given in the saturation region for the first rough calculation.

$$I_{ds} = \frac{\mu WC_{OX}}{L}\left\{\frac{V_g - V_t}{2m}\right\}^2, \text{ m=1+3(tox/xd) .....2}$$

d is the thickness of the corrosion layer and t_{ox} is the thickness of the oxide which means that the current of the I_{ds} does not depend on the voltage of V_{ds}.

Cut-Off Region: $V_g < V_{th}$ in this region, so that there is no channel between source and drain resulting in the current Ids=0. The current flux of the sub-threshold is in fact the exponential current of decay for $V_g < V_{th}$.

High concentrations of electrons induce a high level of electric field along the channel, and the sub-threshold current is primarily due to the conductor's diffusion.

$$I_{ds} = \frac{\mu W}{L} KTKT\acute{n}itsie^{q}\frac{(V_g - \Delta\phi)(1 - e^{q(V_{ds})}}{KT} \text{.....3}$$

Where ΔΔ is the difference between the function of the gate electrode and the almost intruded silicone skin.

3.3Auto Adaptation Unit

A simple adaptation unit is added to reconfigure the proposed ADC in proper operating mode. Figure 4 shows the adaptive unit circuit. The input signal to the adaptation unit is then amplified and then the Schmitt circuit with lower and upper threshold voltages of 530mV and 1.38V is transformed into a square wave for the given signal. The FVC converter then converts the square wave frequency which is generated by the Schmitt trigger to a DC voltage. Two comparators with varying reference voltages have two control bits for this voltage. At present every block is geared towards a stable operation.

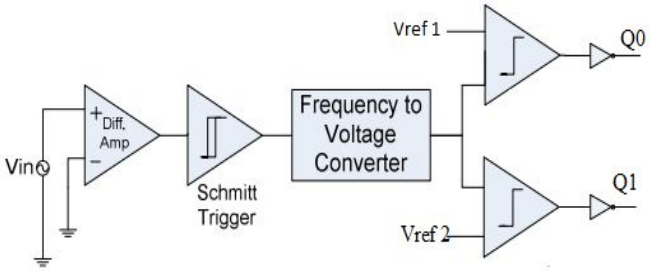

Figure 4: Circuit for Auto Adaption Unit

3.4 Circuit for the Conversion of Frequency to Voltage Converter (FVC)

Frequency to voltage converters are highly flexible electronic building blocks which are commonly used in many applications for frequency conversion. It is the principal factor that defines the adaptation mechanism's functioning. For input frequency values it generates output voltages. During the current work [21, 22], the concept model was previously built for different applications. It includes IBIAS current, several transistors, two different capacitors (C1 = C2 = C), a logical core that activates capacitors for loading and unloading. The logic block functions shall be generated in 2 short V1 and V2 pulses at the same frequency as the input signal. The pulse length is set to 2ns.These bursts are used to monitor loading and unloading of the capacitor. The input signal for the Mp1 and Mn1 transistors was explicitly operated by the FVC. MP1 is activated and if the signal strength is weak MN1 is disabled. The MN2, MN3, and MN4 transistors are blocked by V1 and V2 signals. During this time, the output will be charged to C1.Mn1 transistors are not very important, but can only increase circuit performance. It ensures that the voltage of the joint node is kept low when the input voltage is high, so that the C1 capacitor is charged at a very high voltage when the input signal is shifted from high up to low. Avoid voltage errors that may occur when not disabling the Mp1 transistor.

When a good input signal for Mp1 is received, MN1 reacts further. The load at C1 is proportional to the input signal's pulse width. As soon as the signal goes out, High C1 starts charging. Alternatively, the V1 pulse signal flips Mn3 to allow the C1 and C2 circuits to be very fast (usually 2ns) over an extremely short time. The charge is broken down between C1 and C2 during this process. The C1 and the C2 are divided when the V1 pulse is small, and the load time is over. The rest of the circuit is divided up from C2. For the next half of the input pulse width the load is maintained by C2. If V1's pulse falls, V2 is big, which triggers Mn2, and Mn2 provides a

discharging path for the C1. Figure 5 shows the Frequency to Voltage Converter circuit diagram.

Mn2's diameter is larger than most transistors to quickly discharge C1. It helps to release C1 at high frequencies quickly. The cycle proceeds for the next half of the input pulse range, and C2 remains constant for a given amount of time, while the input signal remains unchanged. The capacitor charge shall be regulated as

$$i = C\left(\frac{dV}{dt}\right) \quad \text{.....4}$$

C is the capacitance value, and dv/dt is the voltage shift level over the condenser w.r.t. time when the charging current is through the condenser power. If the condenser is saturated at half the pulse width (T/2), then.

$$V_{out} = \frac{i}{2}\left(\frac{T}{c}\right) \quad \text{.....5}$$

That implies the output is directly or inversely proportional to the frequency of the input signal. It implies that the output tests the input frequency and decides that the frequency is constant at a defined voltage because the accuracy of Vdd and Vss is low; it is recommended to carefully select IBIAS and C values.

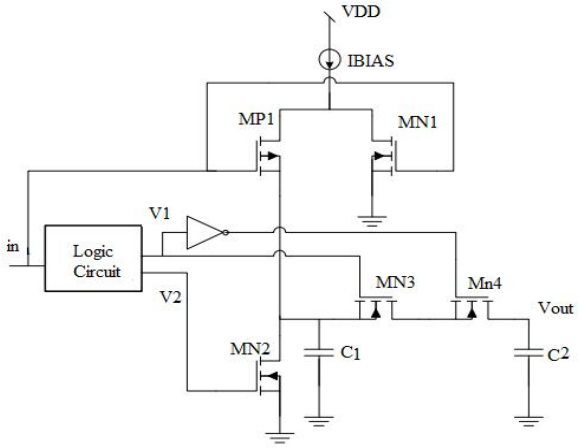

Figure 5: Frequency-to-Voltage Converter

The value of IC is deliberately selected higher than that of the previous model in order to avoid resettling the production of FVC at a pace somewhat close to the source of Vs. This will aid in later research. Performance (Vout) may be given over several cycles, for instance:

$$V_{out} = \frac{1}{2}(VC) + \left(\frac{1}{2^2}\right) + \ldots\ldots \frac{1}{2^N}(VC) \quad \text{.....6}$$

If N is the number of cycles in the input signal. Production is calculated from simulation tests in around 6 T to 9 T states where T is the input signal length.

The IBIAS charging current, the C1 capacitor, can be set to the FVC operating frequency range minimum (Fmin) and peak (Fmax) limits and to the full output voltage values.

$$F_{min} = \frac{1}{2C}\left[\frac{1}{V_{max}}\right] \quad \text{.....7}$$

$$F_{max} = \frac{1}{2C}\left[\frac{1}{V_{min}}\right] \quad \text{.....8}$$

The total available frequency of the circuit shall be determined by

$$F_{max} \leq \frac{1}{2(r_1 + r_2)} \quad \text{.....9}$$

This system operates up to 100MHz, where the pulse widths V1 and V2 are t1 and t2. In the logic block the pulse longitudinal time has to be set to t1 = t2=2ns.

4 RESULTS AND DISCUSSIONS

This finding of this research work are included in this section, where their effects are discussed, as well as the use of the 18 nm Fin-FET technology for circuit implementation. With a supply voltage of 1V this complete op-amp can be run. The results of simulation for the adaptation unit are displayed in Figure 6 with an input signal of 5 kHz, for this case of 5kHz, the frequency-to-voltage DC voltage produced by the converter takes around about a time 4ms to charge up to the final output value of 1 V, which is elevated value when compared with the reference voltages of the two comparators. The control bits produced are therefore '00' which configures the ADC in low resolution, low sampling rate mode.

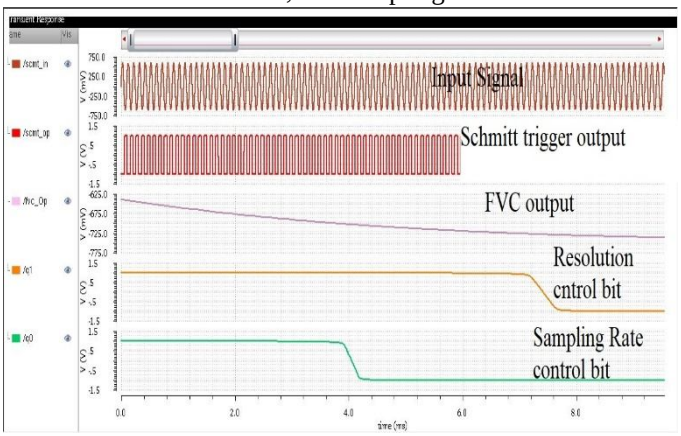

Figure 6: Simulation Results in Auto Adaptation Unit

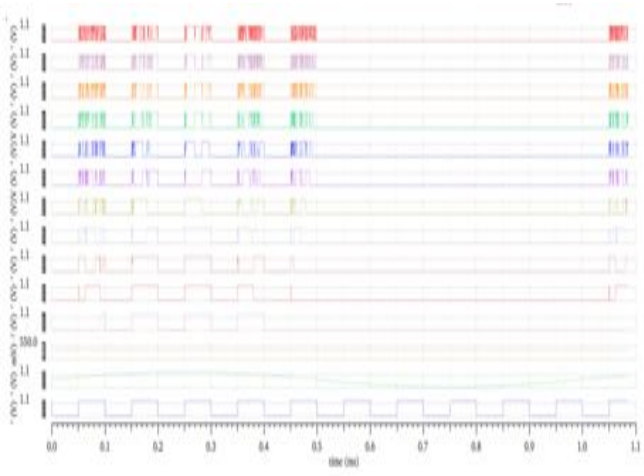

Figure 7: Simulation result of 12-bit pipelined ADC

The transient simulation result of 12-bit, 1-bit and 8-bit reconfigurable pipelined ADC is plotted in the Figures 7, 8 and 9 respectively. The dynamic performance characteristics of the proposed Pipelined ADC are demonstrated in Figures 10, 11 and 12. The corresponding values of SNR, SINAD, and SFDR are stable with a minimum value of 70.95db, 70.94DB and 75.51db respectively. The table I displays the different values for the Reconfigurable Pipelined ADC parameters. It is evident from the table that the reconfigurable ADC has a sampling rate of 10KS / s to 1GS / s, with a resolution of 8 to 12 bits. It will also dissipate for an 8-bit ADC power of 114.70uW, and for a 12-bit ADC power of 144.70uW.

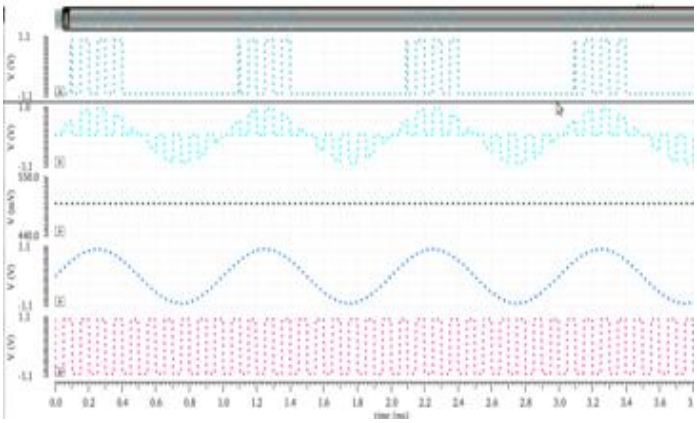

Figure 8: Simulation result of 1-bit pipelined ADC

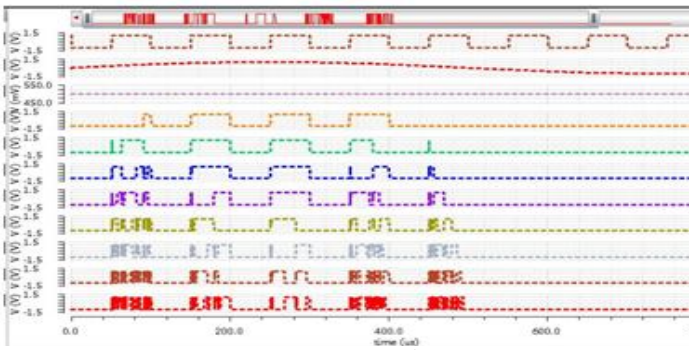

Figure 9: Simulation Result of 8-bit Output

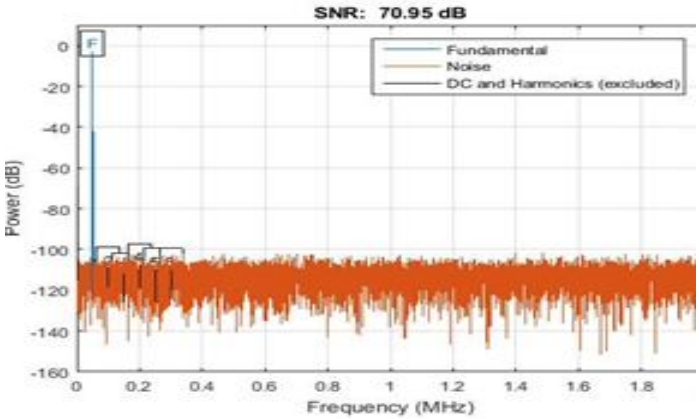

Figure 10: Dynamic Characteristics of ADC showing SNR value

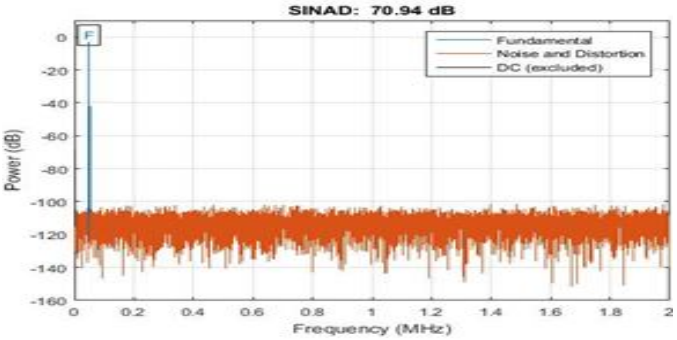

Figure 11: Dynamic Characteristics of ADC showing SINAD value

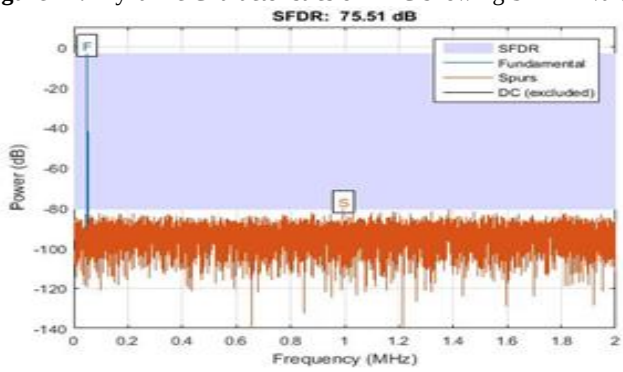

Figure 12: Dynamic Characteristics of ADC showing SFDR value

Table 1: Various parameters of Reconfigurable ADC

Parameter	Work
Technology	FinFET18nm
Supply voltage	1V
Sampling rate	10ks/s – 1Gs/s
Resolution	8/12
Power	114.70/144.70uW
SINAD (dB)	70.94/69.06
SFDR (dB)	75.5.2/74.85
SNR (dB)	70.95/69.01

5 CONCLUSION

The ultra-low power reconfiguration is provided with an analog to digital converter. By operating the transistors to work in the weak inversion region and the ADC is configured for better resolution and sampling rate and low power. The proposed ADC requires an adaptation unit to be reconfigured based on the input signal itself, which is combined with the reconfigurable ADC. The power consumed by the adaptation unit is of lesser concern since it enables a biosensor device to detect a wide range of physiological parameters like measurements of bio-impedance.

REFERENCES

1. S. Grimness and O. G. Martinsen, Bioimpedance and Bioelectricity Basics, 3rd ed. New York, NY, USA: Academic, 2015.
2. D. S. Holder, Electrical Impedance Tomography: Methods, History and Applications. Boca Raton, FL, USA: CRC Press, 2005.
3. P. Aberg, I. Nicander, J. Hansson, P. Geladi, U. Holmgren, and S.Ollmar, "Skin cancer identification using multifrequency electrical impedance–A potential screening tool," IEEE Trans. Biomed. Eng., vol. 51, no. 12, pp. 2097–2102, Dec. 2004.
4. A. Adler and A. Boyle, "Electrical impedance tomography: Tissue properties to image measures," IEEE Trans. Biomed. Eng., vol. 64, no. 11,pp. 2494–2504, Nov. 2017. https://doi.org/10.1109/TBME.2017.2728323
5. Mohammad Takhti and Kofi Odame, Senior Member, IEEE, "A Power Adaptive, 1.22-pW/Hz, 10-MHz Read-Out Front-End for Bio-Impedance Measurement:, IEEE Transactions on Biomedical Circuits And Systems, Vol. 13, No. 4, Pp. 725-734, August 2019.
6. H. Kim, S. Kim, N. Van Helleputte, A. Artes, M. Konijnenburg, J.Huisken, C. Van Hoof, and R. F. Yazicioglu, "A configurable and low power mixed signal SoC for portable ECG monitoring applications,"IEEE Trans. Biomed. Circuits Syst., vol. 8, no. 2, pp. 257–267, Apr.2014.
7. N. Van Helleputte, M. Konijnenburg, J. Pettine, D.-W. Jee, H. Kim, A.Morgado, R. Van Wegberg, T. Torfs, R. Mohan, A. Breeschoten, H. deGroot, C. Van Hoof, and R. F. Yazicioglu, "A 345 multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact Reduction, and integrated DSP," IEEE J. Solid-State Circuits, vol. 50,no. 1, pp. 230–244, 2015. https://doi.org/10.1109/JSSC.2014.2359962
8. G. Qiao et al., "Bioimpedance analysis for the characterization of breast cancer cells in suspension," IEEE Trans. Biomed. Eng., vol. 59, 2012.
9. Lukas Kull, Danny Luu, Thomas toifl,"A 12-bit 300-MS/s SAR ADC With Inverter-Based Preamplifier and Common-Mode-Regulation DAC in 14-nm CMOS FinFET" IEEE International Solid State circuits, 2018.
10. Ewout Martens, Benjamin Hershberg, Jan Craninckx, "A 69-dB SNDR 300-MS/s Two-Time Interleaved Pipelined SAR ADC in 16-nm CMOS FinFET With Capacitive Reference Stabilization ", IEEE international Solid State circuits, 2018.
11. A. Yúfera, A. Rueda, and J. Munoz, "A tissue impedance measurement chip for myocardial ischemia detection," IEEE Trans. Circuits Syst. I,Reg. Papers, vol. 52, no. 12, pp. 2620–2628, 2005.
12. M. Crescentini, M. Bennati, and M. Tartagni, "A high resolution interface for Kelvin impedance sensing," IEEE J. Solid-State Circuits, vol.49, no. 10, pp. 2199–2212, Oct. 2014. https://doi.org/10.1109/JSSC.2014.2346768
13. W. H. Ko, "Early history and challenges of implantable electronics,"ACM J .Emerg. Tech. Com., vol. 8, no. 2, p. 8, Jun. 2012.
14. S. Lee, S. Polito, C. Agell, S. Mitra, R. FiratYazicioglu, J. Riistama,J. Habetha, and J. Penders, "A low-power and compact-sized wearable bio-impedance monitor with wireless connectivity," in Proc. J. Phys.Conf. Ser., Apr. 2013, vol. 434, pp. 1-4.
15. M. Zargham and P. G. Gulak, "Fully integrated on-chip coil in 0.13CMOS for wireless power transfer through biological media," IEEE Trans. Biomed. Circuits Syst., vol. 9, no. 2, pp. 259–271, Apr. 2015.
16. B. I. Mayordomo, T. Dra, P. Spies, J. Bernhard, and A. Pflaum, "An overview of technical challenges and advances of inductive wireless power transmission," Proc. IEEE, vol. 101, no. 6, pp. 1302–1311, 2013.
17. H. Cao, V. Landge, U. Tata, Y.-S. Seo, S. Rao, S.-J. Tang, H. F. Tibbals, S. Spechler, and J.-C. Chiao, "An implantable, battery less, and wireless capsule with integrated impedance and pH sensors for gastroesophagealreflux monitoring," IEEE Trans. Biomed. Eng., vol. 59, no. 11, pp. 3131–3139, Nov. 2012.
18. P. Bogónez-Franco et al., "An implantable bioimpedance monitor using2.54GHz band for telemetry," Physiological Measurement, vol. 34, 2013 https://doi.org/10.1088/0967-3334/34/1/1
19. D. Holder, "Appendix A. Brief introduction to bioimpedance," Electrical Impedance Tomography Methods, History and Applications. Bristol, PA: Taylor& Francis, pp. 411-422, 2004.
20. A. Ivorra, "Bioimpedance Monitoring for physicians: an overview,"BiomedicalApplications Group, CNM Barcelona, 2002.
21. P Ramakrishna, K Hari Kishore "Implementation of Low Power and Area Efficient 7-Bit Flash Analog to Digital Converter" Journal of Computational and Theoretical Nanoscience, ISSN: 1546-1955, Volume-16, Issue No: (5-6), Page No: 2213-2217, June 2019. https://doi.org/10.1166/jctn.2019.7875
22. R.H. Bayford, "Bioimpedance tomography (electrical impedance tomography), Annual Review of Biomedical Engineering, pp. 63-91, 2006.