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Performance Analysis of Arithmetic Logic Unit with Reversible Logic

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ABSTRACT

With advent of quantum computing the urge of using energy efficient digital circuits have become need of hour for many power constrained applications. Our aim is to develop energy efficient combinational and sequential circuits to implement energy efficient applications for large networks in a standalone manner. Clearly quantum computing principle backs the aim and provides digital circuits with better operational and computing methods to save energy which can further be used to enhance lifetime of networks to work for longer time. This paper presents application of reversible logic in arithmetic logic unit. This unit is integral part for almost all digital computational circuit. The results can be viewed in wider purview of its induction in many industrial applications.

Key words: Quantum Computing, Life Expectancy, Arithmetic Logic Unit, Garbage Output.

1. INTRODUCTION

From last few decades, conventional combinational circuits are facing many problems in development from energy dissipations point of view. Each arithmetic and logic operation dissipates some amount of energy during each process [1]. This loss of energy causes major disruption when the devices are self configured and battery powered. Latest technological advancements in circuit integration methods have made digital devices faster in a sense that is commendable especially for mobile devices. This concept has brought us in a world of tiny and self sustainable devices [2].

In conventional computing, each bit of information causes loss of heat as per Von Neuman-Landauer's principle of entropy that calculates per bit energy [11]. During last decade, it was also anticipated that energy saving using reversible computing will make the system faster but will add remarkable cost to system, which will become difficult choice for large scale industrial applications. However, it will not downsize benefits of reversible computing in energy constrained applications. This makes reversible computing always a favourable solution among researchers.

In [5],[9] and [17] it is clearly shown that digital circuits which works over the principle of reversible computing can remove heat dissipation due to loss of bits during various operations. In conventional digital circuits loss is associated due to less count of output vectors than count of input vectors available. Ascribed to enormous benefits it is finding its ways in the arena of wireless sensor networks, optical signal processing and nanotechnology [4].

Reversible computing is backed by second law of thermodynamics [3]. ALU is important part of a CPU. It performs various mathematical operation; and reasoning functions on operands of instruction words [7]. It stays continuously in operation mode in any digital processing units that are integral parts of computational devices and self sustained units. This makes energy saving crucial for the longevity of these devices, and in turn for lifetime enhancement of networks made up of these devices. Their latest applications are found in development of smart city, precise agriculture monitoring and nuclear reactor surveillance.

Hence the reversible computing concept has becomes need of hour for faster digital technologies with increased reliability in delivery of services to end users [6] [8 [17]. This work proposed two different designs of ALU and their synthesis. Design I is developed using Toffoli reversible gate and Design II is made up with MTSG gate. Further designs are synthesized and results are compared using various performance metrics like garbage output, gate count and quantum cost. Propagation delay, power consumption also monitored and analysed with the pre existing work. Section 2 presents a brief description of few reversible gates. Section 3 provides proposed ALU design I and design II. Section 4 gives simulation results with discussion and comparison with existing designs. In section 5, work is concluded with future scope of proposed research.

2.BACKGROUND

Backward computing mainly depends on the following points:

- Backward computing is the base of quantum computing. In reversible logic any gate will have identical input vectors and output vectors.

- Mapping from input vector to output vector will be always distinctive i.e. will carry unique pattern.
- Present input states can be restored using output states.
- Fan-out is proscribing as it affect uniqueness of mapping.
- Feedbacks are restricted to keep the pattern undamaged.

2.1Feynman Gate

It is an invertible gate i.e. NOT gate but with a control. For this logic gate any input vectors (A,B) are mapped to output vector (P,Q) such as: P=A , Q=(A) XOR (B) as shown in Figure 1. Mostly this gate is implemented as fan-out element; also popular as copying gate; and the 2*2 circuits [12].

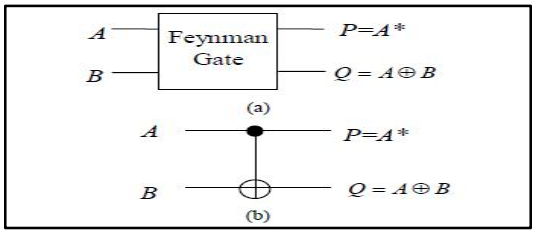

Figure 1: Feyman Gate

2.2Fredkin Gate

It is a universal circuit which comprises 3-input vectors and 3-output vectors; it swapped last two bits if first is '1'. For this gate its input bits (A, B, C) are mapped P=A, Q= (ĀB) XOR(C), R= (ĀC) XOR (AB). Table 1 depicts functions of gate. Its QC is 5; mapping of input and output vector is illustrated in shown in Figure 2 [12].

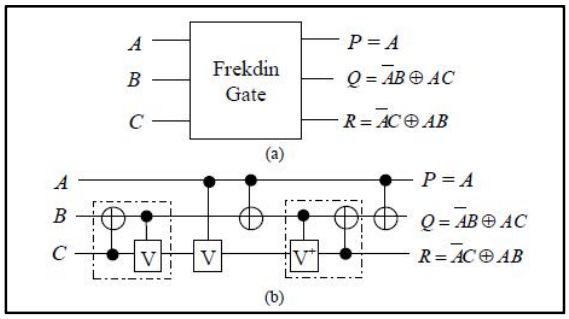

Figure 2: Fredkin Gate

Table 1: Fredkin gate Functions

I/P			O/P		
L	L	L	L	L	L
L	L	H	L	L	H
L	H	L	L	H	L
L	H	H	H	H	H
H	L	L	H	L	L
H	L	H	H	L	H
H	H	L	H	H	H
H	H	H	L	H	L

2.3Toffoli Gate

A digital circuit can be constructed using "Toffoli-Gate", so it comes in category of universal gate. It has three bits long inputs and output, so if any two bits are kept at '1' then it will upturn the third bit.

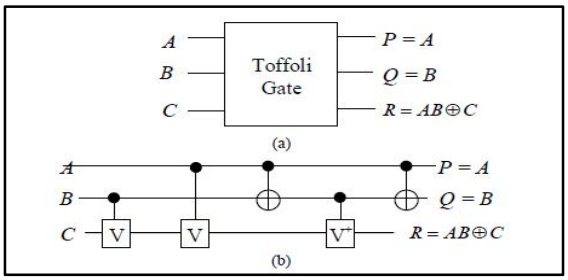

Figure 3: Toffoli gate

The function table is given in Table 2. It maps (A, B, C) to (P, Q, and R) respectively, where R is (AB) XOR (C). Any k-bits toffoli gate takes 'k' bits as input. They are mapped same to same for first 'k-1' bits and last bit is XOR with first AND of 'k-1'bits; as given in Figure 3, [12].

Table 2: Toffoli gate Functions

Reversible Circuits	Circuit Cost
Feynman Gate	1
Fredkin Gate	5
Toffoli Gate	5
R I Gate	4
MTSG	6

2.4 Performance Metrics

The performance analysis of logic circuits is done using following parameters; brief details are provided in Table 3.

Quantum Cost (QC): It provides count for fundamental circuits used to develop any quantum logic circuits. Quantum cost for these reversible quantum gates will be '0' and '1' respectively [15] [16]. If the quantum cost of any designed digital circuits goes up then the efficiency comes down. So for better performance we need to maintain it as low as possible.

Garbage Output (GO): These are the output vectors in a designed reversible circuit that are not used for any further process of computation, only maintain reversibility. They cause generation of heat. For optimization of performance garbage output should be minimized.

Delay: It is the total time taken by any bit to travel from input vector to output vector with complete count of gate circuits used in between gives value of delay.

Table 3: Circuit cost

I/P			O/P		
L	L	L	L	L	L
L	L	H	L	L	H
L	H	L	L	H	L
L	H	H	L	H	H
H	L	L	H	L	L
H	L	H	H	L	H
H	H	L	H	H	H
H	H	H	H	H	L

3. PROPOSED ALU DESIGNS AND SYNTHESIS

An ALU is a core circuit in a central processing unit of a processor that performs usually all kinds of mathematical, computation and data processing operations [1]. The basic arithmetic operations, bitwise logical operations and other complex operation of various modules of task executed by this popular combinational circuit; comprises many other logical units in single block. Generally, a basic ALU comprises two input vector operands and one output operand; can be designed for n-bits which are subjected to size of word processed [2].

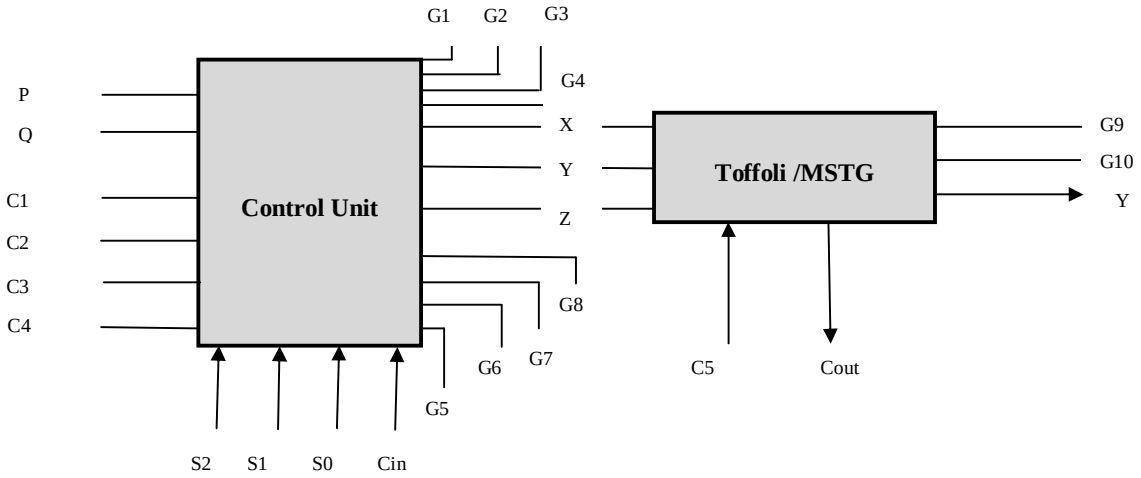

Figure 4: ALU Design I/ II diagram

Although conventionally ALU is designed to perform complex operations as well; that results in increased consumption of power and circuit cost with remarkable increases in complexity of ICs; due to these reasons this approach becomes impractical. Consequently ALUs functions are restricted to simple operations as discussed in Table 4. This idea is exploited in terms of less power consumptions and high speed circuits which is the demand of today's digital technologies. Proposed ALU design with application of reversible gates is presented in Figure 4.

Table 4: Functions of ALU

S_3	S_2	S_1	S_0	C_{in}	O/P	Function
L	L	L	L	L	Y=P	Transfer P
L	L	L	L	H	Y=P+1	Increment P
L	L	L	H	L	Y=P+Q	Add
L	L	L	H	H	Y=P+Q+1	Add w/c
L	L	H	L	L	Y=P+Q'	Sub with borrow
L	L	H	L	H	Y=P+Q'+1	Subtraction
L	L	H	H	L	Y=P-1	Decrement P
L	L	H	H	H	Y=P	Transfer P
L	H	L	L	X	Y=PQ	AND
L	H	L	H	X	Y=PQ	OR
L	H	H	L	X	Y=P+Q	XOR
L	H	H	H	X	Y=P'	NOT
H	L	X	X	X	Y=shr P	Shift right P
H	H	X	X	X	Y=shl P	Shift left P

3.1Control Unit

It is very crucial part of any ALU unit. It mainly tells the ALU to which mathematical and logical operation to be performed on data. Figure 5 illustrates the circuit diagram of the control unit used in these designs. This control unit is build using '3' Feynman gates, '3' RI gates and '1' Fredkin gate. This facilitates the transfer of data between registers and memory. Here S2, S1, S0 and C_{in} are used as control vectors; provides unique reversible data processing operations. This control unit has eight GOs.

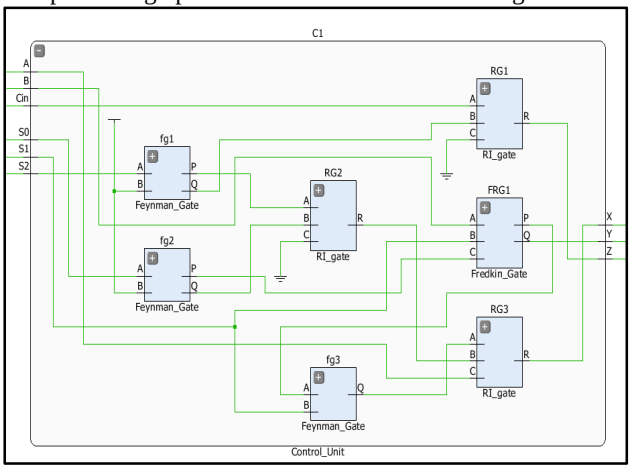

Figure 5: Control Unit Circuit used in Designs

3.2 Full Adder with reversible logic

Adder is a pivotal segment of any arithmetic logic unit. For required compatibility between these two units the paradigm shift is implemented for both quantum and optical logic. Following are their state equations as per equation (1) and (2) for Sum and C_{out} respectively; with inputs as A and B.

$$S=A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = (A \oplus B)C_{in} \oplus AB \quad (2)$$

3.3 Reversible ALU Design I

The design I has toffoli gate as depicted in Figure 6. Four toffoli gates are used to made reversible adder as illustrated in Figure 7. The quantum operator is a 3*3 logic circuit; it is successfully realized using quantum mechanics. The implementation has higher fan out. Here F represents Sum and C_{out} is output vector. While the implementation of adder requires 2n CNOT circuits; can create non trivial quantum state suffices. Figure 8 show the logical circuit TG1 reversible gate used here; with P and Q represents Fan Out.

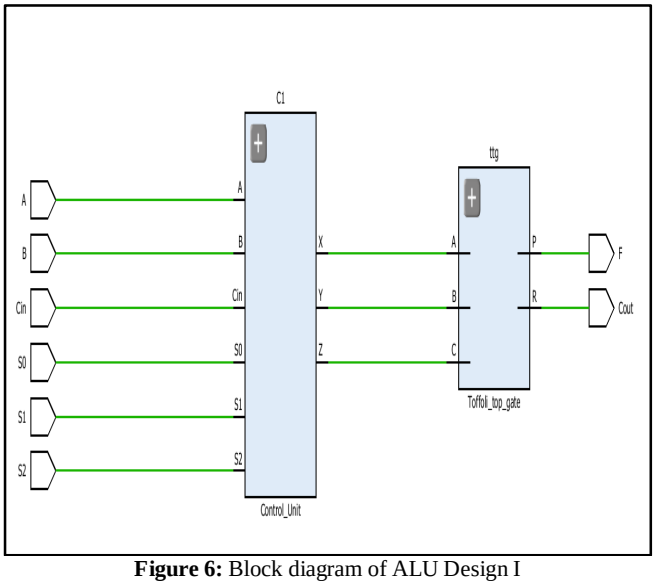

Figure 6: Block diagram of ALU Design I

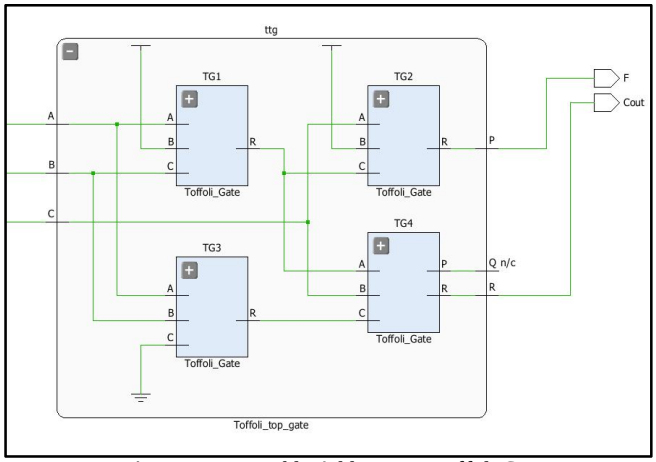

Figure 7: Reversible Adder using Toffoli Gate

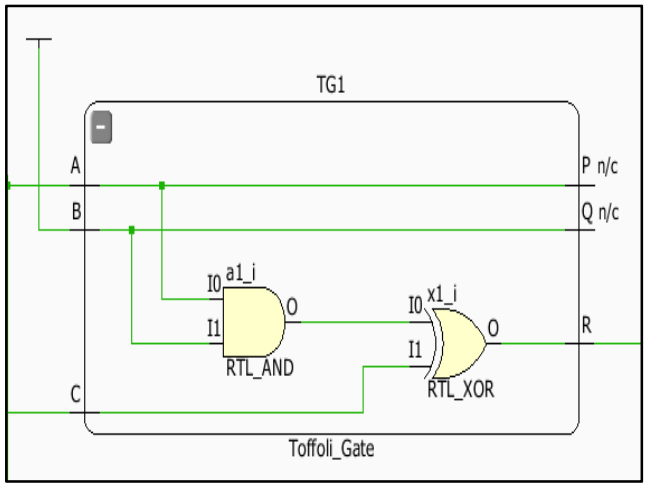

Figure 8: Gate Level Circuit of Toffoli Gate

3.4 Reversible ALU Design II

In second approach of designing reversible ALU; MTSG reversible gate is used in adder circuit. Figure 9 depicts proposed design II. The circuit diagram of MTSG gate is shown in Figure 10. Here MTSG is 4*4 circuits; P and Q are garbage output; while R and S represents Sum and C_{out} in the circuit respectively. Unlike conventional digital circuits these quantum circuits have ortho-normal basis. It is generally assumed that the reduction in propagation delay and power consumption per unit can have larger impact on very large scale integration of these circuits. Further advantage can be seen as expansion in quantum states; that is phenomenal to faster digital world with tiny size self configurable devices. This technological advancement seems to happen instantaneously to resist the latencies in digital circuits; but other interpretations have also emerged as future scope to be dealt with in further extension of work.

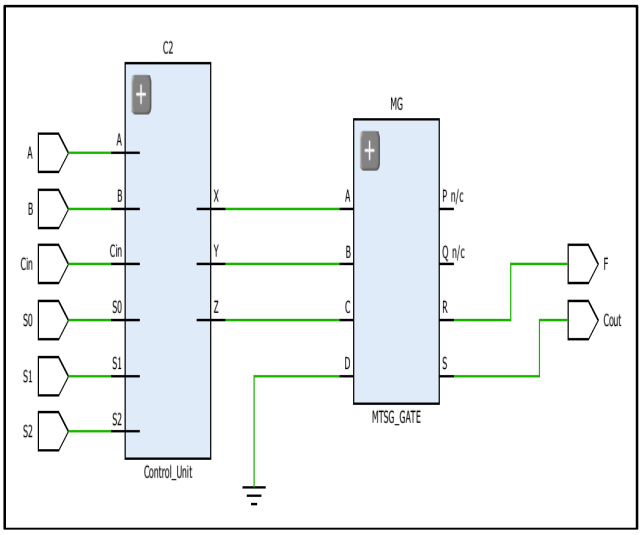

Figure 9: ALU Design II using MTSG Gate

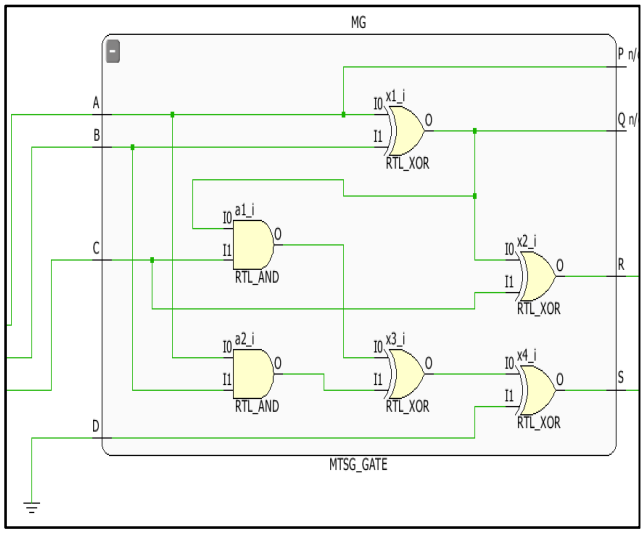

Figure 10: Gate level circuit of MTSG gate

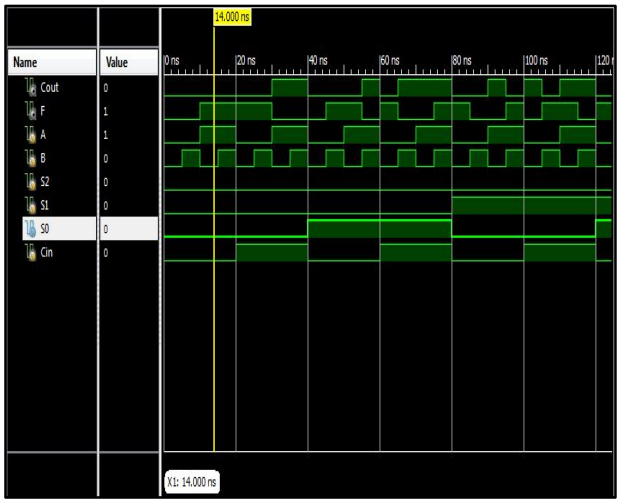

Figure 11: Execution waveform of Design I for Toffoli gate as reversible adder

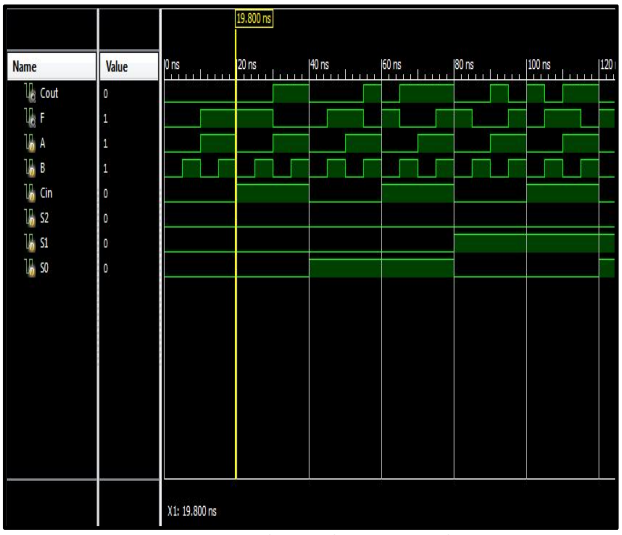

Figure 12: Execution waveform of Design II for MTSG gate as reversible adder

4.SIMULATION RESULTS

Above discussed designs of reversible ALU are executed on Xilinx FPGA family- Nexsys4DDR (xc7a100tcsg324-1). The execution results are provided in Figure 11 and Figure 12 for reversible ALU; built using Toffoli and MTSG respectively. Results clearly satisfy the functions given in Table 4.

From simulation results it can be realized clearly that ALU made up of MTSG gate has shown remarkable improvement in propagation delay making the circuit faster and less expensive in terms of energy consumption. Comparison of propagation delay for various versions of ALU can be seen for both designs in Table 5. Other parametric comparison is given in Table 6. From Table 5; it is seen clearly that design II has shown promising performance in terms of propagation delay improvement and also in power consumption at gate level circuits.

Table 5: Propagation Delays for both designs

Circuits based on bits	Design- I Propagation delay in (ns)	Design -II Propagation delay in (ns)
1-Bit	8.95	8.76
4-Bits	9.04	8.89
8-Bits	9.26	8.96

Table 6: Performance Metrics

Type	GC	GO	QC
Design I Adder with Toffoli Gate	6	15	40
Design II Adder with MSTG gate	5	10	26

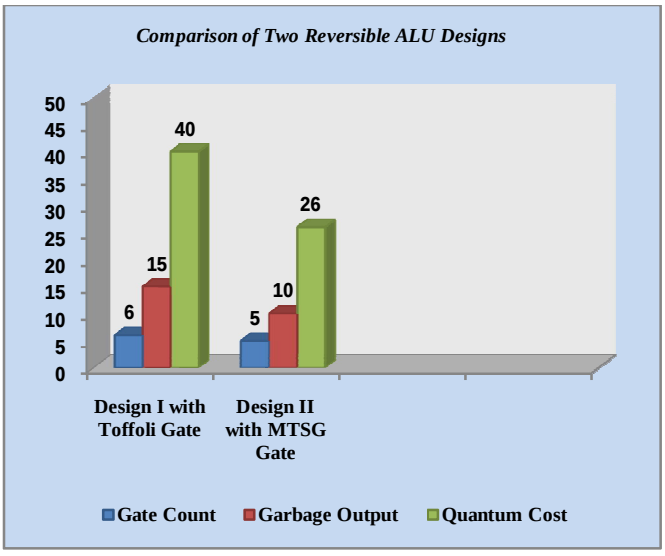

Figure 13: illustrates parametric comparison of Design I and Design II

5. CONCLUSION AND FUTURE SCOPE

In this piece of work, two designs for reversible ALU are presented. It is analysed and compared with the conventional models of ALU. The performance metrics like gate counts, propagation delays, quantum cost and garbage output are discussed from energy efficient circuits point of view. Figure 13 depicts that design II based on MTSG gate has outperforms the first approach. In future scope of work these modules can be extended with implementation at transistor level for various circuits.

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