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Novel Design of Full Adders using QCA Approach

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ABSTRACT

This paper presents a novel design of full adder using QCA approach. It is one of the stand-in technologies introduced as a renewal key to the fundamental limits faced by CMOS technology. Some of the consequences of CMOS technology are their such as high ON/OFF speed, complexity, area and power consumption which are essential to replace with new technology like QCA. By using basic operators like majority gate and an inverter, other logic gates can be designed. Full adders place a major role in computational systems. In this work, 1-bit full adder is mapped out with minimum no. of cells by utilizing cell minimization technique. These circuits are simulated, imitated and verified for their proper output by utilizing QCA designer 2.0.3 tool.

Key words: QCA, Quantum Cells, Majority and Minority gate, Inverter, Adder

1. INTRODUCTION

QCA is commonly implemented as software programs which are proposed in a year 1993, by Lent et al. It was first fabricated in 1997 (figure 1). QCA does not use transistors. Quantum Cell is the basic cell in QCA. QCA cell is charged with two free electrons. These electrons can reside in exactly two possible sites. Thus, there exist two equivalent arrangements of two electrons in the QCA cell. These two courses of action are signified as cell polarization p= +1, p= -1. Here p=+1 represents logic '1' and p=-1 represents logic '0'.

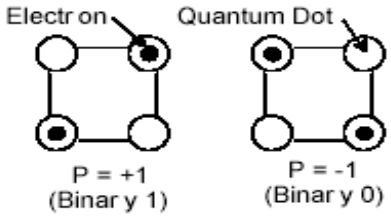


Figure 1: Basic structure of the QCA Cell

1.1 QCA Fundamentals

The fundamental basic elements of QCA are an inverter and a majority gate. Detailed description of the major components is presented in the next sections.

1.2 QCA Majority Gate

It performs 3 input logic functions (figure 2). The cells on top, at the bottom and at the left works as a resource connection cells.

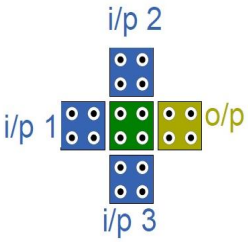


Figure 2: Schematic of the QCA Majority Gate

1.3 QCA Wire

A QCA wire is created by arranging no of QCA cells such that large amount of data can be transferred with the high speed (figure 3). In this the signal propagates from i/p to o/p because of electrostatic association between the cells.

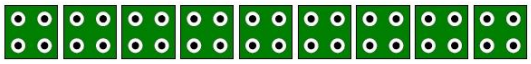


Figure 3: Schematic of the QCA Wire

1.4 QCA Inverter

Inverter is a simple structure. It is normally shaped by setting the cells to the corners touching each other. The inversion operation occurs since the quantum dots are misaligned between the cells (figure 4).

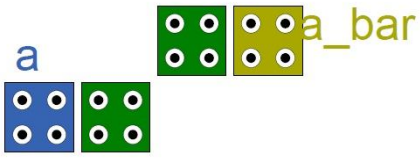


Figure 4: Schematic of the QCA Inverter

1.5 QCA Clocking

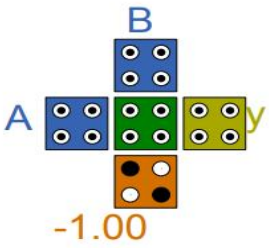
In order to propagate the data from QCA wire, the clock zones through the wire must be aligned with consecutive clock signals for the data propagation (figure 5).

Figure 5: Schematic of Clocking in QCA

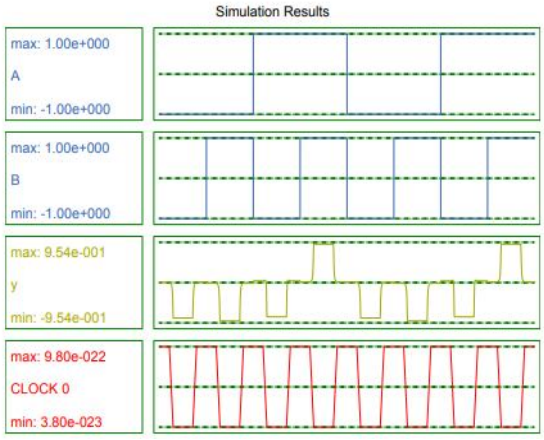
2. BASIC LOGIC GATES

2.1 AND GATE

AND gate can be acquired by keeping the polarization of one of the QCA cell as logic '0' (p= -1) in MG. The required equation is M (A,B,0) = AB (figure 6).



(a)

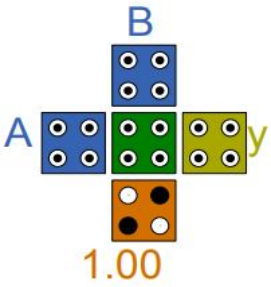


(b)

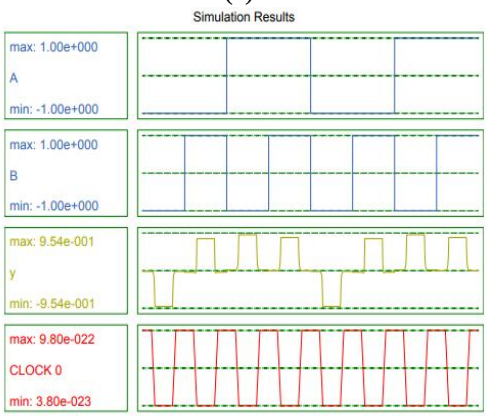
Figure 6: (a) Basic AND Gate (b) AND gate Simulation

2.2 OR GATE

OR gate can be obtained by keeping the polarization of one of the QCA cell as logic '1' (p=1) in MG. The required equation is M (A,B,1)=A+B (figure 7).



(a)

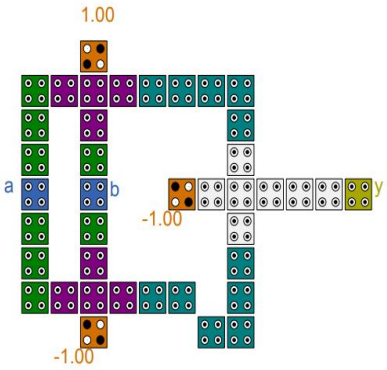


(b)

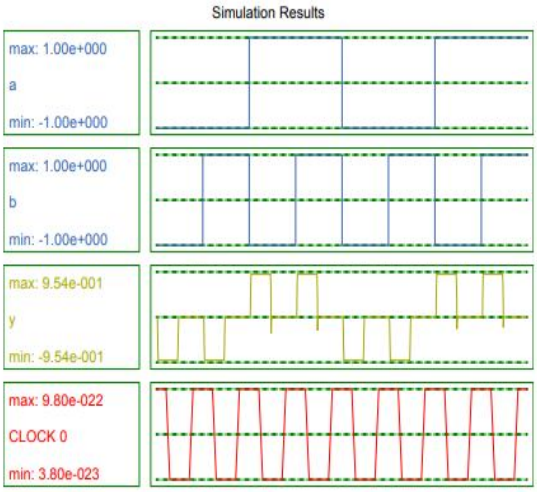
Figure 7: (a) Basic OR Gate (b) OR gate simulation

2.3 XOR Gate

A 3-input MG and an inverter is used to design a 2 input XOR gate. Among the majority gate two AND gates & one OR gates are used (figure 8).



(a)



(b)

Figure 8: (a) Basic XOR Gate (b) XOR gate simulation

3.FULL ADDER

The Full Adder (FA) design is implemented by utilizing digital logic gates (figure 9). A full adder circuit consists of 3 inputs and 2 outputs. Figure 9 shows the block diagram of full adder. The truth table for full adder is shown in Table 1.

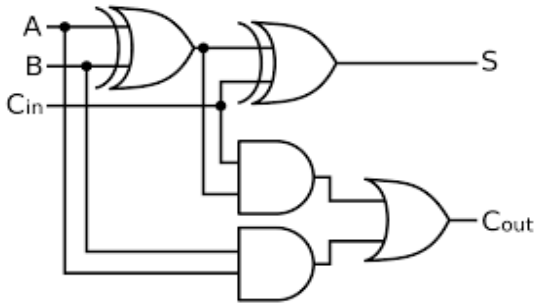


Figure 9: Block diagram of Full Adder

Table 1: 1-bit Full Adder Truth Table

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Expression of Full Adder is given as

$$SUM = \sum m\,(1,2,4,7)$$
$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$
$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$
$$= A \oplus B \oplus C$$

$$CARRY = \sum m\,(1,2,4,7)$$
$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$
$$= C(\bar{A}B + A\bar{B}) + AB(\bar{C} + C)$$
$$= (A \oplus B)C + AB$$

3.1 Previous design

QCA adders are implemented by using majority gates and inverter. These are basic building block of QCA circuits. Most of the circuits are designed by using 3 inputs and 5 input majority gates. In this full adder is achieved by using 5 input majority gates.

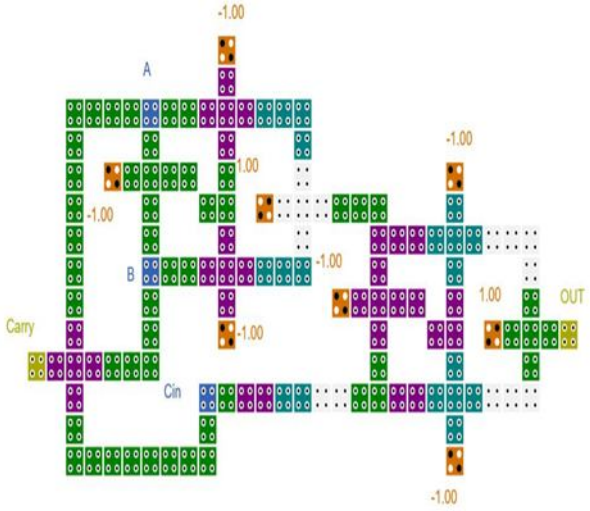


Figure 10: 1-bit Full Adder Previous design

The fundamental basic elements of QCA are an inverter and a majority gate. Detailed description of the major components is

3.2 Proposed design

A systematic adder will have a great assistance in designing mathematical circuits. It can be observed that the structures proposed in this work shows that the structures are nearly three times smaller than conventional designs. In this, full adder is blocked out by utilizing 3 input MG and XOR gates(figure 11).

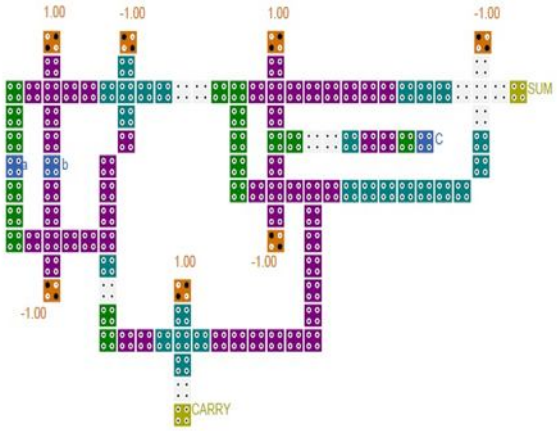


Figure 11: Design of 1-bit Full adder Using QCA Designer Tool

By arranging cells in this way, we get the full adder and the overall number of QCA cells essential to design the FA is 110 total QCA cells with an area of 1980 nm^2.

4.RESULTS AND DISCUSSION

The circuit functionality and robustness is verified utilizing QCA Designer 2.0.3 tool. QCA Designer is the most popular simulation tool among the scientists worldwide for simulation of QCA based circuit design (figure 12). The present adaptation of QCA Designer has 2 diverse simulation engines included. Comparison of various parameters for full adder design is given in Table 2.

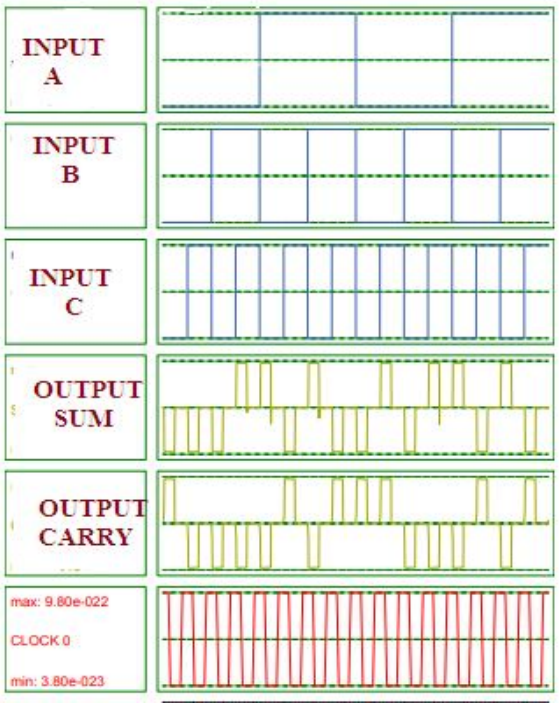


Figure 12: Simulation results of 1-bit adder

Table 2: Results of 1-Bit FA

1 bit FA	Cell count	Area (nm^2)
Previous [Fig. 10]	127	2230
Previous [6]	134	2550
Proposed [Fig. 11]	110	1980

5.POWER DISSIPATION IN QCA

Power dissipation in QCA circuits can be found by QCAPro tool. QCAPro tool is an efficient and powerful tool which finds power dissipation of various types for QCA circuits that have been made utilizing a single layer only [25-29]. One can easily find thermal energy dissipation for QCA design. There will be some hot spots in the thermal model i.e. the black color represents maximum amount of power dissipated and as well as the color goes to while side, it represents the decrease in power dissipation of the circuit itself. Figure 13 and 14 shows the power dissipation results of 1 bit FA. Table 3 shows the Power dissipation analysis of recommended 1-bit FA.

Figure 13: Architecture of the Enhanced Fuzzy Resolution Mechanism using ANFIS

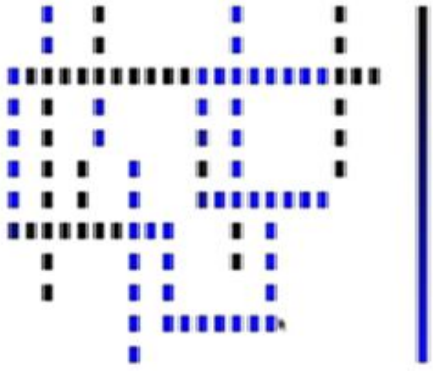


Figure 14: Architecture of the Enhanced Fuzzy Resolution Mechanism using ANFIS

Table 3: Power dissipation analysis of proposed 1-bit FA

Different types of power dissipation	Kink Eenrgy					
	Ek=0.5(mev)x10^{-3}		Ek=1(mev)x10^{-3}		Ek=1.5(mev)x10^{-3}	
	Previous Design	Proposed Design	Previous Design	Proposed Design	Previous Design	Proposed Design
Maximum Energy dissipation of circuit	0.318	0.297	0.382	0.317	0.425	0.350
Avgerage Energy dissipation of circuit	0.264	0.150	0.264	0.190	0.356	0.241
Minimum Energy dissipation of circuit	0.034	0.026	0.095	0.081	0.248	0.146
Average Leakage Dissipation	0.029	0.027	0.095	0.083	0.263	0.149
Average Switching Energy Dissipation	0.248	0.173	0.159	0.107	0.296	0.134

6.CONCLUSION

QCA is a new technology developing to design Quantum computing devices. This methodology is an efficient way that reduces number of cells, area and delay in signal propagation from input to output. From the proposed full adder designs, one can easily compare the designs with reported designs for power dissipation, area, total no of cell counts. The proposed designs are robust and efficient than the previous designs.

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