ISSN 2278-3091
Volume 9, No.5, September - October 2020
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse257952020.pdf
https://doi.org/10.30534/ijatcse/2020/257952020

A Low Power Design of Asynchronous SAR ADC Using DTMOS Technique

P. Ramakrishna[1], R. Naveen Kumar[2], K. Hari Kishore[3], Mukil Alagirisamy[4]
Department of ECE[1, 2], Anurag Group of Intuitions, Hyderabad, Telangana
Professor[3], Department of ECE, Koneru Lakshmaiah Education Foundation, Guntur, A.P, India
[3,4]Department of ECE, Lincoln University College, Petaling Jaya, Selangor, Malaysia

Abstract: This paper substantiates anADC 12-bit SAR with1V input voltage was built in this paper. Using 180 nm technologies, the structure description of various sub blocks was implemented in cadence virtuoso. Comparator was created for proper operation to remain in saturation and could be used withdifferential amplifier. The comparator is thechief blockof power consumption, so we focused mainly much of ability we make to design this module. Boosting the accuracy of DAC sub block, the ladder network R-2R was chosen. Asynchronous control logic in driving ADC the SAR logic power consumed is 165.8uw with input voltage of 1v.

Key words: Comparator, control logic, DAC, low power, SAR ADC

I. INTRODUCTION

Because digital media could be more quickly and efficiently accessed, processed, distributed, analog data must be transformed into digital form. Even then, the real world is digital, so analog to digital converter (ADC) is required at the receiving end portable systems, implantable equipment and extremely effective computer networks require power, field, Since the ADC is the crucial component of almost all communicationnetworks,much more attention helps to pay to the design of ADC.ADC is the key component in designing power-limited systems. Depending on the system's applications and requirements, ADCs could be of various kinds such as Flash, Sigma Delta, SAR ADC; each includes merits capacity and limitations. Such ADCs are identified according to the designer's capabilities. Flash ADC is the quickest ADC at which output is acquired in one stage but as the resolution increases and also the bit number decreases, the count of comparators growing quickly leading to an increase in area consumption and power. If the main criteria are higher resolution, then the ADC Sigma Delta (or ADC form implementation) is introduced. It's the most sluggishADC and its complexsetting too. Several improved and hybrid systems including such as Flash pipeline, SAR pipeline, SARflash is developed and discussed. To enhance processing speed and power consumption optimization. These ADCs have reduced the group of components, and that is not better to adjust power consumption beyond a certain limit.SAR ADC has becoming a bigger subject to study for its excellent power efficiency. It will be used for applications of medium resolution, high speed and low power and small section. This is in the making of an appropriate option such as biomedical purposes software. It consumes less power to its simple structure and therefore innovation scalable as all with its elements or parts are digital other than a comparator. There were some other tasks connected to improve SAR ADC results and this document focus mostly for the extraction of loads. The differential amplifier was used even with fewer disturbances and higher standard noise reduction mode and common source amplifier phase have been used as a second amplification phase and level to keep the transistor in the area of saturation Section II defines the mainSAR ADC architecture. Section III describes various structures of the architecture as well as its diagrams and operation of the control logic. The observations and analysis of the simulation are given in the Section IV and Section V accordingly.

II. SAR ADC STRUCTURE

Because digital media could be more quickly and efficiently accessed, processed, distributed, analog

data must be transformed into digital form. Even then, the real world is digital, so analog to digital converter (ADC) is required at the receiving end portable systems, implantable equipment and extremely effective computer networks require power, field, Since the ADC is the crucial component of almost all communication is shown in figure 1.

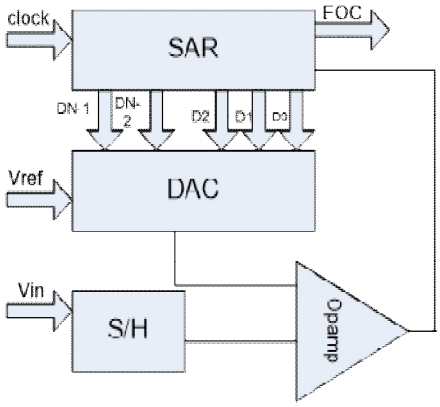

Fig 1: SAR ADC Architecture

III. Design of SAR ADC

A. Track and Hold Circuit

An equivalent Sample and hold circuit is a device in which specified span is used to obtain voltage constantly variable analog signals and locks at a stable value. These are fundamental analog memory instruments that are applied in ADC to get out of some input signal gap which will occur harm mechanism of change**.** Using a condenser, this sample and hold circuit keeps electrical charge to it and then maintains. At only one switching system such as transistor in the field effect and one active amplifier sample and hold samples the input data and gives to comparator. The sample hold circuit is shown in figure 2.

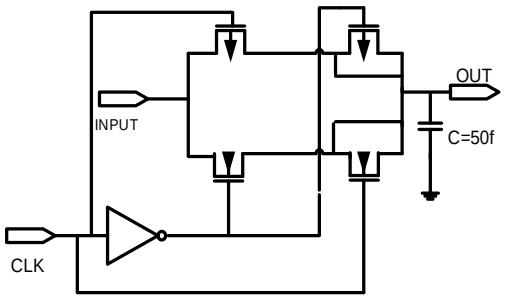

Fig 2: Track and hold circuit

The op amp will switch off and high impedance will be maintained for its output. Unit gain buffer linked take the sample and keep the output phase will be always functional during both sample and hold mode and gives the voltage on hold condenser using the sampling and retaining circuit. Using an operational amplifier, it displays the track and hold circuit. It isconnected by the transition to two op-amps. The sampling method will be on when the switch is in lock state. If the switch is unlocked, the holding will be activated. Connecting the condenser to the second op-amp implies keeping the condenser. We obtain samples of analog signals with the help of the condenser by using the sample and hold circuit. For a certain period of time, it maintains samples. When a stable signal is generated, the analog to digital converter can be used to alter it into a digital signal.

B. Comparator

A comparator is an electronic device that contrasts with two input values are added to it, generating. The comparator's performance value specifies which input is higher otherwise lower. Realize this comparator falls within the range of applications of non-linear IC that comparator is the primary power consumption block in the structure that's the thing much of the progress has been put over this section. The comparator produces a high or low logic output factor depends between analog input and band gap voltage is shown in figure 3. For this function the comparator becomes an improved operational speed and strong resolution.

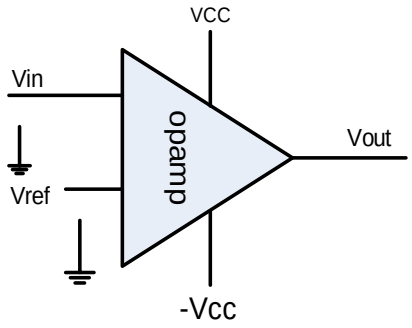

Fig 3: Op amp as comparator

C. Digital to Analog Converter

There are several possibilities to implement DACs along with binary weighted resistors split capacitor array weighted capacitor structure etc. A sector criteria increase as the bit count increases while in

scenario in the binary weighted resistor array type DAC. Therefore, corresponding resistor levels are dynamic.

In the DAC weighted capacitor type, the same problems occur; even now it occupies small area than the previous form. The condenser splitting process therefore decreases area and power consumption thus improves efficiency of those parasites. To improve accuracy, the DAC block was implemented using ladder R-2R network is shown in figure 4.In these only just2 variablesof resistor were applied to shorting up the issue of pairing. Precision and accuracydepend on thevalues of the cho sen resistors.Inmuch architecture, digital word bits are converted into analog signals. DAC architecture is selected on the basis of the code requirements of the data converter. It is necessary to take into account requirements such as accuracy, power, location, the voltage from the reference voltage to the source is stored and released. Transistor current sources can also be used to produce analog output voltages by output currents.

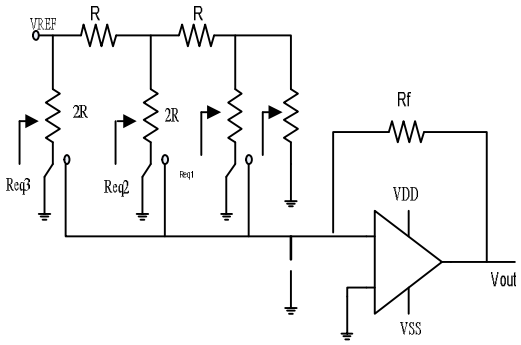

Fig 4: Resistor Ladder Network

D. Successive Approximation Register Logic

Many ADC designs were developed over the years to satisfy the needs of a variety of applications. The predominating systems for industry and science were four of them, i.e. the successive register for approximation (SAR), delta-sigma (delta), the pipeline and the flash system. Every converter provides its benefits and unique drawbacks. Thedesign of selection for moderate-to-high resolution low to spatial resolution sampling speeds is widely used as the successive analog to digital converter reference register (ADCs). SAR sampling speeds historically did not exceed 5 max comparisons per second; however, the case is not as mentioned later with system scaling and newfound techniques. SAR ADC resolutions typically range from 8-16-bit, and low power consumption and a limited die area are given by the SAR ADCs. The approach is suitable with broad variety for the applications like compact devices, manufacturing review and the processing of information / signals obtained. The SAR conversion uses a binary search algorithm as its name implies. The inner circuit is therefore much easier to run than the full ADC sampling frequency. In general, the inner circuit runs at least as quickly like resolution forthe Analog-to-Digital Converters ample rate. Thus a 10 bit, 1 MS/S SAR ADC [4]. Internally does not operate any slower than 10 MHz, allowing for the resolution of all 10 bits in one sample time. An SAR ADC's fundamental structure is very basic and can be seen in Figure 5 even though it developed over the years with further variations and development. A test (or monitor-and-hold) carries the analog input voltage (V_{IN}). Its N-bit register shall then be fixed for a medium-range (MSB is fixed to 1, with all remaining bits lean to 0), thus causing a value of the digital-to-analog conversion (V_{DAC}) often to match $V_{REF/2}$ as V_{REF} might be voltage of reference given for the ADC. This is the result with a half-interval search for itsDigitalizationofAnalog Voltage. The comparator then determines whether V_{IN} reaches or is less than V_{DAC}. The performance of the comparator is logical' high' when V_{IN} is higher than V_{DAC}, and the MSB of the N bits record is 1.When V_{IN} is lower than V_{DAC}, the theoretical ‘low' is the comparator performance, and the registry MSB is transformed into 0. A SAR command controller changes down towards another step then apply that process to most sections. After the sampled analog voltage is done, the digital term N-bit will be made ready for conversion in the register.

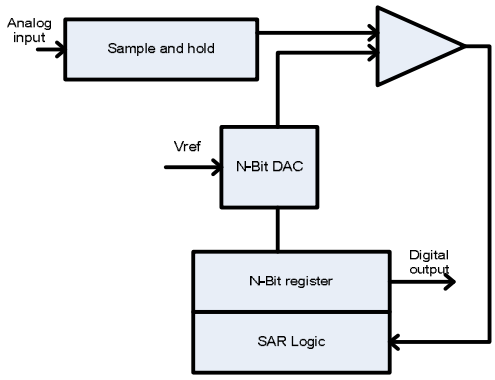

Fig 5: Schematic View of SAR ADC

IV. DTMOS LOGIC

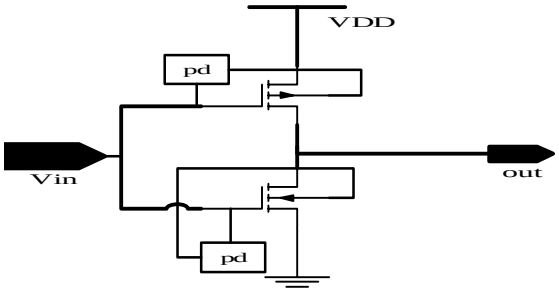

Fig 6: DTMOS Logic Diagram

For adaptive threshold CMOS, their pinch off voltage was changed progressively match its operational status upon the device here the NMOS and PMOS transistor body is biased dynamically as shown in figure 6. Sufficient body biasing voltage to both PMOS and NMOS transistors are provided by the potential dividers which are connected to the input for that inverter. The maximum input impedance in ideal mode provides lower conduction losses whereas a small voltage level makes to large output switches in aggressive state. It could attain adaptive CMOS threshold while binding the gate with body attached. DTMOS input power is constrained mostly by constructed-in diode ability in mass silicon machineries. A p-n diode must be negative voltage among source and body.

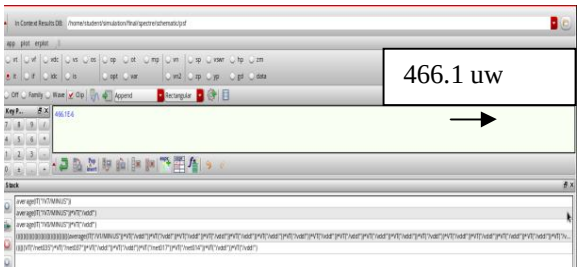

Fig 7: Power consumption of 12 Bit SAR ADC

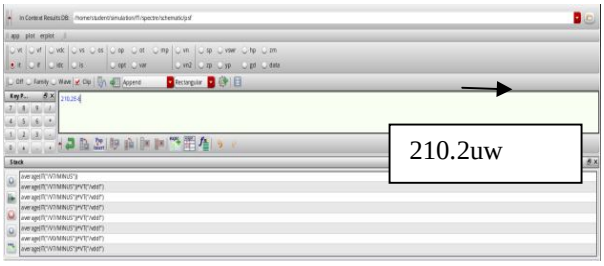

Fig 8: Power consumption of 12 Bit VTCMOS SAR ADC

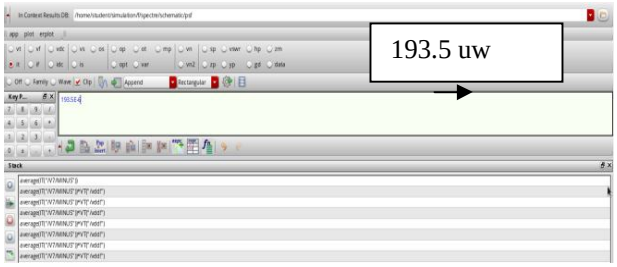

Fig 9: Power Consumption of 12 Bit MTCMOS SAR ADC

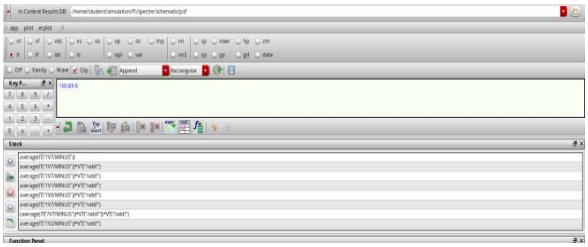

Fig 10: Power consumption of 12 Bit I ADC

V. RESULTS AND EXPLORATION

Hence results obtained during this aspect can be found in this chapter, where their implications are addressed as well as the use of CMOS 180 nm technology for circuit implementation. The obtained results with different low power techniques are shown in figures from 7-10. The output of the SAR ADC can observe in the figure 11.

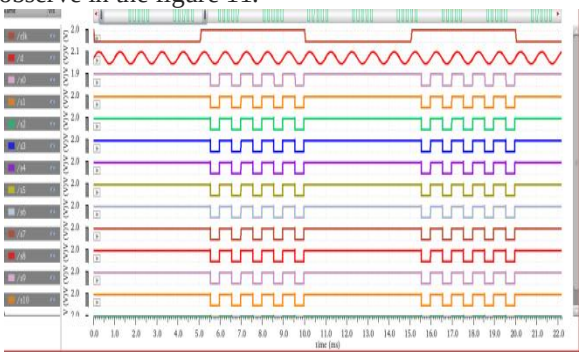

Fig 11: simulation results of 12 Bit SAR ADC

Table-1 Comparison with Existing Work

Parameter	Base paper	In this work
Input supply (V)	1.2	1
Resolution (bits)	8	12
Sampling Rate(MS/s)	0.1-20	0.1-30

Table-2 Power Consumption Values

Parameter	Power Consumption
12 Bit SAR ADC	466.1uw
12 Bit VTCMOS SAR ADC	210.2uw
12 Bit MTCMOS SAR ADC	193.5uw
12 Bit DTMOS SAR ADC	165.8uw

VI. CONCLUSION

This paper12-bitsuccessive ADC approximation is functionally concluded with 1V supply voltage and which is simulated in cadence 180nm CMOS technology this paper mainly focuses on. Minimum power comparator and Digital-to-analog converter (DAC) as more power is used by SAR ADC. The SAR ADC is more appropriate to biomedical applications such as Pacemaker MRI and EEGS.

REFERENCES

[1] Y Madhu Sudhan Reddy, R. S. Ernest Ravindran, K Hari Kishore "Diabetic Retinopathy through Retinal Image Analysis: A review" International Journal of Engineering and Technology (UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 1.5, Page No: 19-25, January 2018.

[2] Yarragudi Madhu Sudhana Reddy, Ramaswami Sachidanandan Ernest Ravindran, Kakarla Hari Kishore "Spatial Mutual Relationship Based Retinal Image Contrast Enhancement for Efficient Diagnosis of Diabetic Retinopathy" International Journal of Intelligent Engineering and Systems, E-ISSN No: 2185-3118, Vol No: 11, Issue No: 5, Page No: 48-58, August 2018

[3] Mahesh Madavath, K Hari Kishore **"**RF Front-End Design of Inductorless CMOS LNA Circuit with Noise Cancellation Method for IoT Applications" International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, Volume-8, Issue No: 6, Page No: 176-183, April 2019.

[4] K.Sarath Chandra, K Hari Kishore **"**Electrical Characteristics of Double Gate FINFET under Different Modes of Operation" International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, Volume-8, Issue No: 6S, Page No: 172-175, April 2019.

[5] P.Ramakrishna, M. Nagarani, K Hari Kishore **"**A Low Power 8-Bit Current-Steering DAC Using CMOS Technology" International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, Volume-8, Issue No: 6S, Page No: 137-140, April 2019.

[6] Avinash Yadlapati, K Hari Kishore **"**Implementation of Asynchronous FIFO using Low Power DFT" International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, Volume-8, Issue No: 6S, Page No: 152-156, April 2019.

[7] P Ramakrishna, K Hari Kishore"Implementation of Low Power and Area Efficient 7-Bit Flash Analog to Digital Converter" Journal of Computational and Theoretical Nanoscience, ISSN: 1546-1955, Volume-16, Issue No: (5-6), Page No: 2213-2217, June 2019.

[8] Mahesh Madavath, K Hari Kishore"Design and Analysis of Receiver Front-End of CMOS Cascode Common Source Stage with Inductive Degeneration Low Noise Amplifier on 65 nm Technology Process" Journal of Computational and Theoretical Nanoscience, ISSN: 1546-1955, Volume-16, Issue No: (5-6), Page No: 2628-2634, June 2019.

[9] K Hari Kishore, Fazal Noorbasha, Katta Sandeep, D. N. V. Bhupesh, SK. Khadar Imran, K. Sowmya "Linear convolution using UT Vedic multiplier" International Journal of Engineering and Technology(UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 2.8, Page No: 409-418, March 2018.

[10] K Hari Kishore, B. K. V. Prasad, Y. Manoj Sai Teja, D. Akhila, K. Nikhil Sai, P. Sravan Kumar "Design and comparative analysis of inexact speculative adder and multiplier" International Journal of Engineering and Technology(UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 2.8, Page No: 413-426, March 2018.

[11] G Siri Vennela, K Hari Kishore, E Raghuveera "High Accurate and Power Efficient ECG-Based Processor for Predicting Ventricular Arrhythmia" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 10, Issue No: 2, Page No: 1180-1121, May 2018.

[12] Avinash Yadlapati, K Hari Kishore "Low Power Synthesis for Asynchronous FIFO using Unified Power Format (UPF)" International Journal of Engineering and Technology (UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 2.8, Page No: 7-9, March 2018.

[13] Chella Santhosh, K. Hari Kishore, G. Pavani Lakshmi, G.Kushwanth, P. Rama Krishna Dharma Teja, R. S. Ernest Ravindran, Sree Vardhan Cheerala, M. Ravi Kumar **"**Detection of Heavy Metal Ions using Star-Shaped Microfluidic Channel" International Journal of Emerging Trends in Engineering Research, ISSN: 2347-3983, Volume-7 Issue-12, Page No: 768-771, December 2019.

[14] B. Srikanth, M. Siva Kumar, J.V.R. Ravindra, K. Hari Kishore **"**Double Precession Floating Point Multiplier using Schonhage-Strassen Algorithm used for FPGA Accelerator" International Journal of Emerging Trends in Engineering Research, ISSN: 2347-3983, Volume-7 Issue-11, Page No: 677-684, December 2019.

[15] Nadhindla Bala Dastagiri, Kakarla Hari Kishore, Vinit Kumar Gunjan and Shaik Fahimuddin, "Design of a Low-Power Low-Kickback-Noise Latched Dynamic Comparator for Cardiac Implantable Medical Device Applications", Lecture Notes in Electrical Engineering, ISSN No: 1876-1100, E-ISSN: 1876-1119, pp. 637-645, 2018.

[16] Avinash Yadlapati, Hari Kishore Kakarla"Low-power design-for-test implementation on phase-locked loop design" Measurement and Control, ISSN: 0020-2940, Volume-52, Issue No: (7-8), Page No: 995-1001, June 2019.

[17] Nan Jiang, Abdol Ghaffar Ebadi, Kakarla Hari Kishore, Qahtan.A.Yousif, Mohammad Salmani "Thermomechanical Reliability Assessment of Solder Joints in a Photo-voltaic Module Operated in a Hot Climate" IEEE Transactions on Components, Packaging and Manufacturing Technology, P-ISSN: 2156-3950, E-ISSN: 2156-3985, Vol No: 10, Issue No: 1, Page No: 160-167, January 2020.

[18] Mahesh Madavath, Hari Kishore Kakarla, Azham Hussain, C.S. Boopathi **"**Design and Analysis of CMOS RF Receiver Front-End of LNA for Wireless Applications" Microprocessors and Microsystems, ISSN: 0141-9331, Volume-75, June 2020. Article number 102999.

[19] K Divya Madhuri, K Hari Kishore "Implementation of 4-bit Ripple Carry Adder by Adopting Sub threshold Adiabatic Logic for Ultralow-Power Application" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 12, Issue No: 6, Page No: 11-17, May 2020.

[20] B Srikanth, M Siva Kumar, J V R Ravindra, K Hari Kishore"The enhancement of security measures in advanced encryption standard using double precision floating point multiplication model" Transactions on Emerging Telecommunications Technologies, ISSN: 2161-3915, Volume: 31, Feb 2020.

[21] A. Surendar, K. H. Kishore, M. Kavitha, A. Z. Ibatova, V. Samavatian "Effects of Thermo-Mechanical Fatigue and Low Cycle Fatigue Interaction on Performance of Solder Joints" IEEE Transactions on Device and Materials Reliability, P-ISSN: 1530-4388, E-ISSN: 1558-2574, Vol No: 18, Issue No: 4, Page No: 606-612, December-2018.

[22] Sk.Md.Reyaan, B.Manoj Venkat, G.Y.V.Siva Shankar, K Hari Kishore, Fazal Noorbasha, Y Archana, Shaik Razia "Power Analysis of FIR Filter Design Using APC-OMS Algorithm" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 12, Issue No: 2, Page No: 1085-1092, March 2020.

[23] Bhogadi Anil Kumar, Chillapalli Haritha, Gumpena Veda Sri Leela, E Raghuveera, K Hari Kishore" A Parametric DFT Scheme for RAMs" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 12, Issue No: 2, Page No: 2298-2305, May 2020.

[24] K Divya Madhuri, K Hari Kishore "Implementation of 4-bit Ripple Carry Adder by Adopting Sub threshold Adiabatic Logic for Ultralow-Power Application" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 12, Issue No: 6, Page No: 11-17, May 2020.

[25] A Murali, K Hari Kishore "An Efficient Debugging Architecture for DTG Based FIR Filter Using I2C Protocol in DSP Processor" International Journal of Emerging Trends in Engineering Research, ISSN: 2347-3983, Volume-8 Issue-7, Page No: 3468-3477, August 2020.

[26] Avinash Yadlapati, Hari Kishore Kakarla "Design and Verification of Asynchronous FIFO with Novel Architecture Using Verilog HDL" Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No: 14, Issue No: 1, Page No: 159-163, January 2019.

[27] Avinash Yadlapati, K Hari Kishore "System Level Verification of Advanced Extensible Interface Protocol Using Verilog HDL" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 10, Special Issue No: 7, Page No: 1359-1365, June 2018.

[28] P Ramakrishna, K Hari Kishore "DESIGN OF AN ULTRA LOW POWER CMOS COMPARATOR FOR DATA CONVERTERS" Journal of Advanced Research

in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 10, Special Issue No: 7, Page No: 1347-1352, June 2018.

[29] G Siri Vennela, K Hari Kishore, E Raghuveera "High Accurate and Power Efficient ECG-Based Processor for Predicting Ventricular Arrhythmia" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 10, Issue No: 2, Page No: 1180-1121, May 2018.

[30] Ch. Naga Babu, P. Naga Siva Sai, Ch.Priyanka, K Hari Kishore, M.Bindu Bhargavi,K.Karthik "Comparative Analysisof High Speed Carry Skip Adders" International Journal of Engineering and Technology (UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 2.24, Page No: 121-125, April 2018.

[31] Avinash Yadlapati, K Hari Kishore "Low Power Synthesis for Asynchronous FIFO using Unified Power Format (UPF)" International Journal of Engineering and Technology (UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 2.8, Page No: 7-9, March 2018.

[32] Avinash Yadlapati, Kakarla Hari Kishore,"Constrained Level Validation of Serial Peripheral Interface Protocol", Proceedings of the First International Conference on Smart Innovation, Systems and Technologies 77, ISSN No: 2190-3018, ISBN: 978-981-10-5544-7, Chapter No: 77, pp. 743-753, 2018.

[33] Nadhindla Bala Dastagiri, Kakarla Hari Kishore, Vinit Kumar Gunjan and Shaik Fahimuddin, "Design of a Low-Power Low-Kickback-Noise Latched Dynamic Comparator for Cardiac Implantable Medical Device Applications", Lecture Notes in Electrical Engineering, ISSN No: 1876-1100, E-ISSN: 1876-1119, pp. 637-645, 2018.

[34] P Kiran Kumar, P Prasad Rao, Kakarla Hari Kishore, "Optimal Design of Reversible Parity Preserving New Full Adder/Full Subtractor", Proceedings of 2017 11thInternational Conference on Intelligent Systems and Control, ISCO 2017,7856019, pp. 368-373, 25th and 26th February 2017.

[35] Meka Bharadwaj, Hari Kishore "Enhanced Launch-Off-Capture Testing Using BIST Designs" Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No.12, Issue No.3, page: 636-643, April 2017.

[36] B. Srikanth, Dr. M. Siva Kumar, Dr. K Hari Kishore, Dr. J.V.R. Ravindra "Towards Reducing Area And Power Of A Multiplier With Double Precision Floating Point Computations Using FPGA Accelerators" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 9, Special Issue No: 18, Page No: 2780, December 2017.

[37] M. Vasudha, B. Sri Pravallika, Ch. Sai Kiran, P. Subhani, G. Rakesh Chowdary, M Durga Prakash, K Hari Kishore, T.V. Ramakrishna "Design and Performance Analysis of A Nonvolatile Memory Cell" Journal of Advanced Research in Dynamical and Control Systems, ISSN No: 1943-023X, Vol No: 9, Special Issue No: 14, Page No: 2320, December 2017.

[38] A Murali, K Hari Kishore, D Venkat Reddy "Integrating FPGAs with Trigger Circuitry Core System Insertions for Observability in Debugging Process" Journal of Engineering and Applied Sciences, ISSN No: 1816-949X, Vol No.11, Issue No.12, page: 2643-2650, December 2016.

[39] Nazeer Hussain, K Hari Kishore, ''Heuristic Approach to Evaluate the Performance of Optimization Algorithms in VLSI Floor Planning for ASIC Design'', Studies in Computational Intelligence, Volume: 885, ISSN: 1860-949X, Pp: 213-225, 5th February 2020.

[40] Avinash Yadlapati, Hari Kishore Kakarla**"**Low-power design-for-test implementation on phase-locked loop design" Measurement and Control, ISSN: 0020-2940, Volume-52, Issue No: (7-8), Page No: 995-1001, June 2019.

[41] Mahesh Madavath, K Hari Kishore**"**Design and Analysis of Receiver Front-End of CMOS Cascode Common Source Stage with Inductive Degeneration Low Noise Amplifier on 65 nm Technology Process" Journal of Nanoscience and Nanotechnology, ISSN: 1546-1955, Volume-16, Issue No: (5-6), Page No: 2628-2634, June 2019.

[42] P Ramakrishna, K Hari Kishore**"**Implementation of Low Power and Area Efficient 7-Bit Flash Analog to Digital Converter" Journal of Nanoscience and Nanotechnology, ISSN: 1546-1955, Volume-16, Issue No: (5-6), Page No: 2213-2217, June 2019.

[43] Mahesh Madavath, K Hari Kishore **"**RF Front-End Design of Inductorless CMOS LNA Circuit with Noise Cancellation Method for IoT Applications" International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, Volume-8, Issue No: 6, Page No: 176-183, April 2019.

[44] K.Sarath Chandra, K Hari Kishore **"**Electrical Characteristics of Double Gate FINFET under Different Modes of Operation" International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, Volume-8, Issue No: 6, Page No: 172-175, April 2019.

[45] P.Ramakrishna, M. Nagarani, K Hari Kishore **"**A Low Power 8-Bit Current-Steering DAC Using CMOS Technology" International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, Volume-8, Issue No: 6, Page No: 137-140, April 2019.

[46] Avinash Yadlapati, K Hari Kishore **"**Implementation of Asynchronous FIFO using Low Power DFT" International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, Volume-8, Issue No: 6S, Page No: 152-156, April 2019.

[47] Mahesh Madavath, Hari Kishore Kakarla, Azham Hussain, C.S. Boopathi **"**Design and Analysis of CMOS RF Receiver Front-End of LNA for Wireless Applications" Microprocessors and Microsystems, ISSN: 0141-9331, Volume-75, Article: 102999, June 2020.

[48] K Hari Kishore, Fazal Noorbasha, Katta Sandeep, D. N. V. Bhupesh, SK. Khadar Imran, K. Sowmya "Linear convolution using UT Vedic multiplier" International Journal of Engineering and Technology(UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 2.8, Page No: 409-418, March 2018.

[49] K Hari Kishore, B. K. V. Prasad, Y. Manoj Sai Teja, D. Akhila, K. Nikhil Sai, P. Sravan Kumar "Design and comparative analysis of inexact speculative adder and multiplier" International Journal of Engineering and Technology(UAE), ISSN No: 2227-524X, Vol No: 7, Issue No: 2.8, Page No: 413-426, March 2018.

[50] Nadhindla Bala Dastagiri, Kakarla Hari Kishore, Vinit Kumar Gunjan and Shaik Fahimuddin, "Design of a Low-Power Low-Kickback-Noise Latched Dynamic Comparator for Cardiac Implantable Medical Device Applications", Proceedings of Lecture Notes in Electrical Engineering 434, pp. 637-645, ISSN No: 1876-1100, E-ISSN: 1876-1119, January 2018.