ISSN 2278-3091
Volume 8, No.1.3, 2019
International Journal of Advanced Trends in Computer Science and Engineering
Available Online at http://www.warse.org/IJATCSE/static/pdf/file/ijatcse2481.32019.pdf
https://doi.org/10.30534/ijatcse/2019/2481.32019

Low-Voltage, High-Speed CMOS Dynamic Latch Voltage Comparator for ADC Module

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ABSTRACT

Comparators are one of the most important block in analog to digital converter (ADC) circuit. ADCs in turns are used widely in data acquisition system and must be fast enough to capture the analog signal. ADCs are also used continuously, thus triggering the need of low power consumption to prolong the battery life. In facing this scenario, this project has designed a low-power and high-speed voltage comparator for the ADC module. In order to have a high speeds performance and better power consumption, the voltage comparator is designed using Silterra 130 nm Complementary Metal Oxide Semiconductor (CMOS) technology with a 1 V voltage supply through a dynamic latch technique. The circuit is simulated using Cadence software and the circuit achieved a total average power consumption of 85.1 µW and a delay of 113.6 ps.

Key words : CMOS voltage comparator, Dynamic latch, High speed, Low-voltage.

1. INTRODUCTION

Nowadays, many applications such as signal filtering and processing are processed digitally. Designers of digital integrated circuit (IC) need to develop a fast analog to digital converter (ADC) circuit because ADC will influence the overall performance of the applications [1]. In these applications, the power consumption and processing time is very critical. Most ADCs use a comparator as part of their building blocks. Hence the comparator must have a high speed and consume less power.

Comparator is used to compare two analog signals and will give the output in binary signal based on the comparison [2]-[3]. Since the input signals are usually low in amplitude, a preamplifier circuit is needed for the comparator. A differential amplifier with active loads is usually the first stage of the preamplifier. The differential amplifier will produce a very high gain. It amplifies the difference between two input voltages. The output of the preamplifier is connected to the decision-making circuit or latch. The decision-making circuit determines which signal is greater by comparing the signals.

A flash and pipeline ADC architecture usually use the preamplifier based comparators [4]. A preamplifier based comparator is a regenerative comparator, it uses back to back latch stage and positive feedback [5, 6]. The preamplifier in a comparator with latch is used to reduce the kickback effect [1]-[5]. This will help in eliminating noise.

A latch is defined as the memory unit that stores a charge on the gate capacitance of an inverter [4]. A commonly used architecture in analog circuits is a dynamic latch because it provides excellent speed along with an acceptable accuracy. A dynamic latch circuit can be constructed using a cross coupled pair of PMOS and NMOS transistors [6]-[7]. The latch works in two phases which is governed by a clock (CLK) level either low or high.

2. VOLTAGE COMPARATOR

The proposed voltage comparator circuit being designed consists of a preamplifier and a dynamic latch.

2.1. Comparator basic

In electronics, a comparator is used to compare two voltages and it will specify which input is higher by stating the output in digital form [1]. A block diagram of a comparator is illustrated in Figure 1. Two terminals at the input are the analogue inputs indicated by V+ and V− and the output in digital form is Vo.

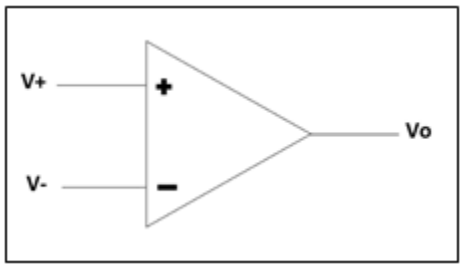

Figure 1: Block diagram of a comparator

Referring to Figure 1, when the input voltage at the positive terminal (V+) is greater than the input voltage at the negative terminal (V-), the output will be a positive value or logic 1. However, when the input at the negative terminal is greater, the output voltage will be negative or logic 0. In simple term, the output voltage is according to equation (1).

$$V_o = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases} \quad (1)$$

2.2. Preamplifier

The preamplifier is used to amplify the input signal. This is done by inputting the signal to the first stage of the preamplifier circuit which is a differential amplifier with active loads. This is followed by a circuit to minimize kickback noise and to reduce the effect of offset voltage error caused by of device mismatch [5]. The output of the preamplifier is connected to the decision-making circuit. The decision-making circuit compares the signals and determines which signal is greater. The output of the decision-making circuit is then converted into a logic signal [2] by an output buffer circuit. The preamplifier used here is self-biased differential circuit with active loads in order to reduce the effect of offset voltage error caused because of device mismatch [8].

Figure 2 shows a regularly used preamplifier in a comparator circuit. The preamplifier can amplify the input signals and reduce the comparison time of regenerative latch comparator. Therefore the speed of the comparator will be improved. Furthermore, it also can amplify the differential input signals to reduce the influence of the offset voltage. Hence, the preamplifier will have a high gain and a wide bandwidth [9].

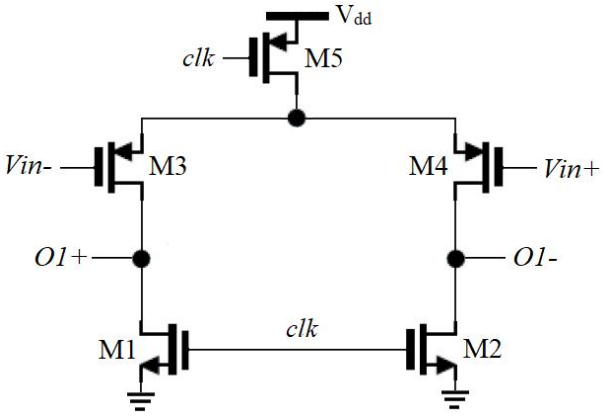

Figure 2: Conventional preamplifier [9]

2.3. Dynamic latch

A dynamic latch stage as depicted in Figure 3 is a second stage of the comparator circuit. In the circuit, two inverters connected back-to-back is used to form a differential comparator. NMOS transistors are also used and placed between the two differential nodes of the latch. The latch stage will amplify the difference between input signals after determining which of the input signals is greater. The output of the latch will be in digital output level indicating whether the differential input signal is positive or negative [1].

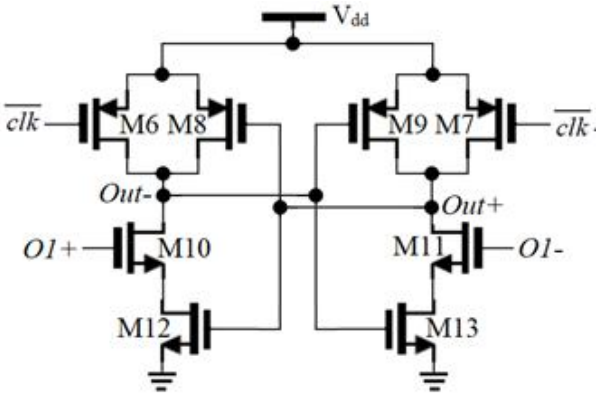

Figure 3: Dynamic latch [9]

A comparator with a latch in the second stage needs a high accuracy clock signal since the latch circuit detects the differential voltage output of the first stage. The high accuracy clock signal can be achieved by using an inverter circuit between both clock signals [4].

2.4. Low voltage comparator

Several comparator circuits using low voltage supply have been reported and different techniques have been used to minimize performance degradation. For example, a Lewis-Gray comparator with adjustable threshold voltage which supposed to consume low DC power. However, the size of the input transistor pair in this comparator has to be very large in order to minimize the offset voltage and this cause an increase in the power consumption [3].

Another comparator is a differential pair comparator which has a very fast operation and low overall offset voltage. But the circuit requires large voltage supply since its structure consists of a stack of four transistors. This will create a problem in low-voltage deep-submicron CMOS technologies1. Hence, the differential pair comparator is not suitable for a comparator with a low power supply.

In this paper a new method is proposed to tackle the problem of high power consumption and at the same time producing a fast circuit. The size of all the transistors used has to be optimized in such a way so that both low power and high speed can be achieved and the circuit will be suitable for high speed ADCs.

3. LOW POWER LATCH COMPARATOR

The comparator designed in this project is the dynamic type circuit. It is chosen because it has low power input capacitance and contention during switching. Dynamic circuit also has zero static power dissipation. There are two modes of operation when using dynamic circuit which are pre-charge and evaluation [5]-[6]. Hence the clock pulse applied to the

preamplifier and latch stage must be alternated. Figure 4 shows the block diagram of the proposed voltage comparator.

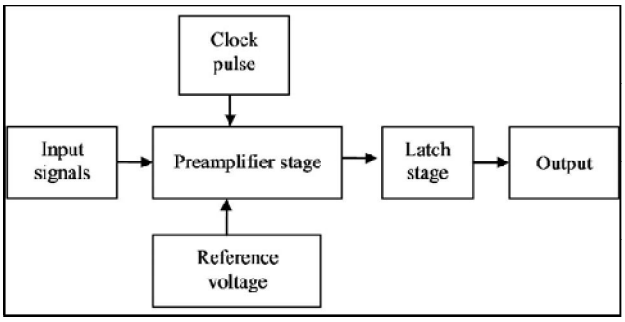

Figure 4: Block diagram for the voltage comparator

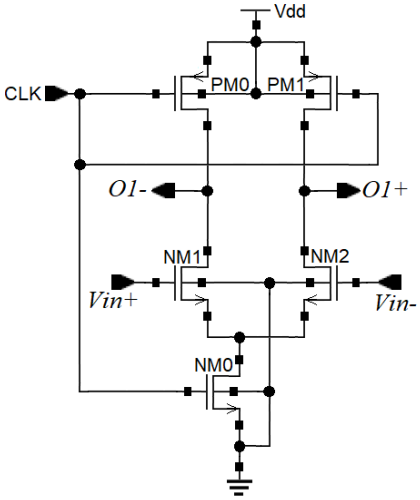

Figure 5: The proposed preamplifier circuit

The preamplifier and dynamic latch circuit are designed by using Cadence Schematic Editor. The preamplifier circuit schematic is shown in Figure 5. In the two-stage dynamic comparators, the size of the input transistors are calculated to achieve a given offset voltage.

The preamplifier is produced by combination of two PMOS transistors and three NMOS transistors. Two input signals are applied at NM1 and NM2 transistor in common mode and differential mode to get the gain. The output 01+ and 01- of this preamplifier is connected to the latch circuit. The CLK is connected to the PM0, PM1 and NM0 transistors.

The main circuit is the dynamic latch circuit. This is where the signal will be converted from analog to digital signal. The circuit is shown in Figure 6. The dynamic latch circuit consists of four PMOS transistors and five NMOS transistors. The input of this dynamic latch is from the preamplifier circuit.

The output of the preamplifier which are 01+ and 01-, are connected to the NM6 and NM7 respectively. The CLK- signal that is inverted form CLK are connected to the PM2, PM5, and NM3 transistors. NM3 transistor is used to cut the path from VDD to GND during the reset phase in order to avoid a DC power consumption in the second stage.

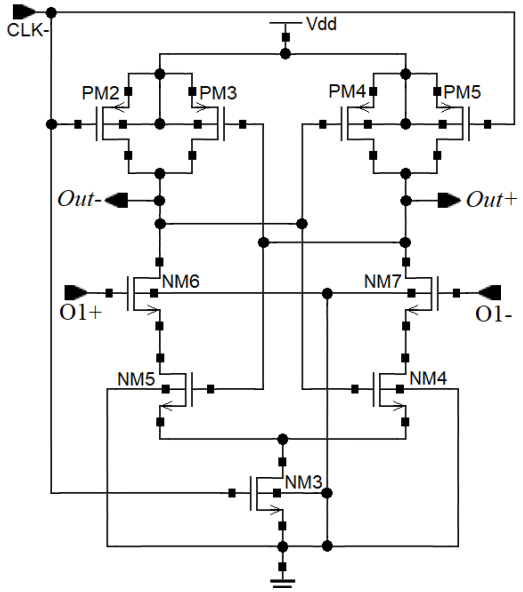

Figure 6: The proposed dynamic latch circuit

4. RESULTS

4.1. Transient analysis

Figure 7 shows the output signal of the preamplifier circuit. The input signal is in common mode voltage. The preamplifier circuit has produced the correct output.

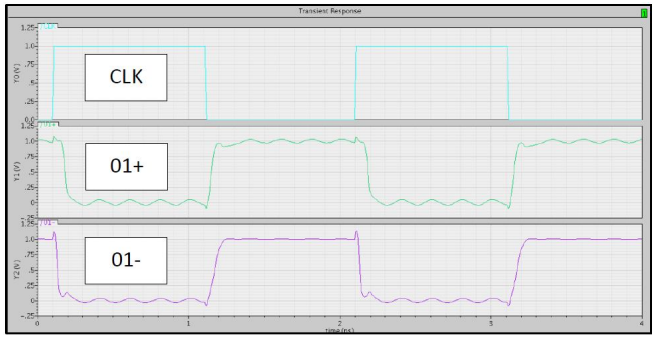

Figure 7: Output voltage of the preamplifier stage

In Figure 7, the positive sinewave input (Vin+) is at 2.5 GHz with amplitude of 500 mV, and the negative input (Vin-) is also at 2.5 GHz but the amplitude is 700 mV. This is to simulate a condition of Vin+ is less than Vin-. The Vin+ is connected to transistor NM1 and Vin- is connected to transistor NM2.

Figure 8 shows the combination of the preamplifier circuit and dynamic latch circuit. An inverter circuit is used to convert the clock signal. With this, the input clock signal at the preamplifier circuit is a positive edge and at the dynamic latch circuit it is a negative edge. The voltage supply used is 1V. The clock signal is 500 MHz or 2 ns per cycle.

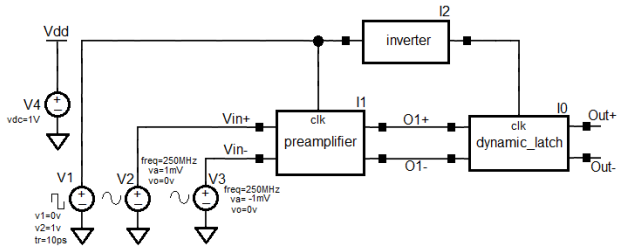

Figure 8: The proposed dynamic latch voltage comparator circuit

The proposed two stages comparator is working with only one clock to reduce the complexity and power consumption. The input for latch is from the preamplifier (01+ and 01-). In its operation, during the pre-charge (reset phase) the CLK is equal to 0V, thus both PMOS transistors PM0 and PM1 are turned on and they charged 01+ and 01- to VDD (see Figure 5). At this moment, the NM0 transistor is turned off. During the evaluation phase (decision making) the clock is equal to VDD. 01+ and 01- nodes are discharged to the ground. The output latch stage difference at Out nodes into full scale digital level. Out+ node will output logic high or equal to VDD if the voltage difference at 01 nodes is positive (01+ > 01-) and Out+ will be low or equal to 0 otherwise.

The latch circuit start make the comparison when in the positive cycle of the clock. Figure 9 shows the output of the comparator (Out+ and Out-). Output are read during the evaluation phase. It is shown the output are correct and they are at the opposite phase.

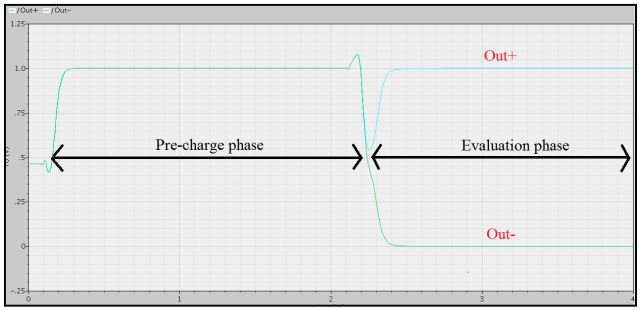

Figure 9: Output voltage of the latch stage in the proposed comparator

4.2. Delay

The delay is calculated in the evaluation phase when the comparator is starting to make comparison as shown in Figure 10. The delay of the proposed voltage comparator is much better than the circuit by Zhang et al. which has a delay of 200 ps10. The proposed comparator has a delay of 113.6 ps.

4.3. Power consumption

To reduce the power consumption, the circuit used 1 V for the voltage supply and has reduced the total number of transistors. The proposed comparator consumed only 85.1 uW.

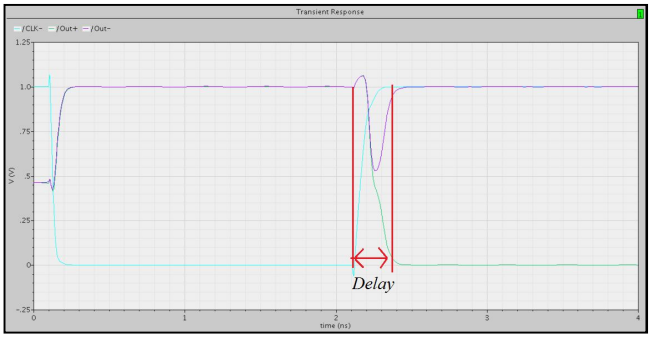

Figure 10: The delay of the output waveform of the comparator

Table 1 shows the result from several other voltage comparator designs and the proposed circuit. The results are in terms of voltage supply and CMOS technology used, power consumption and delay.

Table 1: Result of voltage comparator circuit

References	V_{DD} (V)	CMOS Technology (nm)	Power Consumption (uW)	Delay (ns)
[1]	1	90	148	79
[7]	1	180	39.7	60.29
[10]	1.8	180	420	0.20
Proposed circuit	1	130	85.1	0.12

Although the comparison cannot be made on one to one basis due to different platform and technology used, nevertheless it can be said the proposed comparator has able to produce a low power consumption circuit with a short delay. The comparator circuit reported by Singh has a much lower power consumption, but its delay is very high [7]. On the other hand, circuit by Zhang et al. was able to produce the high speed but it consumed high power [10].

4.4. Circuit analysis

This circuit have been tested with several values of voltage supply to analyze the optimal total power consumption and the delay. Table 2 shows the result of the analysis.

Table 2: Comparison of power consumption and delay

Voltage supply (V)	Delay (ps)	Power consumption (uW)
1.4	78.5	226.9
1.2	88.6	140.7
1.0	113.6	85.1
0.8	211.9	52.0
0.6	515.1	21.0

From the result in Table 2, the delay and power consumption versus voltage supply have been plotted. Figure 11 illustrates

the graph. Based on Figure 11, the suitable voltage supply for this circuit is 1 V because it give the most optimal power consumption and delay. At 1 V of voltage supply the total average power consumed is 85.1 uW and the delay is 113.6 psThe submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. It is the obligation of the authors to cite relevant prior work.

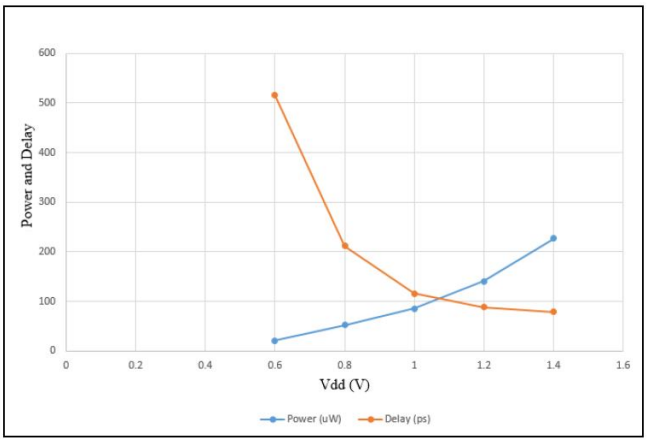

Figure 11: Graph of delay and power consumption versus voltage supply.

5. CONCLUSION

In this paper, a latch comparator circuit for high-speed ADCs has been designed. The comparator circuit is designed to have low power consumption and less propagation delay. By using Cadence EDA software tools and Silterra 130 nm technology, the power consumption is 85.1 µW and the propagation delay is 113.6 ps. The sizes of all the transistors of the proposed comparator are optimized in such a way that they produce low power and fast circuit which is suitable for high speed ADCs.

ACKNOWLEDGEMENT

The work is supported by the Faculty of Electrical and Electronic Engineering (FKEE), Universiti Tun Hussein Onn Malaysia (UTHM), Silterra and Collaborative Microelectronic Design Excellence Centre (CEDEC).

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